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SC122

Low Voltage Synchronous Boost Converter

POWER MANAGEMENT

Features

- Input voltage — 0.7V to 1.6V
- Minimum start-up voltage — 0.85V
- Output voltage fixed at 3.3V
- Peak input current limit — 350mA typically
- Output current 95mA at V_{IN} = 1.6V, 50mA at V_{IN} = 0.9V
- Efficiency up to 80%
- Internal synchronous rectifier
- Switching frequency — 1.2MHz
- Power save (voltage hysteretic) control
- Anti-ringing circuit
- Operating supply current (measured at OUT) — 40µA
- No forward conduction path during shutdown
- MLPD-UT-6 1.5 × 2.0 × 0.6 (mm) package
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Electric toothbrushes
- Personal medical products
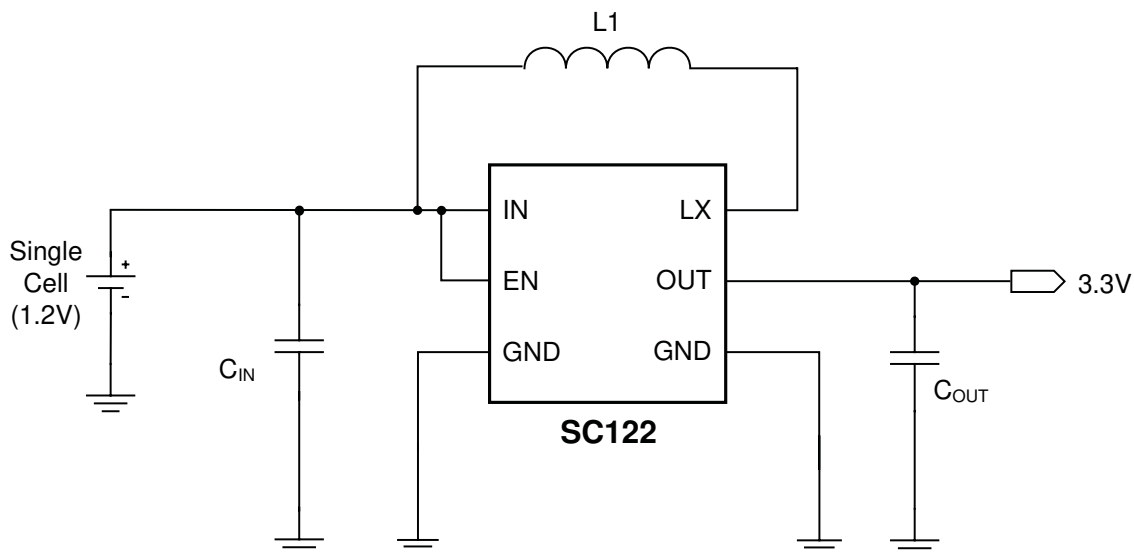- Single-cell alkaline, NiCd, or NiMH applications

Description

The SC122 is a high efficiency, low noise, synchronous step-up DC-DC converter. It produces a fixed 3.3V output from a single cell alkaline or NiMH battery. It features an internal 1.2A switch and synchronous rectifier to achieve high efficiency and to eliminate the need for an external Schottky diode.

The SC122 operates exclusively in voltage-hysteretic power save mode (PSAVE) for high efficiency under light load conditions. It features anti-ringing circuitry for reduced EMI in noise sensitive applications. While disabled, the output remains in a high impedance state to preserve the charge on the output capacitor. This permits ultra-low idle quiescent currents in applications in which the SC122 can be periodically enabled by an external controller to recharge the output capacitor.

Low quiescent current is obtained despite a high 1.2MHz operating frequency. Small external components and the space saving MLPD-UT-6, 1.5×2.0×0.6 (mm) package, make this device an excellent choice for small handheld applications that require the longest possible battery life.

Typical Application Circuit

Pin Configuration

LX — 1
GND — 2
IN — 3
6 — OUT
5 — GND
4 — EN

TOP VIEW

T

MLPD-UT; 1.5×2, 6 LEAD

$\theta_{JA} = 84°C/W$
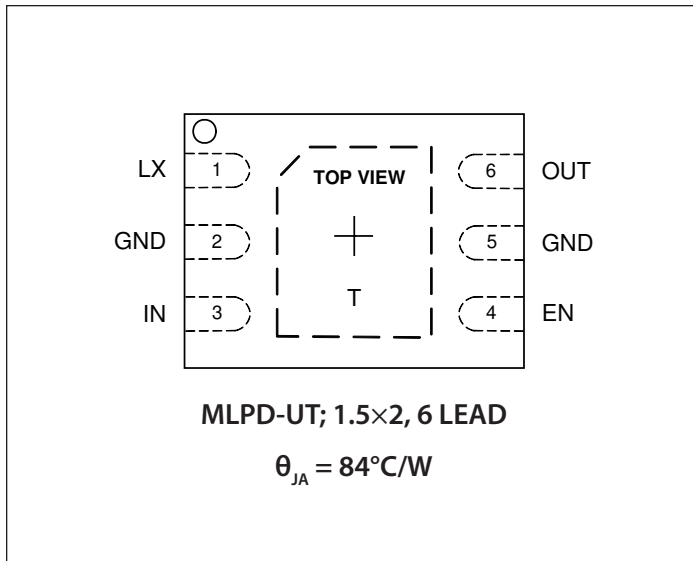
Ordering Information

Device	Package
SC122ULTRT[1][2]	MLPD-UT-6 1.5×2
SC122EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and compliant and halogen-free.

Marking Information

122
○yw

MLPD-UT; 1.5×2, 6 LEAD

yw = date code

SEMTECH
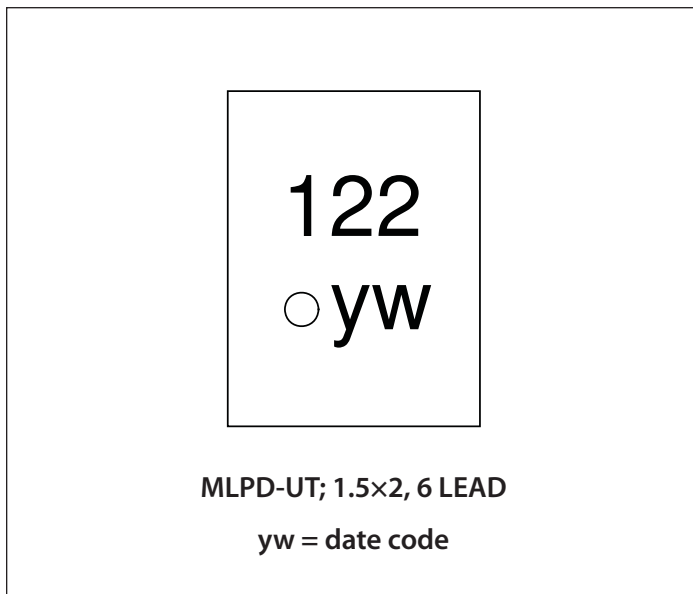
Absolute Maximum Ratings

IN, OUT, LX (V) . . . . -0.3 to +6.0

EN (V) . . . . -0.3 to (V_{IN} + 0.3)

ESD Protection Level[1] (kV) 3

Recommended Operating Conditions

Ambient Temperature Range (°C). . . . . 0 to +70

V_{IN} (V) . . . . 0.7 to 1.6

V_{OUT} (V) 3.3

Thermal Information

Thermal Resistance Junction-Ambient[2] (°C/W) 84

Maximum Junction Temperature (°C) 150

Storage Temperature Range (°C) . . . . -65 to +150

Peak IR Reflow Temperature (10s to 30s) (°C) . . . . . . +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 1.2V, C_{IN} = C_{OUT} = 22µF, L_1 = 4.7µH, T_A = 0 to +70°C. Typical values are at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		0.7		1.6	V
Output Voltage	V_{OUT}			3.3		V
Output Accuracy	$V_{OUT-tol}$	V_{EN} = V_{IN}	-3		3	%
Minimum Startup Voltage	V_{IN-SU}	I_{OUT} < 1mA		0.85		V
Operating Supply Current [1]	I_{OUT-Q}	V_{EN} = V_{IN}, I_{OUT} = 0mA, V_{OUT} = 3.3V		40		µA
Disabled OUT Leakage Current	$I_{OUT-DIS}$	V_{EN} = 0, V_{OUT} = 3.3V (externally forced)		2		µA
Disabled IN Quiescent Current	I_{IN-DIS}	V_{EN} = 0, V_{IN} = 1.6, V_{OUT} = 3.3V (externally forced)		4		µA
Shutdown Current	$I_{IN-SHDN}$	V_{EN} = 0V, V_{IN} = 1.6V, V_{OUT} = 0V		8.5		µA
Internal Oscillator Frequency	f_{OSC}	while bursting		1.2		MHz
Startup Time	t_{SU}	From V_{EN} low-to-high transition		1		ms
Minimum V_{IN} for Restart [2]	$V_{IN-Restart}$	Lowest V_{IN} to ensure re-enable within 300µs, V_{OUT} = 3.1V (externally forced)			1.0	V
P-Channel ON Resistance	$R_{DS(ON)P}$	I_{LX} = 50mA		0.6		Ω
N-Channel ON Resistance	$R_{DS(ON)N}$	I_{LX} = 50mA, V_{IN}=1.6V		0.5		Ω
P-Channel Startup Current Limit	$I_{LIM(P)-SU}$	V_{IN} = 1.2V, V_{EN} > V_{IH}		100		mA

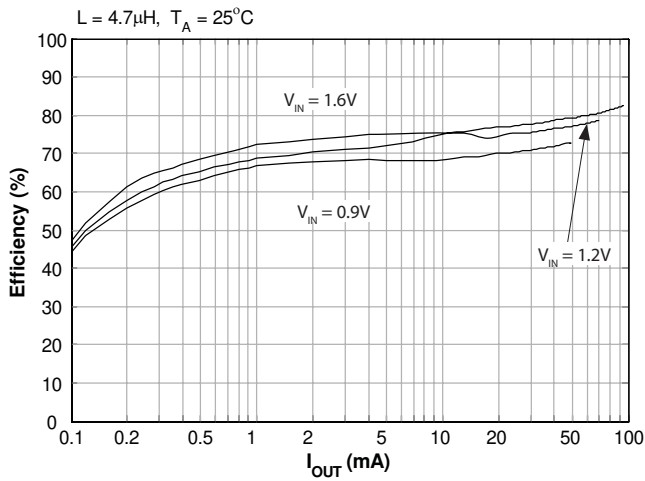## Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
N-Channel Current Limit	$I_{LIM(N)}$	$V_{IN} = 1.2V$		350		mA
LX Leakage Current PMOS	I_{LXPLK}	$T_A = 25°C$, $V_{LX} = 0V$, $V_{OUT} = 3.3V$			1	µA
LX Leakage Current NMOS	I_{LXNLK}	$T_A = 25°C$, $V_{LX} = 3.3V$, $V_{OUT} = 3.3V$			1	µA
Logic Input High	V_{IH}	$V_{IN} = 1.2V$	0.4			V
Logic Input Low	V_{IL}	$V_{IN} = 1.2V$			0.1	V
Logic Input Current High	I_{IH}	$V_{EN} = V_{IN} = 1.2V$			1	µA
Logic Input Current Low	I_{IL}	$V_{EN} = 0V$	-0.2			µA

NOTES:

(1) Quiescent operating current is drawn from the OUT pin while in regulation. The quiescent operating current projected to the IN pin is approximately $I_Q \times (V_{OUT}/V_{IN})$.

(2) Restart occurs when the EN pin transitions from low to high while the output voltage is at or near the regulation value (3.3V). See the application section "The Enable Pin" for details.
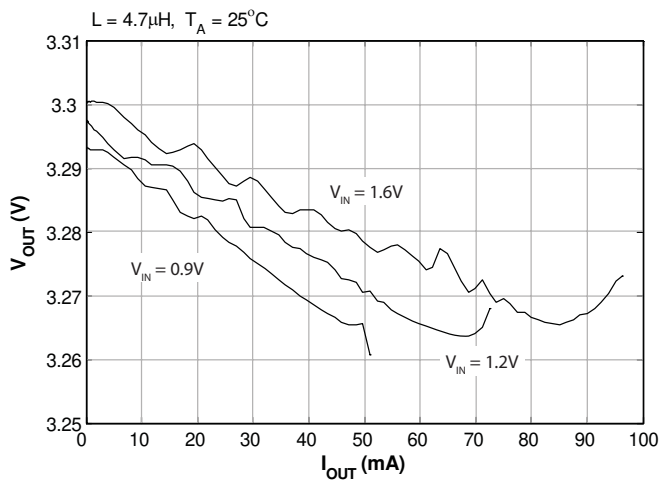
SEMTECH

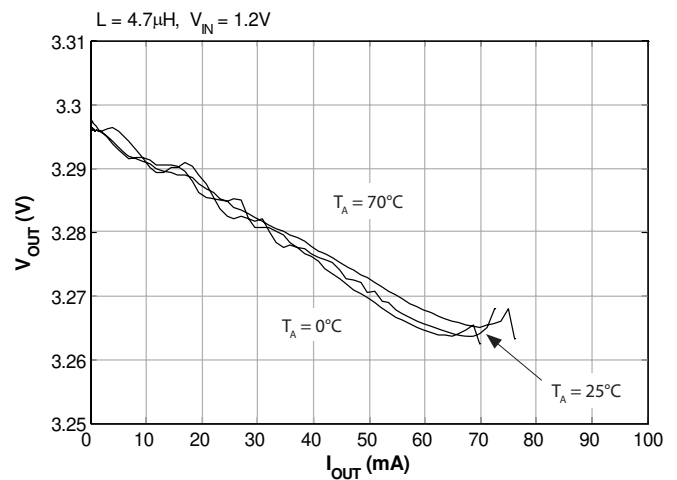## Typical Characteristics — V$_{OUT}$ = 3.3V

Efficiency vs. I$_{OUT}$
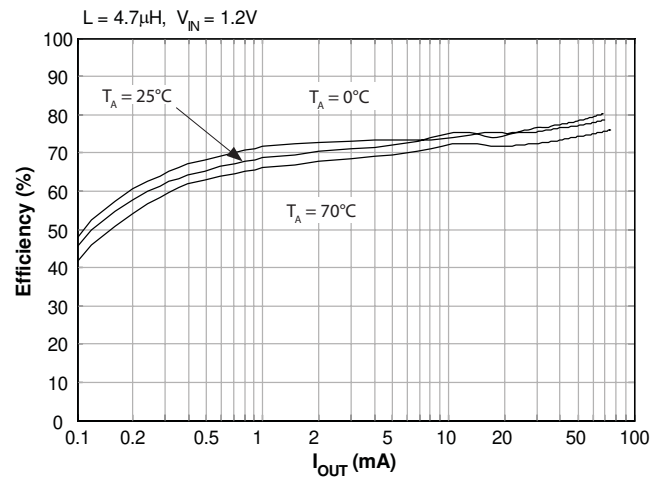
L = 4.7µH, T$_A$ = 25°C

V$_{IN}$ = 1.6V

V$_{IN}$ = 0.9V

V$_{IN}$ = 1.2V

Efficiency (%)

I$_{OUT}$ (mA)

Efficiency vs. I$_{OUT}$

L = 4.7µH, V$_{IN}$ = 1.2V

T$_A$ = 25°C

T$_A$ = 0°C

T$_A$ = 70°C

Efficiency (%)

I$_{OUT}$ (mA)

Load Regulation

L = 4.7µH, T$_A$ = 25°C

V$_{IN}$ = 1.6V

V$_{IN}$ = 0.9V

V$_{IN}$ = 1.2V

V$_{OUT}$ (V)

I$_{OUT}$ (mA)

Load Regulation

L = 4.7µH, V$_{IN}$ = 1.2V

T$_A$ = 70°C

T$_A$ = 0°C

T$_A$ = 25°C

V$_{OUT}$ (V)

I$_{OUT}$ (mA)

Line Regulation — Low Load

L = 4.7µH, I$_{OUT}$ = 1mA

T$_A$ = 0°C, 25°C, 70°C

V$_{OUT}$ (V)

V$_{IN}$ (V)

Line Regulation — High Load

L = 4.7µH, I$_{OUT}$ = 45mA

T$_A$ = 0°C, 25°C, 70°C

V$_{OUT}$ (V)

V$_{IN}$ (V)

5

SEMTECH
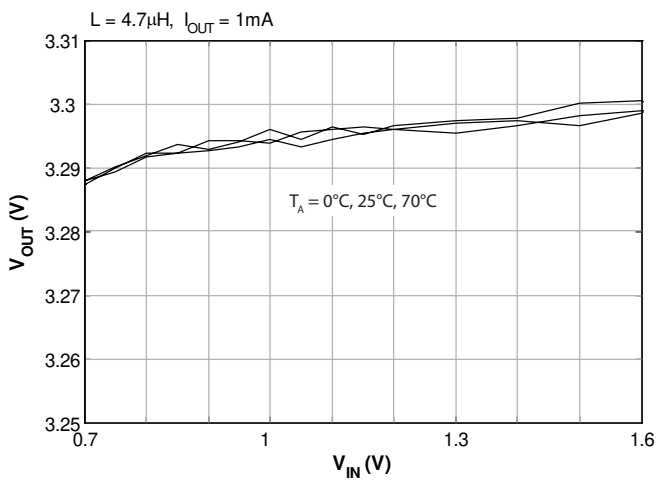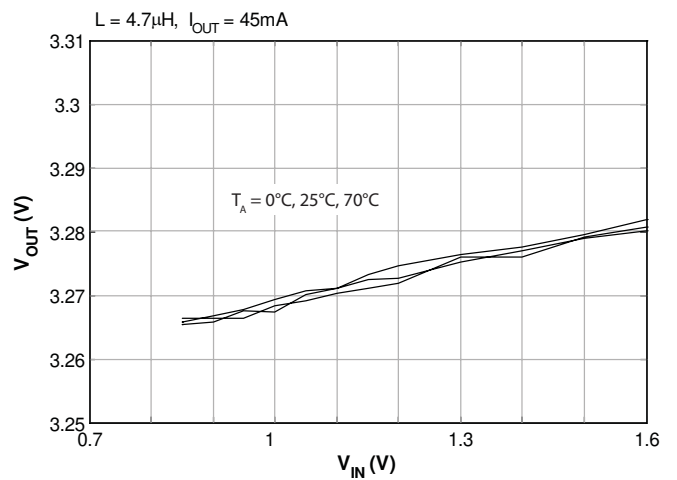
Typical Characteristics — V$_{OUT}$ = 3.3V (continued)

Temperature Regulation — Low Load

L = 4.7µH, I$_{OUT}$ = 1mA
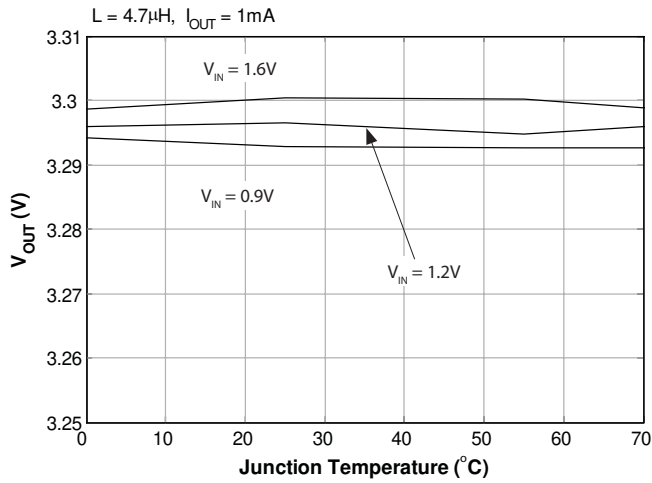
Temperature Regulation — High Load

L = 4.7µH, I$_{OUT}$ = 45mA
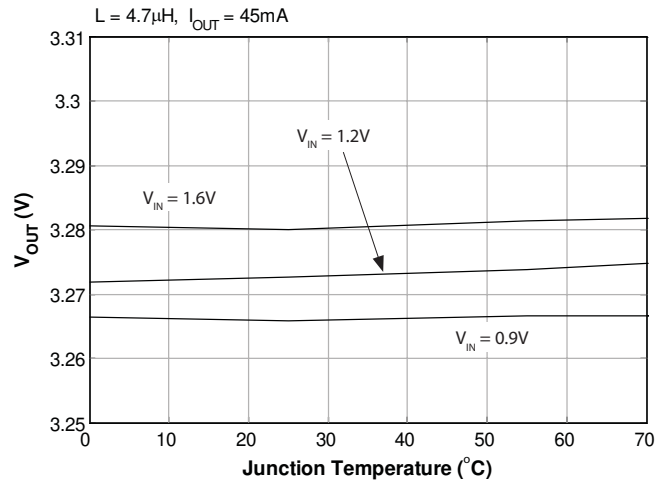
Startup Max. Load Current vs. V$_{IN}$

L = 4.7µH
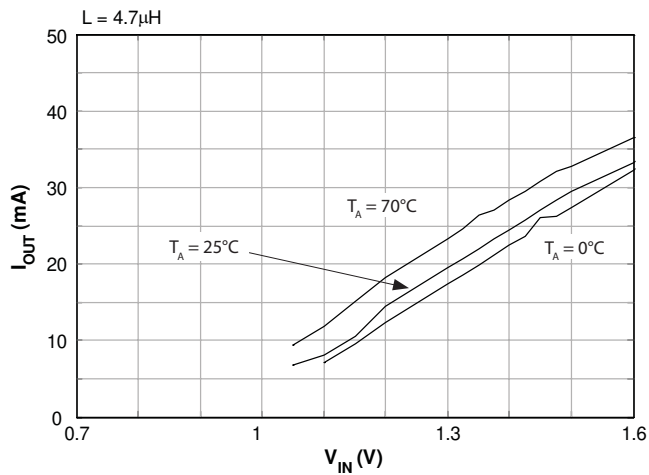
Startup Min. Load Resistance vs. V$_{IN}$

L = 4.7µH
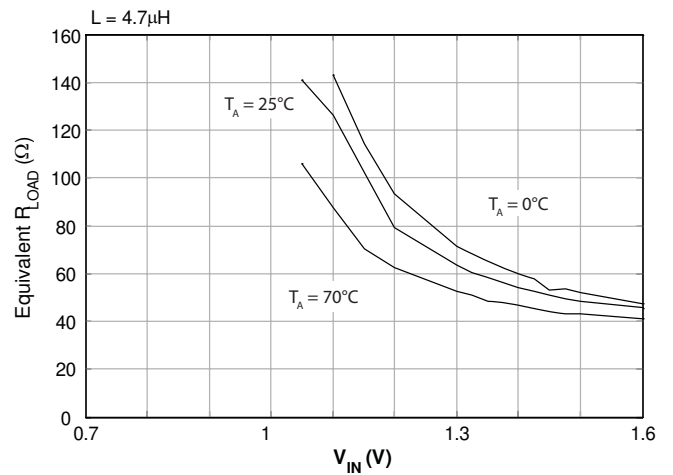
Maximum I$_{OUT}$ vs. V$_{IN}$

L = 4.7µH
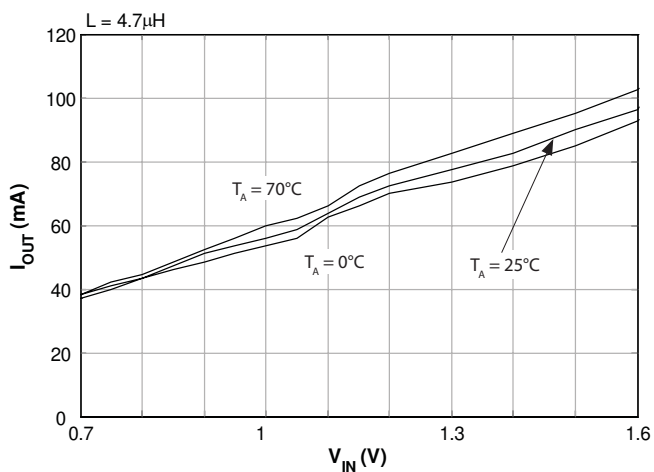
Minimum Start-up Voltage vs. Temperature

V$_{OUT}$ = 3.3V, I$_{OUT}$ = 1mA

SEMTECH
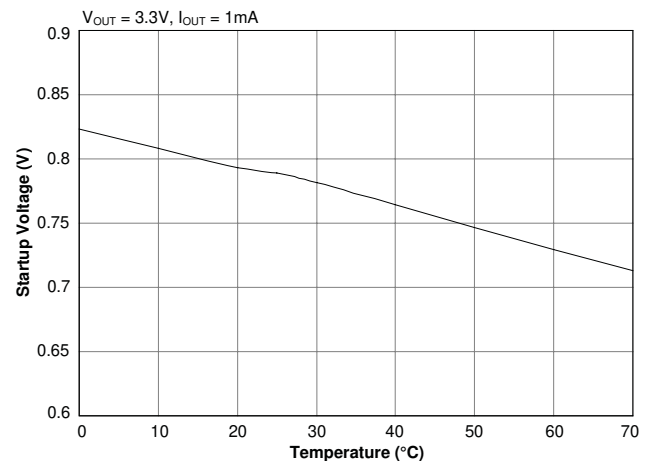
Pin Descriptions

MLPD Pin #	Pin Name	Pin Function
1	LX	Switching node — connect an inductor from the input supply to this pin.
2, 5	GND	Signal and power ground connections.
3	IN	Battery input and damping switch connection.
4	EN	Enable digital control input — active high.
6	OUT	Output voltage supply pin — requires an external 10µF bypass capacitance (effective under V_{OUT} bias) for normal operation.
T	Thermal Pad	Thermal Pad is for heat sinking purposes — connect to ground using multiple vias, not connected internally.

Block Diagram
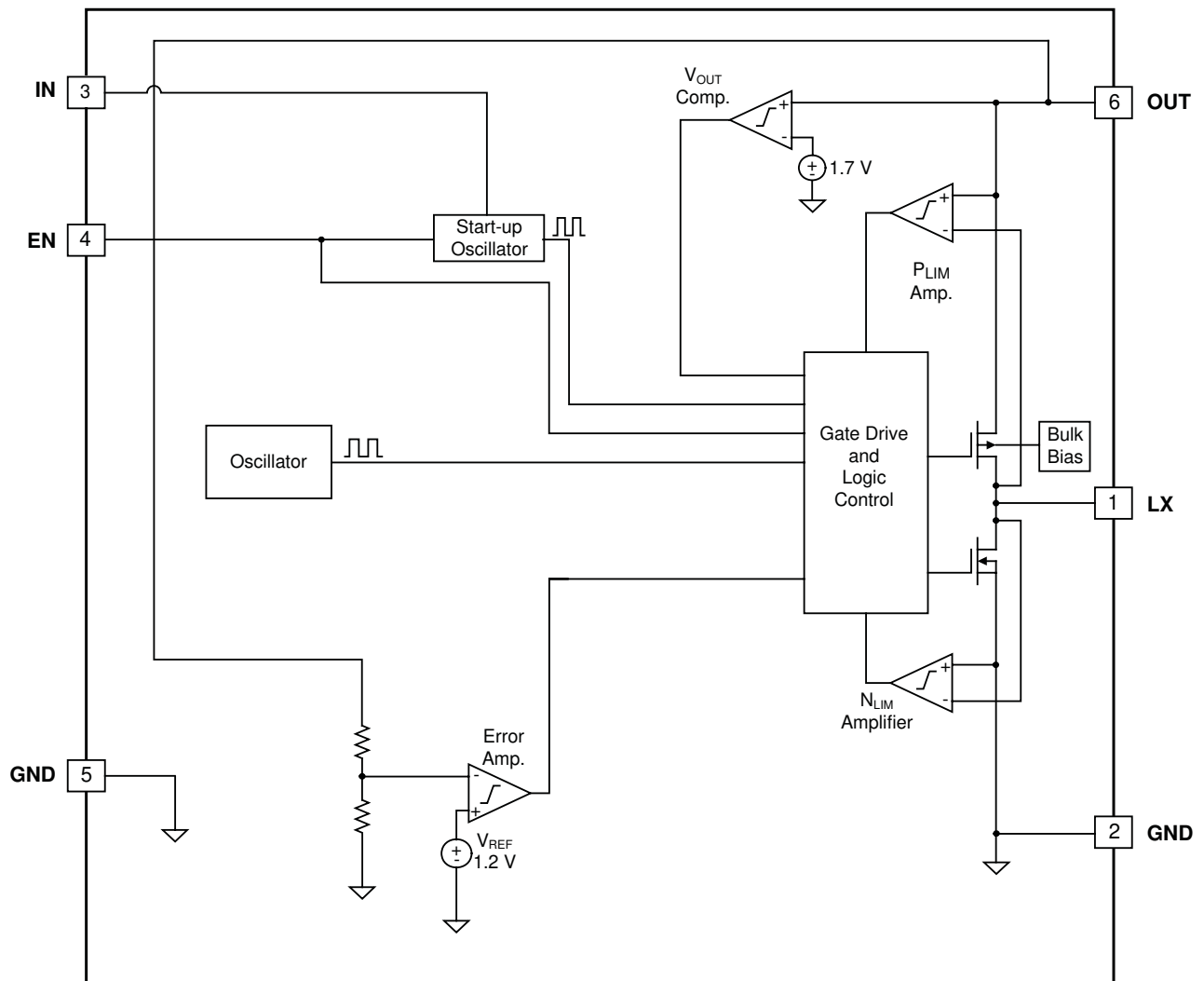
Applications Information

Detailed Description
The SC122 is a synchronous step-up hysteretic DC-DC converter utilizing a 1.2MHz fixed frequency switching architecture. It provides a fixed 3.3V output from an input voltage as low as 0.7V, with an unloaded startup input voltage of 0.85V.

The SC122 operates exclusively in PSAVE regulation mode (bursts of switching boost cycles, alternating with periods of an output-high-impedance state). It has quiescent current consumption as little as 40μA into the OUT pin. It features anti-ringing circuitry for reduced EMI in noise sensitive applications. The boost cycles can be disabled with an active-high enable input. While disabled, the output remains in a high impedance state to preserve the charge on the output capacitor. This permits ultra-low idle quiescent currents in applications in which the SC122 can be periodically enabled by an external controller to recharge the output capacitor.

The regulator control circuitry is shown in the Block Diagram. It is comprised of a feedback controller, an internal 1.2MHz oscillator, an n-channel Field Effect Transistor (FET) between the LX and GND pins, and a p-channel FET between the LX and OUT pins. The current flowing through both FETs is monitored and limited as required for startup and PSAVE regulator operation. An external inductor must be connected between the IN pin and the LX pin.

During the burst phase of PSAVE operation, the controller alternates between the on-state and the off-state. During the on-state the n-channel FET is turned on, grounding the inductor at the LX pin. This causes the current flowing from the input supply through the inductor to ground to ramp up. The on-state continues until the first of two limits is reached, either the n-channel current limit $I_{LIM(N)}$, or the on-time limit $T_{ON-MAX} = 0.9 \times 1/f_{OSC}$. Then during the off-state, the n-channel FET is turned off and the p-channel FET is turned on, connecting the inductor between IN and OUT. The (now decreasing) inductor current flows from the input to the output, transferring the inductor energy to the output and boosting the output voltage above the input voltage for the remainder of the cycle period $T = 1/f_{OSC}$. The cycle then repeats to re-energize the inductor.

The burst phase continues until V_{OUT} reaches an upper voltage threshold, at which point both FETs are turned off.

This begins the high-impedance phase. The output capacitor then discharges into the load until V_{OUT} reaches a lower voltage threshold, which initiates a new burst phase. The upper and lower voltage thresholds differ by approximately 50mV, and were chosen to provide an average output voltage of 3.3V. The time between bursts is determined by the discharge rate of the output capacitor, which depends on the value of output capacitance and the magnitude of the applied load. Figure 1 illustrates PSAVE regulation.
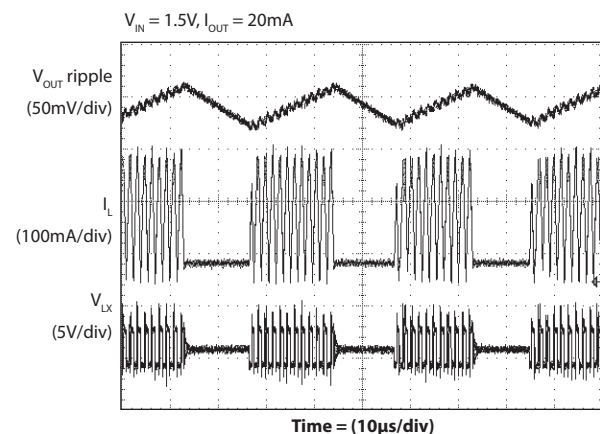

$V_{IN} = 1.5V, I_{OUT} = 20mA$

V_{OUT} ripple (50mV/div)

I_L (100mA/div)

V_{LX} (5V/div)

Time = (10μs/div)

Figure 1 — PSAVE Regulation Waveforms

The Enable Pin
The EN pin is a high impedance logical input that can be used to enable or disable the SC122 under processor control. $V_{EN} > 0.4V$ will enable the output. The startup sequence from the EN pin is identical to the startup sequence from the application of input power.

$V_{EN} < 0.1V$ will disable regulation and set the LX pin in a high-impedance state (turn off both FET switches). The OUT pin is also left in a high-impedance state when disabled. The SC122 can be disabled while maintaining the output voltage on the output capacitor, for the lowest possible quiescent current, while supporting a low application idle state load. The SC122 can then be periodically re-enabled for a brief time to refresh the charge held on the output capacitor, then disabled for an extended time as determined by the discharge rate of the output capacitor while supplying the idle-state load current. For $V_{IN} > V_{IN-Restart}$, and over the full specified temperature range, regulation will be fully enabled within 300μs of a high voltage on the EN pin with V_{OUT} discharged to as low as 2.5V.

Applications Information (continued)

A suggested very low duty cycle refresh oscillator circuit is included on the SC122 EVB-RM, the SC122 Evaluation Board with Refresh Modulation.

Regulator Startup, Short Circuit Protection, and Current Limits

The SC122 permits power up at input voltages from 0.85V to 1.6V. Startup current limiting of the internal switching n-channel and p-channel FET power devices protects them from damage in the event of a short between OUT and GND. This protection prevents startup into an excessive load.

At the beginning of the cycle, the p-channel FET between the LX and OUT pins turns on with its current limited to approximately 100mA, the short-circuit output current. When V_{OUT} approaches V_{IN} (still below 1.7V), the n-channel current limit is set to 350mA (the p-channel limit is disabled), an internal oscillator turns on (approximately 200kHz), and a fixed 75% duty cycle PWM-type operation begins. When the output voltage exceeds 1.7V, fixed frequency PSAVE operation begins, with the duty cycle determined by an n-channel FET peak current limit of 350mA.

Note that startup with a regulated active load is not the same as startup with a resistive load. The resistive load output current increases proportionately as the output voltage rises until it reaches V_{OUT}/R_{LOAD}, while a regulated active load presents a constant load as the output voltage rises from 0V to V_{OUT}. Note also that if the load applied to the output exceeds the startup current limit, the criterion to advance to the next startup stage may not be achieved. In this situation startup may pause at a reduced output voltage until the load is reduced further.

Output Overload and Recovery

As the output load increases, the duration of each burst increases, and the time between bursts decreases. The output load reaches its maximum when the burst duration becomes indefinite (and the time between bursts becomes zero). At this time, all the energy stored in the inductor during the on-time portion of each burst cycle is discharged into the output during off-time. The inductor current reduces to zero just as the next on-time begins.

Above this critical maximum load, the output voltage will decrease rapidly, and the startup current and switching limits will be invoked in reverse order as the output voltage falls through its various startup voltage thresholds. How far the output voltage drops depends on the load voltage vs. current characteristic.

A reduction in input voltage, such as a discharging battery, will lower the load current at which overload occurs. At the overload threshold, the energy stored in the inductor at the end of each on-time is the same for all V_{IN}. But since the voltage increase above the input voltage is greater, the available output current, $I_{OUT} = P/(V_{OUT} - V_{IN})$, must decrease.

When an overload has occurred, the load must be decreased to permit recovery. The conditions required for overload recovery are identical to those required for successful initial startup.

Anti-ringing Circuitry

When both FET switches are simultaneously turned off, an internal switch between the IN and LX pins is closed. This provides a moderate resistance path across the inductor to dampen the oscillations at the LX pin. This effectively reduces EMI that can develop from the resonant circuit formed by the inductor and the drain capacitance at LX. The anti-ringing circuitry is disabled between PSAVE bursts.

Inductor Selection

The inductance value primarily affects the amplitude of inductor current ripple (ΔI_L). The inductor peak current $I_{L-max} = I_{L-avg} + \Delta I_L/2$, where I_{L-avg} is the inductor current averaged over a full on/off cycle, is subject to the n-channel FET peak current limit $I_{LIM(N)}$. The inductor average current is equal to the output load current. Increasing inductance reduces ΔI_L and therefore increases the maximum supportable output current.

The performance plots of this datasheet were obtained with L = 4.7μH. Larger values of inductance can provide higher maximum output currents.

Any chosen inductor should have low DCR, compared to the R_{DS-ON} of the FET switches, to maintain efficiency. For DCR << R_{DS-ON}, further reduction in DCR will provide diminishing benefit. The inductor I_{SAT} value must exceed $I_{LIM(N)}$. The inductor self-resonant frequency should exceed

Applications Information (continued)

$5 \times f_{osc}$. Any inductor with these properties should provide satisfactory performance.

The following table lists the manufacturers of recommended inductor options.

Manufacturer/ Part #	Value (µH)	DCR (mΩ)	Rated Current (mA)	Tolerance (%)	Dimensions L×W×H (mm)
Sumida 5508472xxxx	4.7	3800	90	2/5/10/20	2.2 × 1.4 × 1.6
Murata LQM31PN4R7M00L	4.7	300	700	20	3.2 × 1.6 × 0.85

Capacitor Selection

Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended for input bypassing and output filtering. Low-ESR tantalum capacitors are not recommended due to possible reduction in capacitance seen at the switching frequency of the SC122. Ceramic capacitors of type Y5V are not recommended as their temperature coefficients make them unsuitable for this application.

The input and output each require a minimum capacitance value of 10µF at the programmed output voltage. This must be considered when choosing small package size capacitors as the DC bias must be included in their derating to ensure this required value. For example, a 10µF 0805 capacitor may provide sufficient capacitance at low output voltages but may be too low at higher output voltages. Therefore, a higher nominal capacitance value may be required to provide the minimum of 10µF at these higher output voltages. Additional output capacitance can be used extend the time between bursts, or to improve load transient response. The following table lists recommended capacitors.

Manufacturer/ Part Number	Value (µF)	Rated Voltage (VDC)	Type	Case Size
Murata GRM21BR60J226ME39B	22	6.3	X5R	0805
Murata GRM31CR71A226KE15L	22	10	X7R	1206

PCB Layout Considerations

Good layout can enhance the performance of the DC-DC converter and can avoid EMI problems, ground bounce, and resistive voltage losses. The recommended layout is shown in Figure 2.

The following simple design rules can be implemented to ensure good layout:

- Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
- Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling capacitance between the LX node and the ground plane.
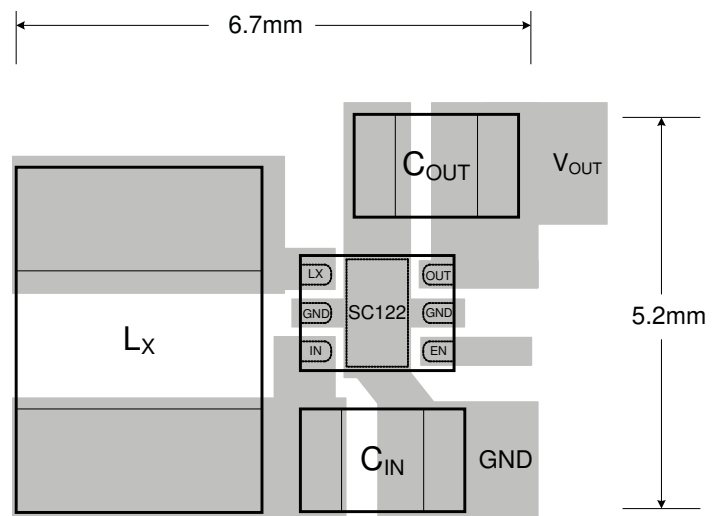- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
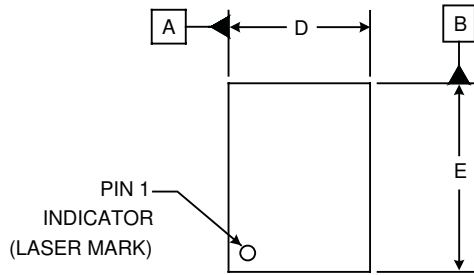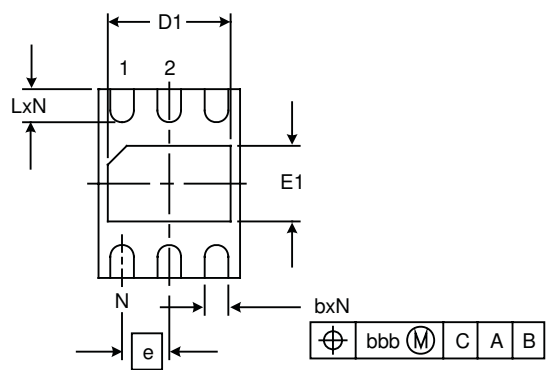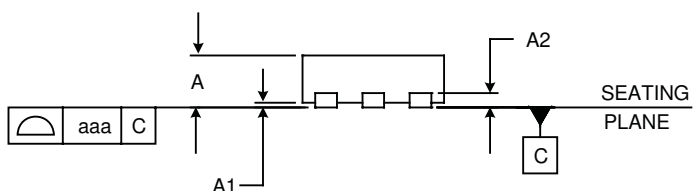

Figure 2 — Recommended Layout

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Outline Drawing — MLPD-UT-6 1.5x2

DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(.152)	
b	.007	.010	.012	0.18	0.25	0.30
D	.055	.059	.063	1.40	1.50	1.60
D1	.035	-	.055	0.90	-	1.40
E	.075	.079	.083	1.90	2.00	2.10
E1	.026	.031	.035	0.65	0.80	0.90
e		.020 BSC			0.50 BSC	
L	.012	.014	.016	0.30	0.35	0.40
N		6			6	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-UT-6 1.5x2
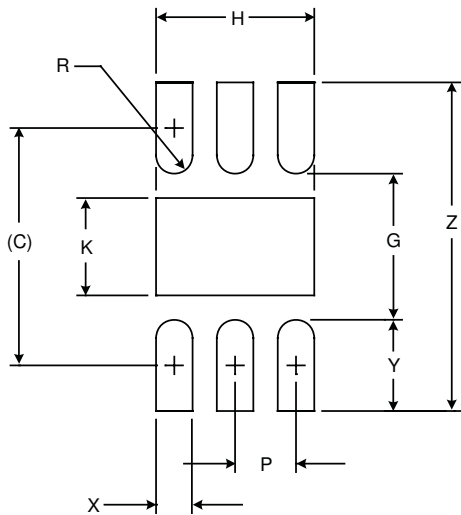
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.077)	(1.95)
G	.047	1.20
H	.051	1.30
K	.031	0.80
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.030	0.75
Z	.106	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.

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