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SC1405D
High Speed Synchronous Power MOSFET Smart Driver

Description

The SC1405D is a Dual-MOSFET Driver with an internal Overlap Protection Circuit to prevent shoot-through. Each driver is capable of driving a 3000pF load in 15ns rise/fall time and has ULTRA-LOW propagation delay from input transition to the gate of the power FETs. Adaptive Overlap Protection circuit ensures that the synchronous FET does not turn on until the top FET source has reached a voltage low enough to prevent shoot-through. The delay between the bottom gate going low to the top gate transitioning high is externally programmable via a capacitor to minimize dead time. The bottom FET may be disabled at light loads by keeping S_MOD low to trigger asynchronous operation, thus saving the bottom FET's gate drive current and inductor ripple current.

An internal voltage reference allows threshold adjustment for an Output Over-Voltage protection circuitry, independent of the PWM controller. The device provides overvoltage protection independent of the PWM feedback loop with a unique "adaptive OVP" comparator which rejects noise but responds quickly to a true OVP situation.

Under-Voltage-Lock-Out circuit is included to guarantee that both driver outputs are off when Vcc is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). A CMOS output provides status indication of the 5V supply. A low enable input places the IC in stand-by mode, reducing supply current to less than 10µA.

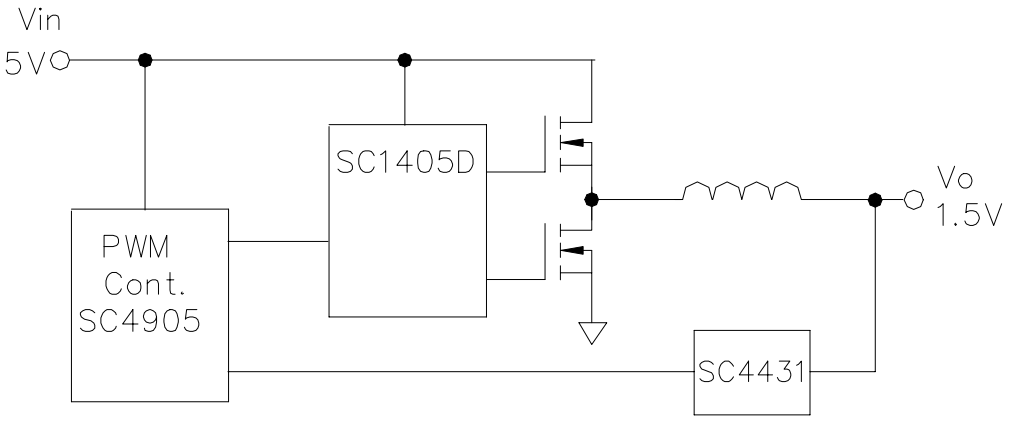
Features

- Fast rise and fall times (15ns with 3000pf load)
- **14ns max. Propagation delay (BG going with low)**
- Adaptive and programmable shoot-through protection
- Adaptive overvoltage protection
- Wide input voltage range (4.5V - 25V)
- Programmable delay between FETs
- Power saving asynchronous mode control
- Output overvoltage protection/overtemp shutdown
- Under-Voltage lock-out and power ready signal
- Less than 10µA stand-by current (EN=low)
- Power ready output signal
- High frequency (to 1.2MHz) operation allows use of small inductors and low cost caps in place of electrolytics
- TSSOP-14 package

Applications

- High Density/Fast transient microprocessor power supplies
- Motor Drives/Class-D amps
- High efficiency portable computers

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Minimum	Maximum	Units
V_{CC} Supply Voltage	V_{CCMAX}		-0.3	7	V
BST to PGND	$VMAX_{BST-PGND}$		-0.3	30	V
BST to DRN	$VMAX_{BST-DRN}$		-0.3	8	V
DRN to PGND	$VMAX_{DRN-PGN}$	DC	-2	25	V
DRN to PGND Pulse	$VMAX_{PULSE}$	t_{PULSE} < 100nS	-5	25	V
OVP_S to PGND	$VMAX_{OVP\ S-PGND}$		-0.3	10	V
EN, CO, DSPS, MODE, PRDY, DELAY to AGND			-0.3	V_{CC} + 0.3	V
AGND to PGND			-1	+1	V
Continuous Power Dissipation	Pd	Tamb = 25°C, T_J = 125°C Tcase = 25°C, T_J = 125°C		0.66 2.56	W
Thermal Impedance Junction to Case	θ_{JC}			40	°C/W
Thermal Impedance Junction to Ambient	θ_{JA}			150	°C/W
Junction Temperature Range	T_J		-40	+125	°C
Storage Temperature Range	T_{STG}		-65	+150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}			300	°C

NOTE:
(1) Specification refers to application circuit.

Electrical Characteristics - DC Operating Specifications

Unless otherwise specified: -40 < T_J < 125°C; V_{CC} = 6V; 4V < V_{BST} < 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}		4.6	5	6.0	V
Quiescent Current	Iq_stby	EN = 0V			10	µA
Quiescent Current, operating	Iq_op	V_{CC} = 5V, CO = 0V		1		mA
PRDY						
High Level Output Voltage	V_{OH}	V_{CC} = 4.7V, Iload = 10mA	4.5	4.55		V
Low Level Output Voltage	V_{OL}	V_{CC} < UVLO threshold, Iload = 10µA		0.1	0.2	V
Sink Current	I_{O_SINK}	VPRDY = 0.4V	5	10		mA

Electrical Characteristics - DC Operating Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DSPS_DR						
High Level Output Voltage	V_{OH}	V_{CC} = 4.6V, Cload = 100pF	4.15			V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.6V, Cload = 100pF			0.05	V
Under Voltage Lockout						
Start Threshold			4.2	4.4	4.6	V
Hysteresis	Vhys			0.05		V
Logic Active Threshold		EN is low			1.5	V
Overvoltage Protection						
Trip Threshold	V_{TRIP}		1.17	1.225	1.28	V
Hysteresis	$Vhys_{OVP}$			0.8		V
Trip Delay, 50mV Overdrive		T_J = 0 to 125°C	300	470	800	ns
Trip Delay, 100mV Overdrive		T_J = 0 to 125°C	125	225	400	ns
S_MOD						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Enable						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
CO						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			165		°C
Hysteresis	T_{HYST}			10		°C
High-Side Driver						
Peak Output Current	I_{PKH}			3		A
Output Resistance	$Rsrc_{TG}$ $Rsink_{TG}$	duty cycle < 2%, tpw < 100µs, TJ = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V (src)+V_{DRN} or VTG = 0.5V (sink)+VDRN		1 .7		Ω
Low-Side Drive						
Peak Output Current	I_{PKL}			3		A
Output Resistance	$Rsrc_{BG}$ $Rsink_{BG}$	duty cycle < 2%, tpw < 100µs, TJ = 125°C, V_{VS} = 4.6V, V_{BG} = 4V (src) or V_{LOWDR} = 0.5V (sink)		1.2 1.0		Ω

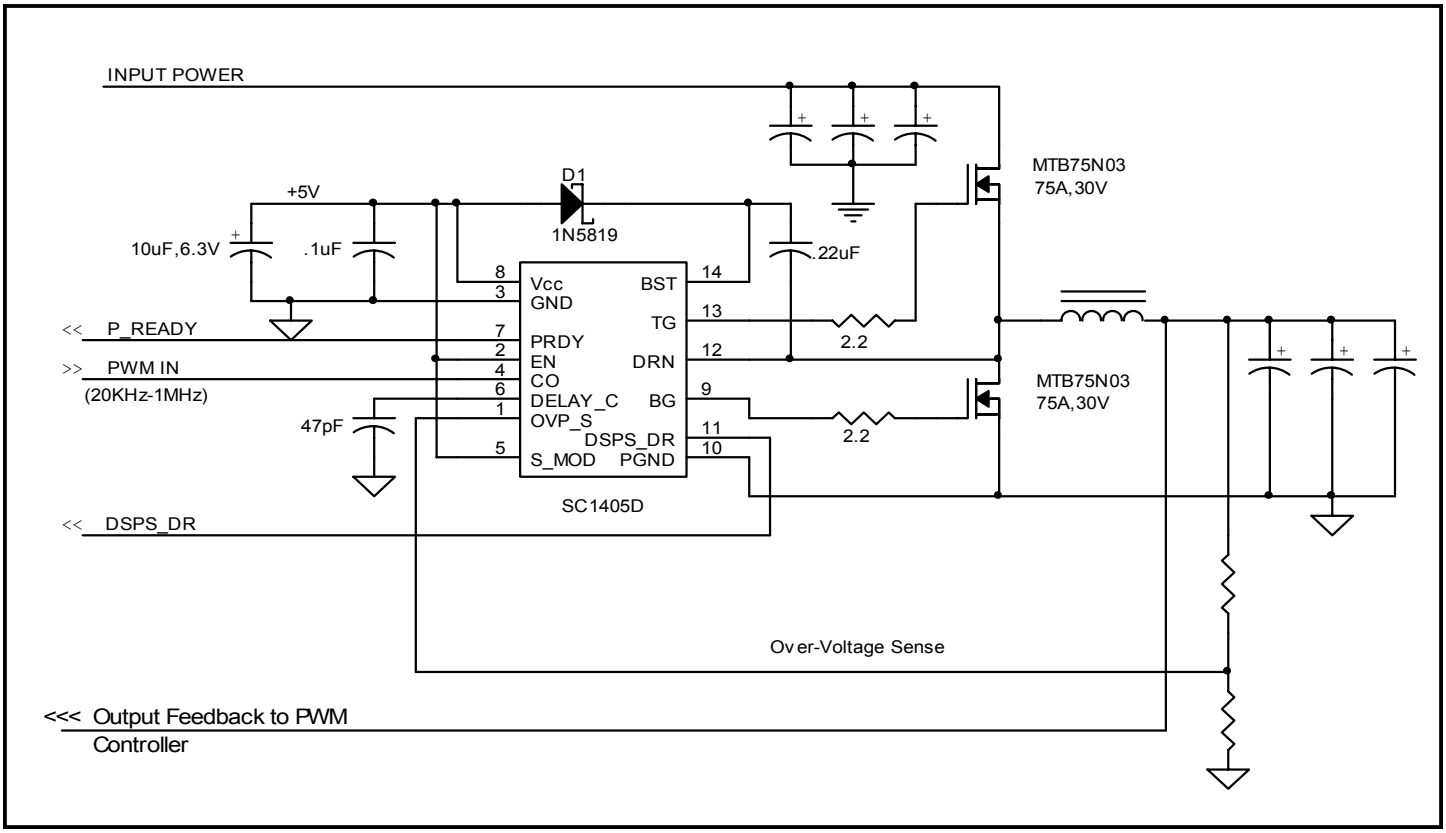
Electrical Characteristics - AC Operating Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Side Driver						
rise time	tr_{TG1}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		14	**23**	ns
fall time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		12	**19**	ns
propagation delay time, TG going high	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **C-delay=0**		20	**32**	ns
propagation delay time, TG going low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		15	**24**	ns
Low-Side Driver						
rise time	tr_{BG}	Cl = 3nF, V_{VS} = 4.6V,		15	**24**	ns
fall time	tr_{BG}	Cl = 3nF, V_{VS} = 4.6V,		13	**21**	ns
propagation delay time, BG going high	$tpdh_{BGHI}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **C-delay=0**		12	**19**	ns
propagation delay time, TG going low	$tpdl_{BG}$	Cl = 3nF, V_{VS} = 4.6V, DRN <1V		7	**12**	ns
Under-Voltage Lockout						
V_5 ramping up	$tpdh_{UVLO}$	EN is High			**10**	µs
V_5 ramping down	$tpdh_{UVLO}$	EN is High			**10**	µs
PRDY						
EN is transitioning from low to high	tpdhPRDY	V_5 >UVLO threshold, Delay measured from EN > 2.0V to PRDY > 3.5V			**10**	µs
EN is transitioning fro high to low	tpdhUVLO	V_5 >UVLO threshold, Delay measured from EN < 0.8V to PRDY < 10% of V_5V			**500**	µs
DSPS_DR						
rise/fall time	$tr_{DSPS\ DR.}$	Cl = 100 pf, V_5 = 4.6V			**20**	ns
propagation delay, DSPS_DR going high	$tpdh_{DSPS\ DR}$	S_MOD goes high and BG goes high or S_MOD goes low			**10**	ns
propagation delay, DSPS_DR goes low	$tpdl_{DSPS\ DR}$	S_MOD goes high and BG goes low			**10**	ns

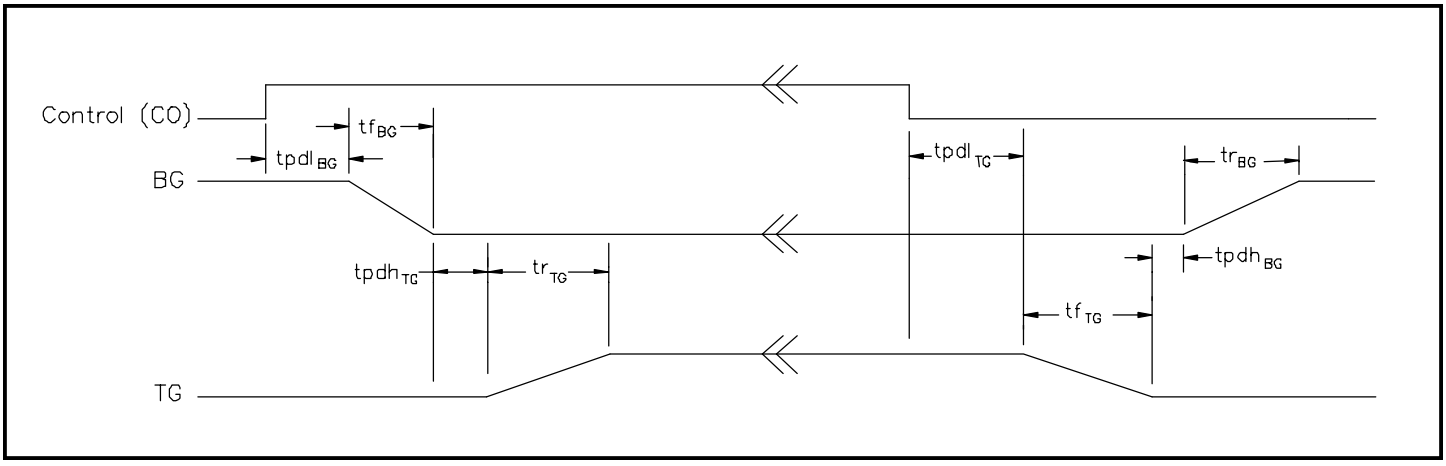
NOTE:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Application Circuit - TSSOP-14

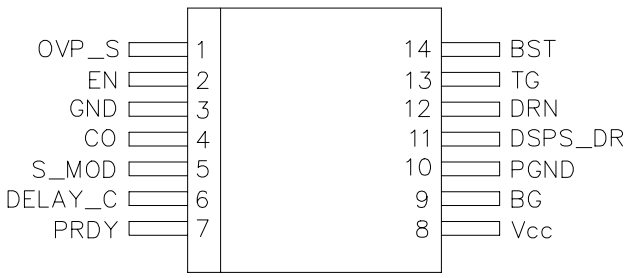


Timing Diagram



Pin Configuration

Top View



(14-Pin TSSOP)

Ordering Information

Device	Package	Temp Range (T_J)
SC1405DITSTRT	TSSOP-14	-40° to 125°C

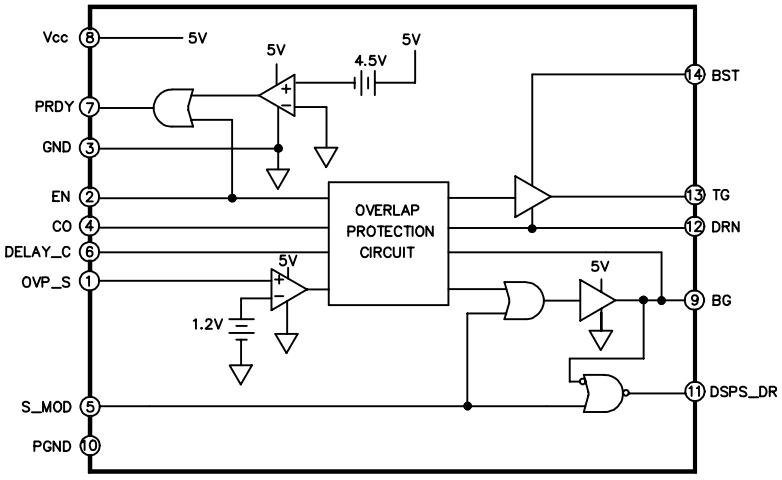
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	OVP_S	Overvoltage protection sense. External scaling resistors required to set protection threshold.
2	EN	When high, this pin enables the internal circuitry of the device. When low, TG, BG, and PRDY are forced low and the supply current (5V) is less than 10µA.
3	GND	Logic GND.
4	CO	TTL-level input signal to the MOSFET drivers.
5	S_MOD	When low, this signal forces BG to be low, triggering asynchronous operation. When high, BG is not a function of this signal.
6	DELAY_C	The capacitance connected between this pin and GND sets the additional propagation delay for BG going low to TG going high. Total propagation delay =20ns + 1ns/pF. If no capacitor is connected, the propragation delay = 20ns.
7	PRDY	This pin indicates the status of VCC. When VCC is less than the UVLO threshold, this output is driven low. When VCC is greater than or equals to the UVLO threshold this output goes high.
8	VCC	Input supply of 5 - 8V. A .22-1µF ceramic capacitor should be connected from VCC to PGND very close to the chip.
9	BG	Output drive for the synchrounous (bottom) MOSFET.
10	PGND	Power ground. Connect to the synchronous FET source pin (power ground).
11	DSPS_DR	Dynamic Set Point Switch Drive. TTL level output signal. When S-MOD is high, this pin follows the BG driver pin voltage.
12	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
13	TG	Output gate drive for the switching (high-side) MOSFET.
14	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).

NOTE:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Applications Information

SC1405D is designed to drive Low Rds_On power FETs with ultra-low rise/fall times and propagation delays. As the switching frequency of PWM controllers is increased to reduce power supply volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP FET) and reduce Dead-time (BOTTOM FET) losses. While Low Rds_On FETs present a power saving in I^2R losses, the FET's die area is larger and thus the effective input capacitance of the FET is increased. Often a 50% decrease in Rds_On more than doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a suboptimum driver. While discrete solution can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC1405 family of parts presents a total solution for the high-speed, high power density applications. Wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power servers as well as Class-D amplifiers.

Theory of Operation

The control input (CO) to the SC1405D is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic on page 12). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET's drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a condition which both the top and bottom FETs are on momentarily. The top FET is also prevented from turning on until the bottom FET is off. This time is internally set to 20ns (typical) and may be increased by adding a capacitor from the C-Delay pin to GND. The delay is approximately 1ns/pF in addition to the internal 20ns delay. The external capacitor may be needed if multiple High input capacitance FETs are used in parallel and the fall time is substantially greater than 20ns.

It must be noted that increasing the dead-time by high values of C-Delay capacitor will reduce efficiency since the parallel Schottky or the bottom FET's body diode will have to conduct during dead-time.

Layout Guidelines

As with any high speed , high current circuit, proper layout is critical in achieving optimum performance of the SC1405D. The Evaluation board schematic on page 12 shows a dual phase synchronous design with all surface mountable components.

While components connecting to C-Delay, OVP_S, EN,S-MOD, DSPS_DR and PRDY are relatively noncritical, tight

placement and short, wide traces must be used in layout of The Drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the +5V supply and adding it the phase node voltage (DRN). Since the bootstrap capacitor supplies the charge to the TOP gate, it must be less than 0.5" away from the SC1405. Ceramic X7R capacitors are a good choice for supply bypassing near the chip. The Vcc pin capacitor must also be less than 0.5" away from the SC1405. The ground node of this capacitor, the SC1405 PGND pin and the Source of the bottom FET must be very close to each other, preferably with common PCB copper land and multiple vias to the ground plane (if used). The parallel Schottky (if used) must be physically next to the Bottom FET's drain and source. Any trace or lead inductance in these connections will drive current way from the Schottky and allow it to flow through the FET's body diode, thus reducing efficiency.

Preventing Inadvertent Bottom FET Turn-on

At high input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, Crss of the bottom FET. The voltage appearing on the gate due to this spike is:

$$V_{spike} = \frac{V_{in} * C_{rss}}{C_{rss} + C_{iss}}$$

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors. (since dV/dT and thus the effective frequency is very high). If the BG pin of the SC1405D is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate if rise of current, etc.

While not shown in Application Evaluation Board Schematic on page 12, a capacitor may be added from the gate of the bottom FET to its source, preferably less than 0.5" away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage, Vspike.

The selection of the bottom FET must be done with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also FETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. The FET shown in the schematic has a 2 volt threshold and will require approximately 5 volts Vgs to be conducting, thus reducing the possibility of shoot-through. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low.

Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low.

Ringing on the Phase Node

The top FET source must be close to the bottom FET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

$$F_{ring} = \frac{1}{2\Pi\sqrt{L_{st} * C_{oss}}}$$

Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection.

Coss=Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to the value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. This ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss can often eliminate the EMI issue. If double pulsing is caused due to excessive ringing, placing 4.7-10 ohm resistor between the phase node and the DRN pin of the SC1405 should eliminate the double pulsing.

The negative voltage spikes on the phase node adds to the bootstrap capacitor voltage, thus increasing the voltage between VBST - VDRN. If the phase node negative spikes are too large, the voltage on the boost capacitor

Applications Information (Cont.)

could exceed device's absolute maximum rating of 8V. To eliminate the effect of the ringing on the boost capacitor voltage, place a 4.7 - 10 Ohm resistor between boost Schottky diode and Vcc to filter the negative spikes on DRN Pin. Alternately, a Silicon diode, such as the commonly available 1N4148 can substitute for the Schottky diode and eliminate the need for the series resistor.

Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of SO-8 or other surface mount FETs will reduce lead inductance and their parasitic effects.

ASYNCHRONOUS OPERATION

The SC1405D can be configured to operate in Asynchronous mode by pulling S-MOD to logic LOW, thus disabling the bottom FET drive. This has the effect of saving power at light loads since the bottom FET's gate capacitance does not have to charged at the switching frequency. There can be a significant savings since the bottom driver can supply up to 2A pulses to the FET at the switching frequency. There is an additional efficiency benefit to operating in asynchronous mode. When operating in synchronous mode, the inductor current can go negative and flow in reverse direction when the bottom FET is on and the DC load is less than 1/2 inductor ripple current. At that point, the inductor core and wire losses, depending on the magnitude of the ripple current, can be quite significant. Operating in asynchronous mode at light loads effectively only charges the inductor by as much as needed to supply the load current, since the inductor never completely discharges at light loads. DC regulation can be an issue when operating in asynchronous mode, depending on the type of controller used and minimum load required to maintain regulation. If there are no Shottkey diodes used in parallel with bottom FET, the FET's body diode will need to conduct in asynchronous mode. The high voltage drop of this diode must be considered when determining the criteria for this mode of operation.

DSPS DR

This pin produces an output which is a logical duplicate of the bottom FET's gate drive, if S-MOD is held High.

OVP_S/OVER TEMP SHUTDOWN

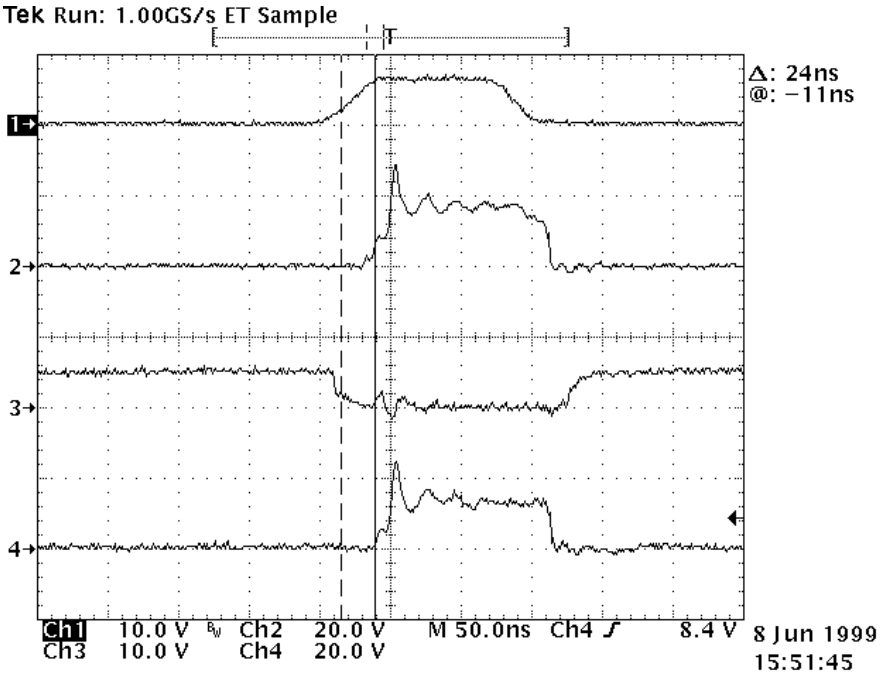
Output over-voltage protection (OVP) may be implemented on the SC1405D independent of the PWM controller . A voltage divider from the output is compared with the internal bandgap voltage of 1.2V (typical). Upon exceeding this voltage, the overvoltage comparator disables the top FET, while turning on the bottom FET to allow discharge of the output capacitors excessive voltage through the output inductor.

The SC1405D has a unique adaptive OVP circuit. Short noise pulses, less than ~100ns are rejected completely; longer pulses will trigger OVP if only of sufficient magnitude. A long term transient will trigger OVP with a smaller magnitude. To assure proper tripping, bypass the resistor from OVP_S pin to GND with a capacitor. The value of this capacitor must be selected to achieve a time constant equal to one switching period. Leave at least 250mV headroom on the OVP pin to prevent false OVP events.

The SC1405D will shutdown if its T_J exceeds 165°C.

Typical Characteristics

Performance diagrams, Application Evaluation Board.



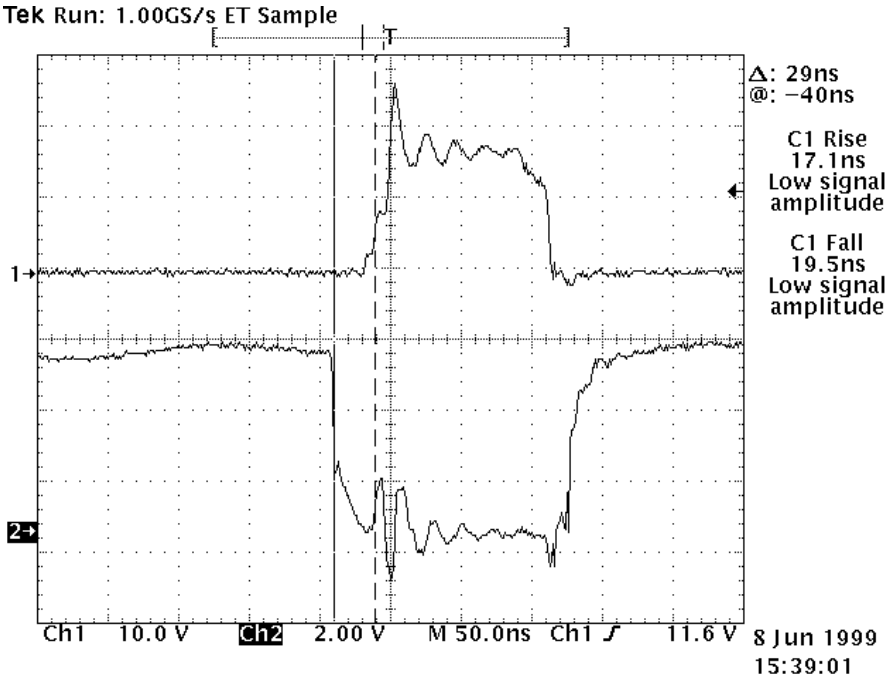
Timing diagram:

Ch1: CO input

Ch2: TG drive

Ch3: BG non-overlap drive

Ch4: phase node
Iout = 20A (10A/phase)
Refer to Eval. Schematic (fig.3)



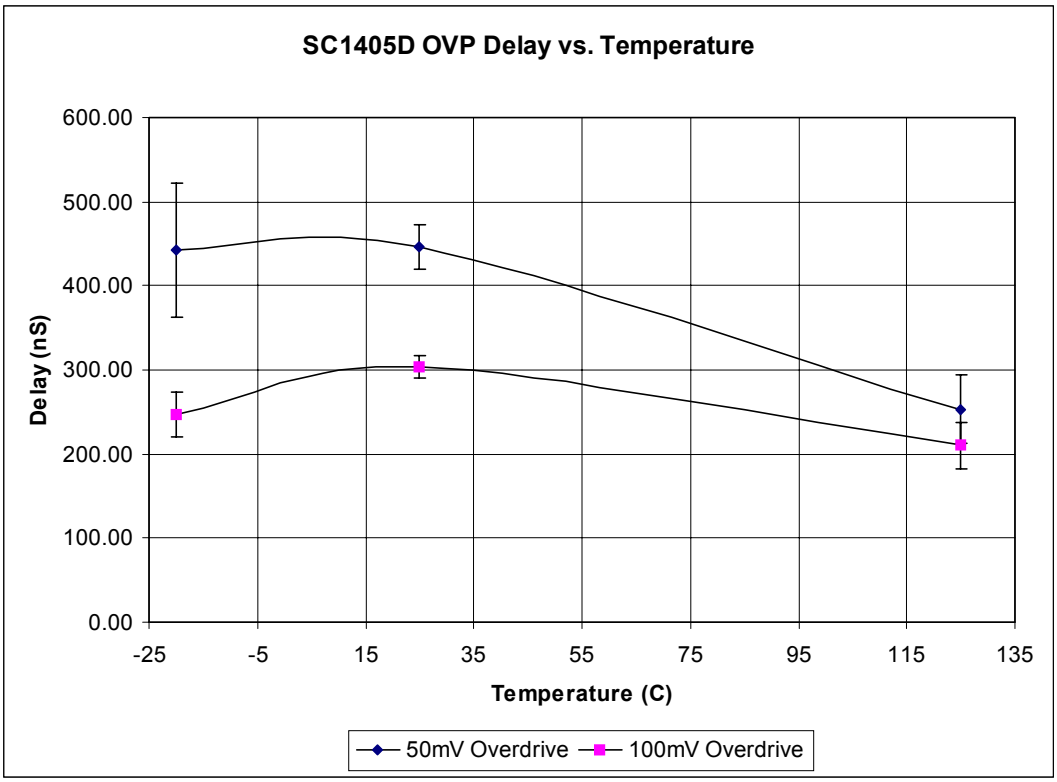
Timing diagram:
Rise/Fall times

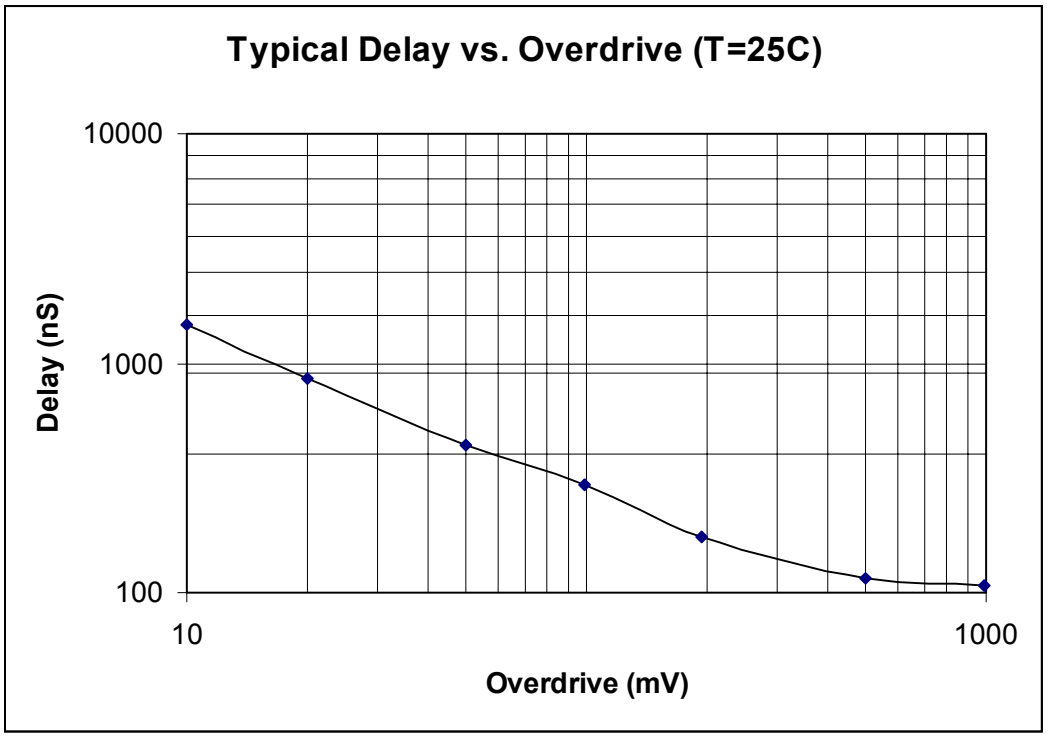
Ch1: TG drive

Ch2: BG drive
Cursor: $Tpdh_{TG}$
Iout = 20A (10A/phase)
Refer to Eval. Schematic (fig.3)

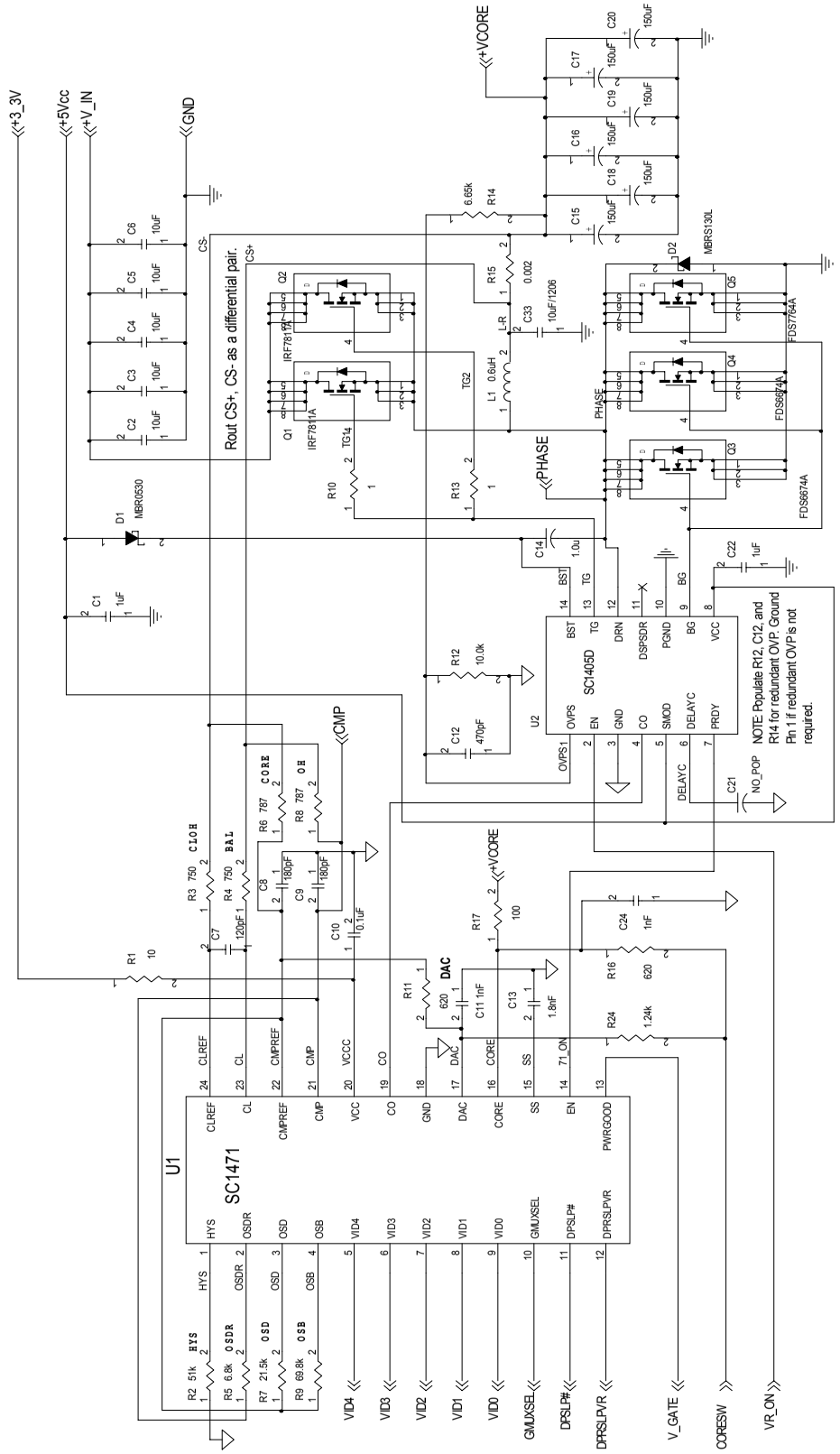
V_{IN} = 12V, V_{OUT} = 1.6V. Top FET = IR7811 FDB7030(BL) Qgd = 23nc

Typical Characteristics (Cont.)

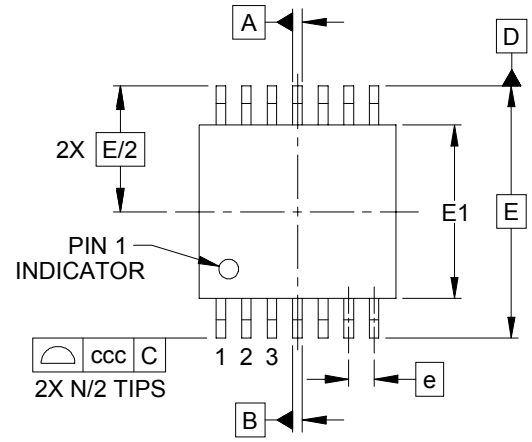




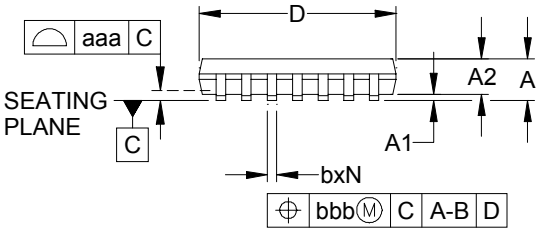
Evaluation Board Schematic

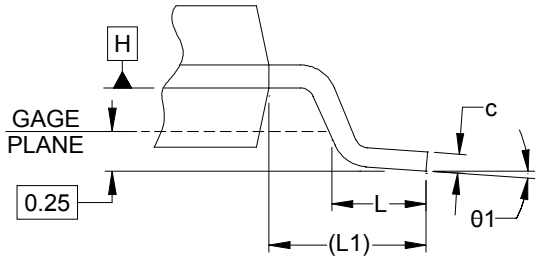


Outline Drawing -TSSOP-14

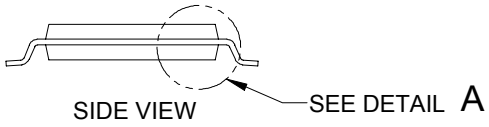


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.193	.197	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		





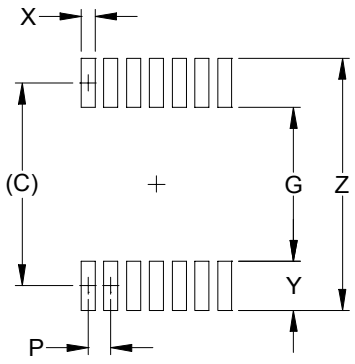
DETAIL A



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AB-1.

Land Pattern - TSSOP-14



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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