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SC16C2552

Dual UART with 16-byte transmit and receive FIFOs

Rev. 03 — 20 June 2003 **Product data**

1. Description

The SC16C2552 is a two channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 5 Mbits/s.

The SC16C2552 is pin compatible with the PC16C552 and ST16C2552. It will power-up to be functionally equivalent to the 16C2450. The SC16C2552 provides enhanced UART functions with 16 byte FIFOs, modem control interface, DMA mode data transfer and concurrent writes to control registers of both channels. The DMA mode data transfer is controlled by the FIFO trigger levels and the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loop-back capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC16C2552 operates at 5 V, 3.3 V and 2.5 V, and the Industrial temperature range, and is available in a plastic PLCC44 package.

2. Features

- Industrial temperature range (–40 °C to +85 °C)
- 5 V, 3.3 V and 2.5 V operation
- Pin-to-pin and functionally compatible to PC16C552, ST16C2552
- Software compatible with INS8250, NS16C550
- Up to 5 Mbits/s data rate at 5 V and 3 V, and 3 Mbits/s at 2.5 V
- 16-byte transmit FIFO
- 16-byte receive FIFO with error flags
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels; fixed XMIT FIFO interrupt trigger level
- Modem control signals ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, $\overline{\text{CD}}$)
- DMA operation and DMA monitoring via package I/O pins, $\overline{\text{TXRDY}}$/$\overline{\text{RXRDY}}$
- UART internal register sections A and B may be written to concurrently
- Multi-function output allows more package functions with fewer I/O pins
- Programmable character lengths (5, 6, 7, 8), with even, odd, or no parity

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SC16C2552IA44	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

4. Block diagram

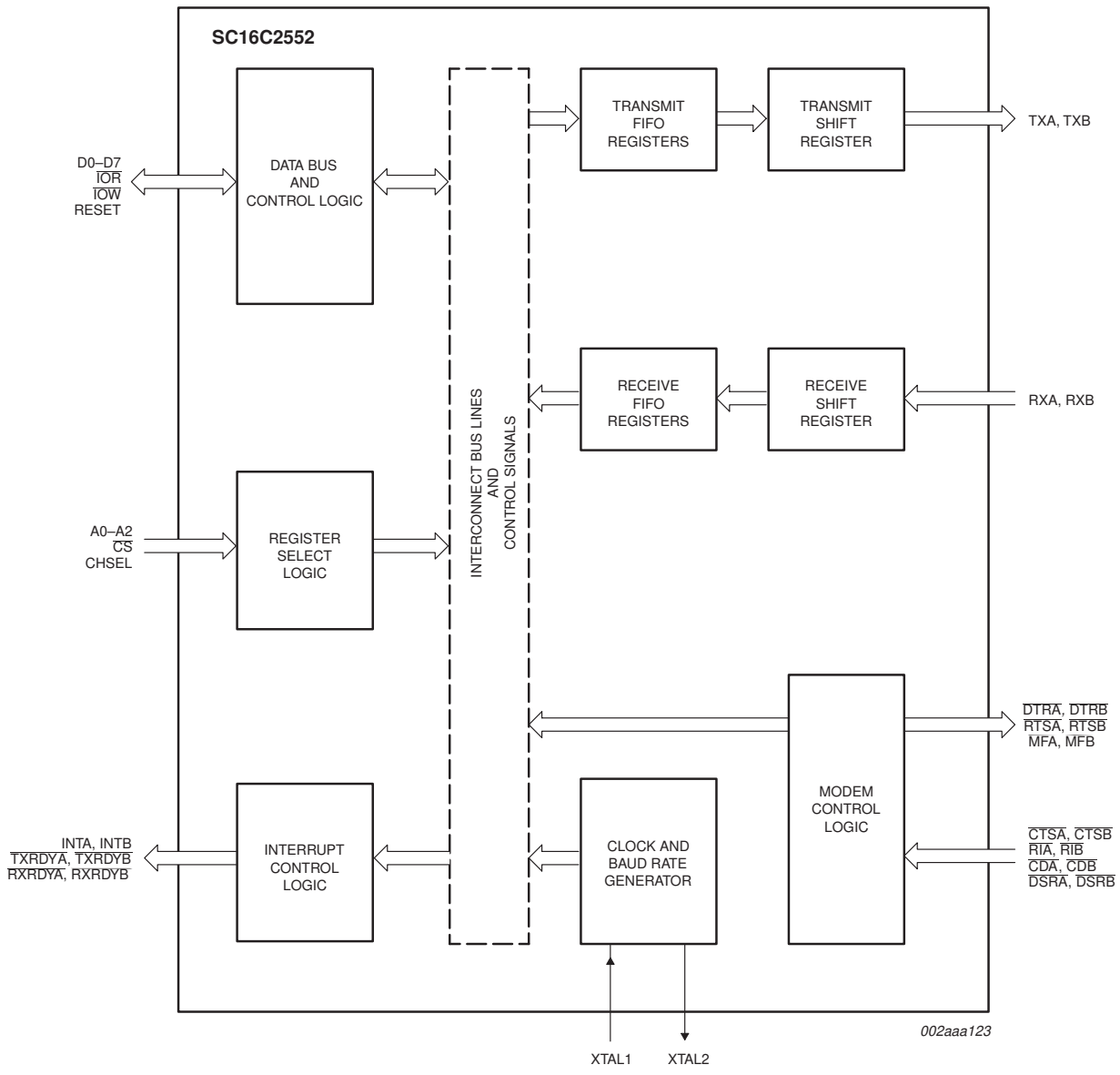

Fig 1. SC16C2552 block diagram.

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5. Pinning information

5.1 Pinning

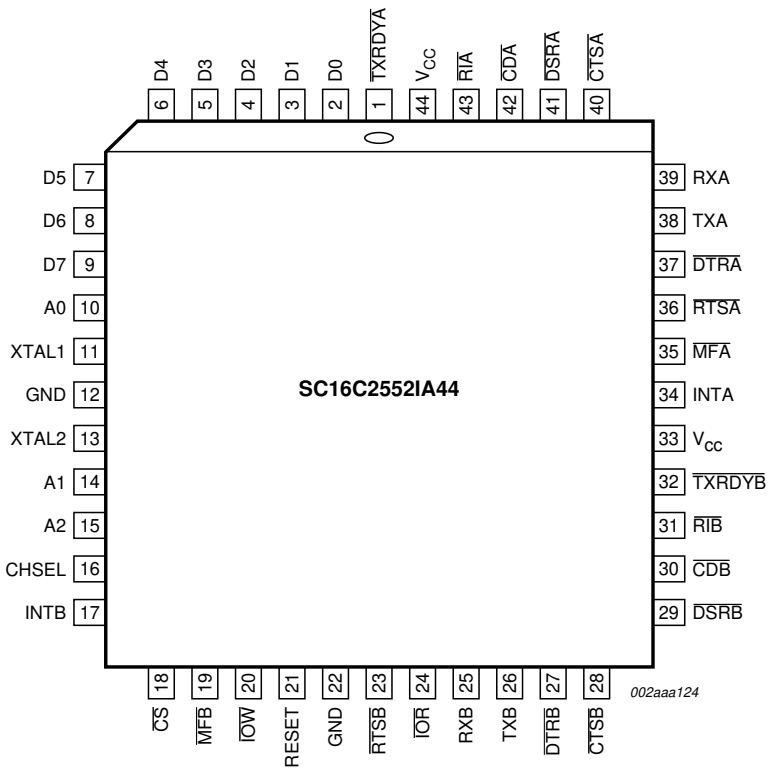

Fig 2. PLCC44 pin configuration.

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
A2-A0	10, 14, 15	I	**Register select.** A0-A2 are used during read and write operations to select the UART register to read from or write to.
CHSEL	16	I	**Channel Select.** UART channel A or B is selected by the logical state of this pin when the $\overline{CS}$ is a logic 0. A logic 0 on CHSEL selects the UART channel 'B', while a logic 1 selects UART channel 'A'.
$\overline{CS}$	18	I	**Chip Select (Active-LOW).** This function is selects channel 'A' or 'B', in accordance with the logical state of the CHSEL pin. This allows data to be transferred between the user CPU and the SC16C2552, or the SC16C2552 and the CPU for a channel selected by CHSEL. MF[0] overrides CHSEL while in the write cycle mode, allowing the user to write both channel registers simultaneously with one write cycle.
D0-D7	2-9	I/O	**Data bus (bi-directional).** These pins are the 8-bit, 3-State data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
GND	12, 22	I	**Signal and power ground.**

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Table 2: Pin description...*continued*

Symbol	Pin	Type	Description
INTA, INTB	34, 17	O	**Interrupt A, B (Active-HIGH).** This function is associated with individual channel interrupts, INTA, INTB. INTA, INTB are enabled when MCR bit 3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
$\overline{IOR}$	24	I	**Read strobe (Active-LOW).** A logic 0 transition on this pin will load the contents of an internal register defined by address bits A0-A2 onto the SC16C2552 data bus (D0-D7) for access by external CPU.
$\overline{IOW}$	20	I	**Write strobe (Active-LOW).** A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2.
$\overline{MFA}$, $\overline{MFB}$	35, 19	O	**Multi-Function A, B.** This function is associated with an individual channel function, 'A' or 'B'. User programmable bits 1-2 of the Alternate Function Register (AFR), selects a signal function or output on these pins. $\overline{OP2}$ (interrupt enable), $\overline{BAUDOUT}$, and $\overline{RXRDY}$ are signal functions that may be selected by the AFR. These signal functions are described as follows: **$\overline{OP2}$.** When $\overline{OP2}$ (interrupt output enable function) is selected, the MF pin is a logic 1 when INTA, INTB is set to the 3-State mode (disabled), or a logic 0 when INTA, INTB is enabled. (See MCR[3].) A logic 1 is the default signal condition that is available following a master reset or power-up. **$\overline{BAUDOUT}$.** When $\overline{BAUDOUT}$ function is selected, the 16× baud rate clock output is available at this pin. **$\overline{RXRDY}$.** $\overline{RXRDY}$ is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFOs. A logic 0 indicates there is receive data to read/unload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).
RESET	21	I	**Reset (Active-HIGH).** A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See Section 7.11 "SC16C2552 external reset conditions" for initialization details.)
$\overline{TXRDYA}$, $\overline{TXRDYB}$	1, 32	O	**Transmit Ready A, B (Active-LOW).** These outputs provide the TX FIFO/THR status for individual transmit channels (A-B). $\overline{TXRDY}$n is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{TXRDYA}$, $\overline{TXRDYB}$ buffer ready status is indicated by logic 0, i.e., at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
V_{CC}	33, 44	I	**Power supply input.**
XTAL1	11	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates. (See Section 6.5 "Programmable baud rate generator".)
XTAL2	13	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1.
$\overline{CDA}$, $\overline{CDB}$	42, 30	I	**Carrier Detect (Active-LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.

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Table 2: Pin description...*continued*

Symbol	Pin	Type	Description
$\overline{CTSA}$, $\overline{CTSB}$	40, 28	I	**Clear to Send (Active-LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{CTS}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C2552. Status can be tested by reading MSR[4].
$\overline{DSRA}$, $\overline{DSRB}$	41, 29	I	**Data Set Ready (Active-LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART.
$\overline{DTRA}$, $\overline{DTRB}$	37, 27	O	**Data Terminal Ready (Active-LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the SC16C2552 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTR}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset.
$\overline{RIA}$, $\overline{RIB}$	43, 31	I	**Ring Indicator (Active-LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
$\overline{RTSA}$, $\overline{RTSB}$	36, 23	O	**Request to Send (Active-LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{RTS}$ pin indicates the receiver is ready to receive data. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating that the receiver is ready to receive data. After a reset this pin will be set to a logic 1.
RXA, RXB	39, 25	I	**Receive data A, B.** These inputs are associated with individual serial channel data to the SC16C2552 receive input circuits, A-B. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is connected to the UART RX input, internally.
TXA, TXB	38, 26	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC16C2552. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.

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6. Functional description

The SC16C2552 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C2552 is fabricated with an advanced CMOS process.

The SC16C2552 is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory, instead of none in the 16C450. The SC16C2552 is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C2552 by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable receive FIFO trigger interrupt levels are uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C2552 is capable of operation to 1.5 Mbits/s with a 24 MHz. With a crystal or external clock input of 7.3728 MHz, the user can select data rates up to 460.8 kbits/s.

The rich feature set of the SC16C2552 is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls are all standard features.

6.1 UART A-B functions

The UART provides the user with the capability to bi-directionally transfer information between an external CPU, the SC16C2552 package, and an external serial device. A logic 0 on chip select pin $\overline{CS}$, and a logic 1 on CHSEL allows the user to configure, send data, and/or receive data via UART channel A. A logic 0 on chip select pin $\overline{CS}$ and a logic 0 on CHSEL allows the user to configure, send data, and/or receive data via UART channel B. Individual channel select functions are shown in Table 3.

Table 3: Serial port selection

Chip Select	Function
$\overline{CS}$ = 1	none
$\overline{CS}$ = 0	UART channel selected as follows: CHSEL = 1: UART Channel A CHSEL = 0: UART Channel B

During a write mode cycle, the setting of AFR[0] to a logic 1 will override the CHSEL selection and allow a simultaneous write to both UART channel sections. This functional capability allow the registers in both UART channels to be modified concurrently, saving individual channel initialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode.

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6.2 Internal registers

The SC16C2552 provides two sets of internal registers (A and B) consisting of 12 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), a user accessible scratchpad register (SPR), and an Alternate Function Register (AFR).

Table 4: Internal registers decoding

A2	A1	A0	READ mode	WRITE mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Register set 2 (DLL/DLM/AFR)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

[1] The General Register sets are accessible only when $\overline{CS}$ is a logic 0 and LCR[7] is a logic 0.

[2] The Baud Rate register and AFR register sets are accessible only when $\overline{CS}$ is a logic 0 and LCR[7] is a logic 1 for the register set (A/B) being accessed.

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6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. The user can set the receive trigger level via FCR bits 6-7, but not the transmit trigger level. The transmit interrupt trigger level is set to 16 following a reset. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

6.4 Time-out interrupts

The interrupts are enabled by IER[0-3]. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the SC16C2552 will issue an interrupt to indicate that Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C2552 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

6.5 Programmable baud rate generator

The SC16C2552 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A baud rate generator is provided for each UART channel, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 80 MHz, as required for supporting a 5 Mbits/s data rate. The SC16C2552 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 5).

The generator divides the input 16× clock by any divisor from 1 to $2^{16} - 1$. The SC16C2552 divides the basic external clock by 16. The basic 16× clock provides table rates to support standard and custom applications using the same system

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design. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

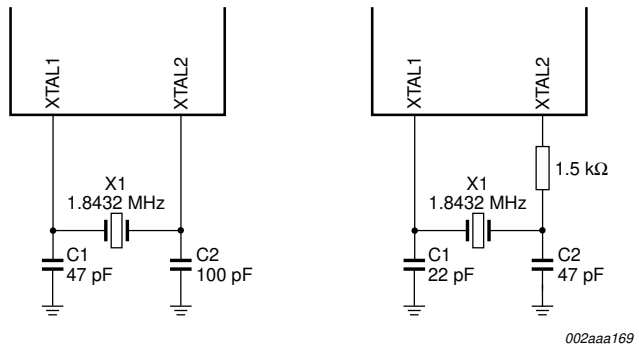

Fig 3. Crystal oscillator connection.

Table 5: Baud rate generator programming table using a 1.8432 MHz clock

Output baud rate	Output 16× clock divisor (decimal)	User 16× clock divisor (HEX)	DLM program value (HEX)	DLL program value (HEX)
50	2304	900	09	00
75	1536	600	06	00
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

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6.6 DMA operation

The SC16C2552 FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[5,6] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C2552 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the SC16C2552 sets the interrupt output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFOs are above the receive trigger level.

6.7 Loop-back mode

The internal loop-back capability allows on-board diagnostics. In the loop-back mode, the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR[0-3] register bits are used for controlling loop-back diagnostic testing. In the loop-back mode, INT enable and MCR[2] in the MCR register (bits 2-3) control the modem $\overline{RI}$ and $\overline{CD}$ inputs, respectively. MCR signals $\overline{DTR}$ and $\overline{RTS}$ (bits 0-1) are used to control the modem $\overline{CTS}$ and $\overline{DSR}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 4). The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control inputs pins, and instead are connected internally to $\overline{DTR}$, $\overline{RTS}$, INT enable, and MCR[2]. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[0-3]) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

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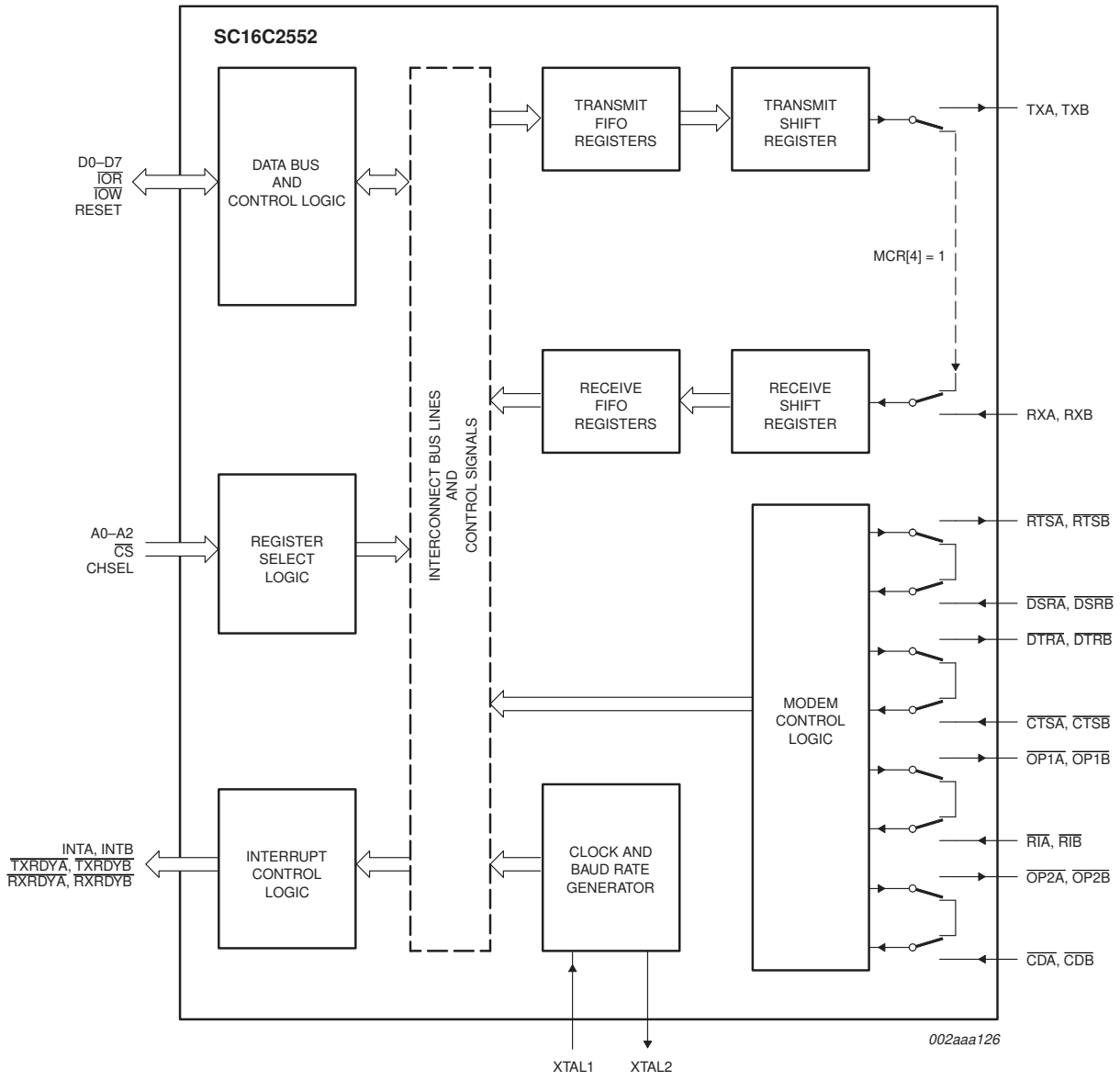

Fig 4. Internal loop-back mode diagram.

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7. Register descriptions

Table 6 details the assigned bit functions for the SC16C2552 internal registers. The assigned bit functions are further defined in Section 7.1 through Section 7.11.

Table 6: SC16C2552 internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General Register Set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	0	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	0	loop back	$\overline{OP}$ A/B, INT A/B enable	$\overline{OP1}$	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special Register Set[3]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0	1	0	AFR	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

[1] The value shown in represents the register's initialized HEX value; X = n/a.

[2] The General Register sets are accessible only when CS is a logic 0 and LCR[7] is a logic 0. Set A is accessible when CHSEL is a logic 1, and set is accessible when CHSEL is a logic 0.

[3] The Baud Rate register and AFR register sets are accessible only when CS is a logic 0 and LCR[7] is a logic 1 for the register set (A/B) being accessed.

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7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16C2552 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After 7-$\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA, INTB output pins.

Table 7: Interrupt Enable Register bits description

Bit	Symbol	Description
7-4	IER[7-4]	Not used; initialized to logic 0.
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[0-3]. Logic 0 = Disable the modem status register interrupt (normal default condition). Logic 1 = Enable the modem status register interrupt.
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[1-4]. Logic 0 = Disable the receiver line status interrupt (normal default condition). Logic 1 = Enable the receiver line status interrupt.
1	IER[1]	Transmit Holding Register interrupt. In the 16C450 mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO and THR are empty. Logic 0 = Disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition). Logic 1 = Enable the TXRDY (ISR level 3) interrupt.

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Table 7: Interrupt Enable Register bits description...*continued*

Bit	Symbol	Description
0	IER[0]	Receive Holding Register. In the 16C450 mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. Logic 0 = Disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition). Logic 1 = Enable the RXRDY (ISR level 2) interrupt.

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register, or by loading the THR with new data characters.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[0-3] enables the SC16C2552 in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[1-4] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

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7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

Mode 0 (FCR bit 3 = 0): Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) at the MF pin will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character and the MF register is set to the RXRDY mode.

Mode 1 (FCR bit 3 = 1): Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO has at least one empty location. $\overline{\text{TXRDY}}$ remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ at the MF pin remains a logic 0 as long as the FIFO fill level is above the programmed trigger level, and the MF register is set to the RXRDY mode.

7.3.2 FIFO mode

Table 8: FIFO Control Register bits description

Bit	Symbol	Description
7-6	FCR[7] (MSB), FCR[6] (LSB)	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 9.
5-4	FCR[5-4]	Not used; initialized to logic 0.
3	FCR[3]	DMA mode select. Logic 0 = Set DMA mode ‘0’ (normal default condition). Logic 1 = Set DMA mode ‘1’ **Transmit operation in mode ‘0’:** When the SC16C2552 is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode ‘0’:** When the SC16C2552 is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ signal at the MF pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ signal at the MF pin will go to a logic 1 when there are no more characters in the receiver. NOTE: The AFR register must be set to the RXRDY mode prior to any possible reading of the $\overline{\text{RXRDY}}$ signal.

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Table 8: FIFO Control Register bits description...*continued*

Bit	Symbol	Description
3 (continued)		**Transmit operation in mode '1':** When the SC16C2552 is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty. **Receive operation in mode '1':** When the SC16C2552 is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDY}}$ signal at the MF pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO. NOTE: The AFR register must be set to the RXRDY mode prior to any possible reading of the $\overline{\text{RXRDY}}$ signal.
2	FCR[2]	XMIT FIFO reset. Logic 0 = No FIFO transmit reset (normal default condition). Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. Logic 0 = No FIFO receive reset (normal default condition). Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFOs enabled. Logic 0 = Disable the transmit and receive FIFO (normal default condition). Logic 1 = Enable the transmit and receive FIFO. **This bit must be a '1' when other FCR bits are written to, or they will not be programmed.**

Table 9: RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

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7.4 Interrupt Status Register (ISR)

The SC16C2552 provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 10 “Interrupt source” shows the data values (bits 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 10: Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 11: Interrupt Status Register bits description

Bit	Symbol	Description
7-6	ISR[7-6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the 16C450 mode. They are set to a logic 1 when the FIFOs are enabled in the SC16C2552 mode. Logic 0 or cleared = default condition.
5-4	ISR[5-4]	Not used; initialized to a logic 0. Logic 0 or cleared = default condition.
3-1	ISR[3-1]	INT priority bits 2-0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 10). Logic 0 or cleared = default condition.
0	ISR[0]	INT status. Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine. Logic 1 = No interrupt pending (normal default condition).

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7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 12: Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhance Feature mode enable. Logic 0 = Divisor latch disabled (normal default condition). Logic 1 = Divisor latch enabled.
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. Logic 0 = no TX break condition (normal default condition) Logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.
5-3	LCR[5-3]	Programs the parity conditions (see Table 13).
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 14). Logic 0 or cleared = default condition.
1-0	LCR[1-0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 15). Logic 0 or cleared = default condition.

Table 13: LCR[5] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
X	0	1	ODD parity
0	1	1	EVEN parity
0	0	1	force parity ‘1’
1	1	1	forced parity ‘0’

Table 14: LCR[2] stop bit length

LCR[2]	Word length	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	1-½
1	6, 7, 8	2

Table 15: LCR[1-0] word length

LCR[1]	LCR[0]	Word length
0	0	5
0	1	6
1	0	7
1	1	8

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7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 16: Modem Control Register bits description

Bit	Symbol	Description
7-5	MCR[7-5]	Not used; initialized to a logic 0.
4	MCR[4]	Loop-back. Enable the local loop-back mode (diagnostics). In this mode the transmitter output TX and the receiver input RX, $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from the SC16C2552 I/O pins. Internally the modem data and control pins are connected into a loop-back data configuration (see Figure 4). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. Logic 0 = Disable loop-back mode (normal default condition). Logic 1 = Enable local loop-back mode (diagnostics).
3	MCR[3]	$\overline{OP2}$, INTA/INTB enable. Used to control the modem $\overline{CD}$ signal in the loop-back mode. Logic 0 = Forces INT (A-B) outputs to the 3-State mode and sets $\overline{OP2}$ to a logic 1 (normal default condition). In the loop-back mode, sets $\overline{CD}$ internally to a logic 1. Logic 1 = Forces the INT (A-B outputs to the active mode and sets $\overline{OP2}$ to a logic 0. In the loop-back mode, sets $\overline{CD}$ internally to a logic 0.
2	MCR[2]	$\overline{OP1}$. This bit is used in the Loop-back mode only. In the loop-back mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal.
1	MCR[1]	$\overline{RTS}$ Logic 0 = Force $\overline{RTS}$ output to a logic 1 (normal default condition). Logic 1 = Force $\overline{RTS}$ output to a logic 0.
0	MCR[0]	$\overline{DTR}$ Logic 0 = Force $\overline{DTR}$ output to a logic 1 (normal default condition). Logic 1 = Force $\overline{DTR}$ output to a logic 0.

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7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C2552 and the CPU.

Table 17: Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. Logic 0 = No error (normal default condition). Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to '1' whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. Logic 0 = No break condition (normal default condition). Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. Logic 0 = No framing error (normal default condition). Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. Logic 0 = No parity error (normal default condition). Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. Logic 0 = No overrun error (normal default condition). Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

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Table 17: Line Status Register bits description...*continued*

Bit	Symbol	Description
0	LSR[0]	Receive data ready. Logic 0 = No data in receive holding register or FIFO (normal default condition). Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C2552 is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 18: Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	Carrier Detect, CD. During normal operation, this bit is the complement of the $\overline{CD}$ input. Reading this bit in the loop-back mode produces the state of MCR[3] ($\overline{OPA}$/OPB).
6	MSR[6]	Ring Indicator, RI. During normal operation, this bit is the complement of the $\overline{RI}$ input. Reading this bit in the loop-back mode produces the state of MCR[2] ($\overline{OP1}$).
5	MSR[5]	Data Set Ready, DSR. During normal operation, this bit is the complement of the $\overline{DSR}$ input. During the loop-back mode, this bit is equivalent to MCR[0] ($\overline{DTR}$).
4	MSR[4]	Clear To Send, CTS. During normal operation, this bit is the complement of the $\overline{CTS}$ input. During the loop-back mode, this bit is equivalent to MCR[1] ($\overline{RTS}$).
3	MSR[3]	$\Delta\overline{CD}$ [1] Logic 0 = No $\overline{CD}$ change (normal default condition). Logic 1 = The $\overline{CD}$ input to the SC16C2552 has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] Logic 0 = No $\overline{RI}$ change (normal default condition). Logic 1 = The $\overline{RI}$ input to the SC16C2552 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] Logic 0 = No $\overline{DSR}$ change (normal default condition). Logic 1 = The $\overline{DSR}$ input to the SC16C2552 has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] Logic 0 = No $\overline{CTS}$ change (normal default condition). Logic 1 = The $\overline{CTS}$ input to the SC16C2552 has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR bit 0-3 is set to logic 1, a Modem Status Interrupt will be generated.

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7.9 Scratchpad Register (SPR)

The SC16C2552 provides a temporary data register to store 8 bits of user information.

7.10 Alternate Function Register (AFR)

This is a read/write register used to select specific modes of $\overline{MF}$ operation and to allow both UART register's sets to be written concurrently.

Table 19: Alternate Function Register bits description

Bit	Symbol	Description
7-3	AFR[7-3]	Not used. All are initialized to logic 0.
2-1	AFR[2-1]	Selects a signal function for output on the $\overline{MFA}$, $\overline{MFB}$ pins. These signal functions are described as: $\overline{OP2}$ (interrupt enable), $\overline{BAUDOUT}$, or $\overline{TXRDY}$. Only one signal function can be selected at a time. See Table 20.
0	AFR[0]	When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. The external CPU can set or clear this bit by accessing either register set. When this bit is set, the Channel Select pin still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations. The user should ensure that LCR[7] of both channels are in the same state before executing a concurrent write to the registers at address 0, 1, or 2. Logic 0 = No concurrent write (normal default condition). Logic 1 = Register set A and B are written concurrently with a single external CPU I/O write operation.

Table 20: $\overline{MFA}$, $\overline{MFB}$ function selection

AFR[2]	AFR[1]	MF function
0	0	$\overline{OP2}$
0	1	$\overline{BAUDOUT}$
1	0	$\overline{RXRDY}$
1	1	reserved

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7.11 SC16C2552 external reset conditions

Table 21: Reset state for registers

Register	Reset state
IER	IER[7-0] = 0
ISR	ISR[7-1] = 0; ISR[0] = 1
LCR	LCR[7-0] = 0
MCR	MCR[7-0] = 0
LSR	LSR[7] = 0; LSR[6-5] = 1; LSR[4-0] = 0
MSR	MSR[7-4] = input signals; MSR[3-0] = 0
FCR	FCR[7-0] = 0
AFR	AFR[7-0] = 0

Table 22: Reset state for outputs

Output	Reset state
TXA, TXB	HIGH
$\overline{OP2A}$, $\overline{OP2B}$	HIGH
$\overline{RTSA}$, $\overline{RTSB}$	HIGH
$\overline{DTRA}$, $\overline{DTRB}$	HIGH
INTA, INTB	LOW
$\overline{TXRDYA}$, $\overline{TXRDYB}$	LOW

8. Limiting values

Table 23: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage at any pin		GND – 0.3	V_{CC} + 0.3	V
T_{amb}	operating temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
$P_{tot(pack)}$	total power dissipation per package		-	500	mW

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9. Static characteristics

Table 24: DC electrical characteristics

T_{amb} = −40 °C to +85 °C; V_{CC} = 2.5 V, 3.3 V or 5.0 V ±10%, unless otherwise specified.

Symbol	Parameter	Conditions	2.5 V		3.3 V		5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
$V_{IL(CK)}$	LOW-level clock input voltage		−0.3	0.45	−0.3	0.6	−0.5	0.6	V
$V_{IH(CK)}$	HIGH-level clock input voltage		1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage (except X1 clock)		−0.3	0.65	−0.3	0.8	−0.5	0.8	V
V_{IH}	HIGH-level input voltage (except X1 clock)		1.6	-	2.0	-	2.2	-	V
V_{OL}	LOW-level output voltage on all outputs[1]	I_{OL} = 5 mA (databus)	-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)	-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (databus)	-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)	-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −5 mA (databus)	-	-	-	-	2.4	-	V
		I_{OH} = −1 mA (other outputs)	-	-	2.0	-	-	-	V
		I_{OH} = −800 µA (data bus)	1.85	-	-	-	-	-	V
		I_{OH} = −400 µA (other outputs)	1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current		-	±10	-	±10	-	±10	µA
I_{CL}	clock leakage		-	±30	-	±30	-	±30	µA
I_{CC}	supply current	f = 5 MHz	-	3.5	-	4.5	-	4.5	mA
C_i	input capacitance		-	5	-	5	-	5	pF

[1] Except x_2, V_{OL} = 1 V typical.

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10. Dynamic characteristics

Table 25: AC electrical characteristics

T_{amb} = −40 °C to +85 °C; V_{CC} = 2.5 V, 3.3 V or 5.0 V ±10%, unless otherwise specified.

Symbol	Parameter	Conditions	2.5 V		3.3 V		5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
t_{1w}, t_{2w}	clock pulse duration		10	-	6	-	6	-	ns
t_{3w}	oscillator/clock frequency	[1]	-	48	-	80		80	MHz
t_{6s}	address set-up time		0	-	0	-	0	-	ns
t_{6h}	address hold time		0	-	0	-	0	-	ns
t_{7d}	$\overline{IOR}$ delay from chip select		10	-	10	-	10	-	ns
t_{7w}	$\overline{IOR}$ strobe width	25 pF load	77	-	26	-	23	-	ns
t_{7h}	chip select hold time from $\overline{IOR}$		0	-	0	-	0	-	ns
t_{9d}	read cycle delay	25 pF load	20	-	20	-	20	-	ns
t_{12d}	delay from $\overline{IOR}$ to data	25 pF load	-	77	-	26	-	23	ns
t_{12h}	data disable time	25 pF load	-	15	-	15	-	15	ns
t_{13d}	$\overline{IOW}$ delay from chip select		10	-	10	-	10	-	ns
t_{13w}	$\overline{IOW}$ strobe width		20	-[2]	20	-[2]	15	-[2]	ns
t_{13h}	chip select hold time from $\overline{IOW}$		0	-	0	-	0	-	ns
t_{15d}	write cycle delay	[3]	25	-	25	-	20	-	ns
t_{16s}	data set-up time		20	-	20	-	15	-	ns
t_{16h}	data hold time		15	-	5	-	5	-	ns
t_{17d}	delay from $\overline{IOW}$ to output	25 pF load	-	100	-	33	-	29	ns
t_{18d}	delay to set interrupt from Modem input	25 pF load	-	100	-	24	-	23	ns
t_{19d}	delay to reset interrupt from $\overline{IOR}$	25 pF load	-	100	-	24	-	23	ns
t_{20d}	delay from stop to set interrupt		-	1	-	1	-	1	R_{clk}
t_{21d}	delay from $\overline{IOR}$ to reset interrupt	25 pF load	-	100	-	29	-	28	ns
t_{22d}	delay from start to set interrupt		-	100	-	45	-	40	ns
t_{23d}	delay from $\overline{IOW}$ to transmit start		8	24	8	24	8	24	R_{clk}
t_{24d}	delay from $\overline{IOW}$ to reset interrupt		-	100	-	45	-	40	ns
t_{25d}	delay from stop to set $\overline{RXRDY}$		-	1	-	1	-	1	R_{clk}
t_{26d}	delay from $\overline{IOR}$ to reset $\overline{RXRDY}$		-	100	-	45	-	40	ns
t_{27d}	delay from $\overline{IOW}$ to set $\overline{TXRDY}$		-	100	-	45	-	40	ns
t_{28d}	delay from start to reset $\overline{TXRDY}$		-	8	-	8	-	8	R_{clk}
t_{RESET}	Reset pulse width		200	-	40	-	40	-	ns
N	baud rate divisor		1	$2^{16} - 1$	1	$2^{16} - 1$	1	$2^{16} - 1$	R_{clk}

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] $$\overline{IOW}\,\text{strobe}_{max} = \frac{1}{2(\text{Baudrate}_{max})}$$

= 333 ns (for $Baudrate_{max}$ = 1.5 Mbits/s)

= 1 µs (for $Baudrate_{max}$ = 460.8 kbits/s)

= 4 µs (for $Baudrate_{max}$ = 115.2 kbits/s)

[3] When in **both** DMA mode 0 **and** FIFO enable mode, the write cycle delay should be larger than one x_1, clock cycle.

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