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SC16C550B

5 V, 3.3 V and 2.5 V UART with 16-byte FIFOs

Rev. 6 — 16 December 2014 Product data sheet

1. General description

The SC16C550B is a Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 3 Mbit/s.

The SC16C550B is pin compatible with the ST16C550, TL16C550 and PC16C550, and it will power-up to be functionally equivalent to the 16C450. The SC16C550B also provides DMA mode data transfers through FIFO trigger levels and the $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ are not supported in the HVQFN32 package). On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C550B operates at 5 V, 3.3 V and 2.5 V, and the Industrial temperature range, and is available in plastic HVQFN32, DIP40, PLCC44 and LQFP48 packages.

2. Features and benefits

- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range
- After reset, all registers are identical to the typical 16C450 register set
- Capable of running with all existing generic 16C450 software
- Pin compatibility with the industry-standard ST16C450/550, TL16C450/550, PC16C450/550
- Up to 3 Mbit/s transmit/receive operation at 5 V, 2 Mbit/s at 3.3 V, and 1 Mbit/s at 2.5 V
- 5 V tolerant on input only pins[1]
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Programmable auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$
  - In auto-$\overline{\text{CTS}}$ mode, $\overline{\text{CTS}}$ controls transmitter
  - In auto-$\overline{\text{RTS}}$ mode, RX FIFO contents and threshold control $\overline{\text{RTS}}$
- Automatic hardware flow control
- Software selectable baud rate generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Independent receiver clock input
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled

1. For data bus pins D7 to D0, see Table 24 “Limiting values”.

- Fully programmable character formatting:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (up to 3 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RI}$, $\overline{DCD}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$)

3. Ordering information

Table 1. Ordering information

Industrial: V_{DD} = 2.5 V, 3.3 V or 5 V ± 10 %; T_{amb} = −40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
SC16C550BIA44	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
SC16C550BIBS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1
SC16C550BIB48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
SC16C550BIN40	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1

4. Block diagram

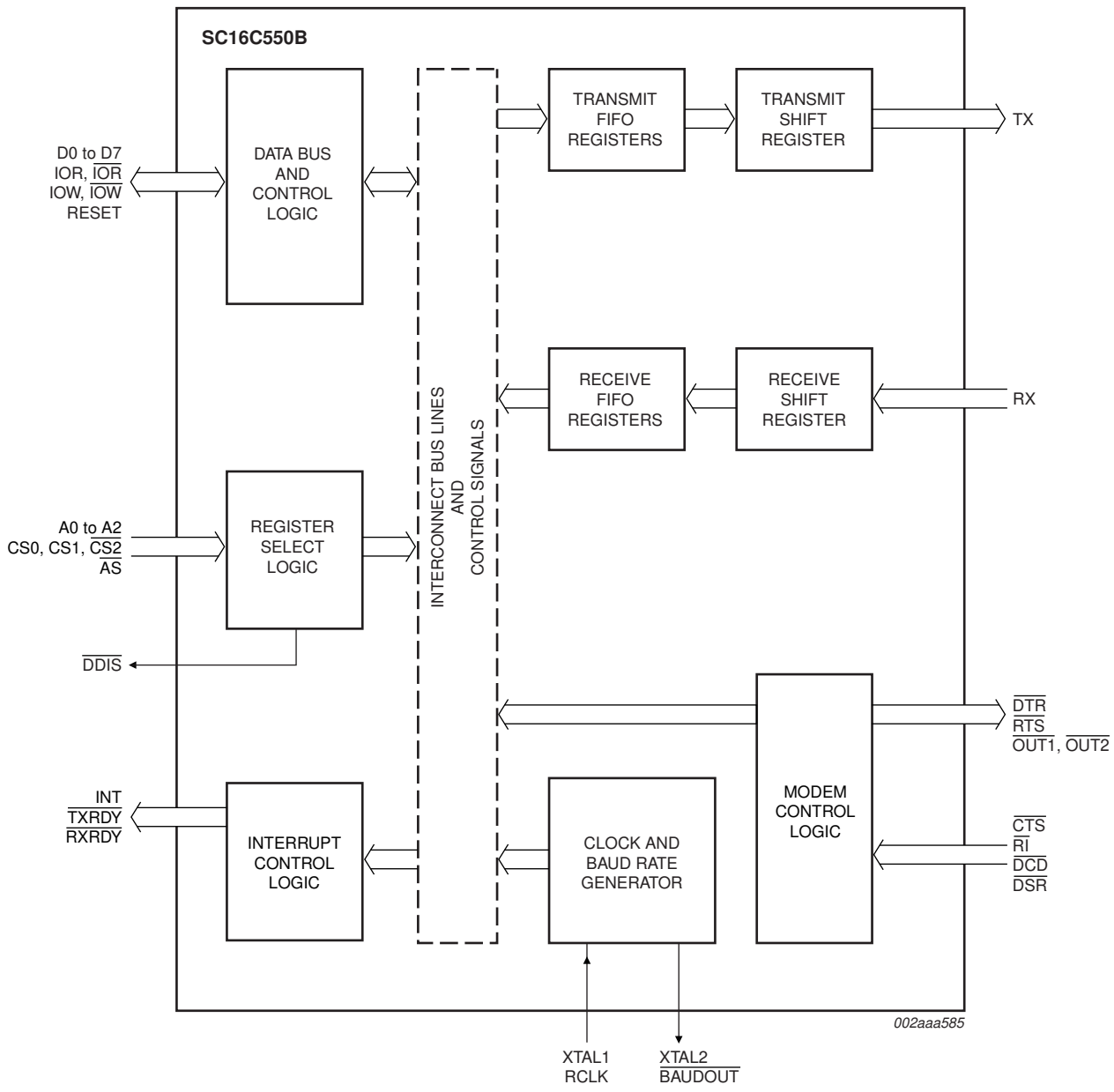


Fig 1. Block diagram of SC16C550B

5. Pinning information

5.1 Pinning

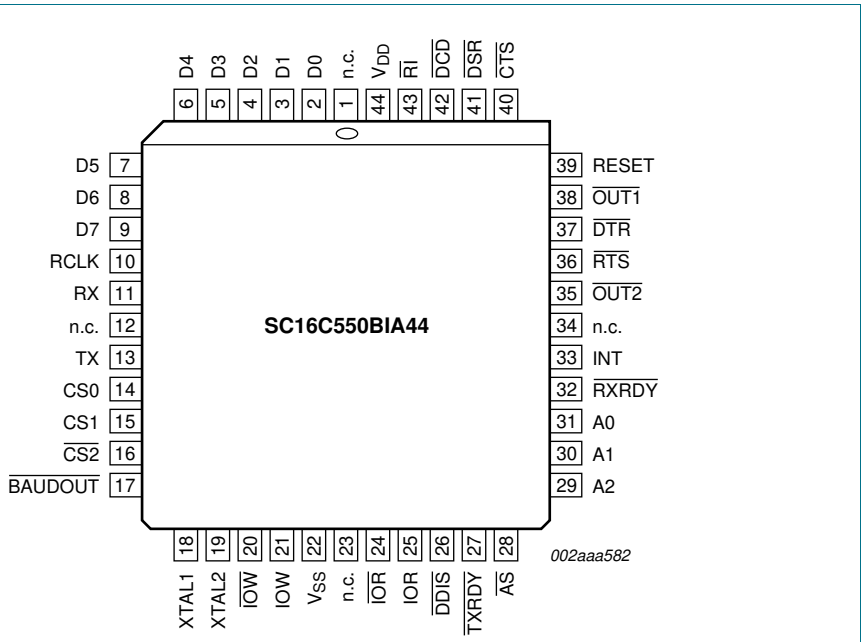


Fig 2. Pin configuration for PLCC44

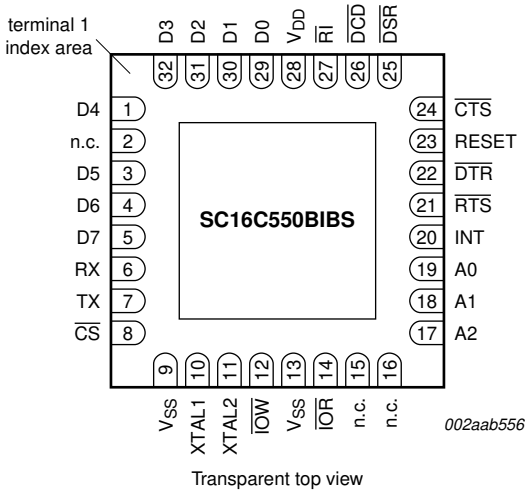


Fig 3. Pin configuration for HVQFN32

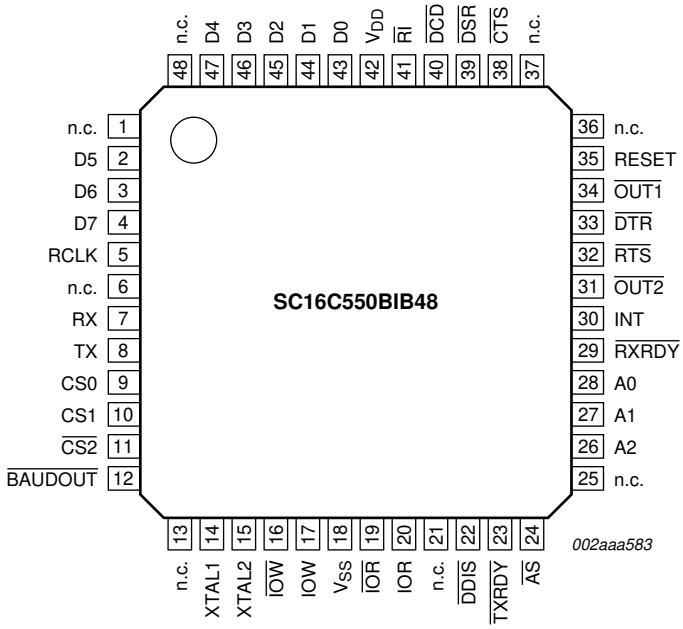


Fig 4. Pin configuration for LQFP48

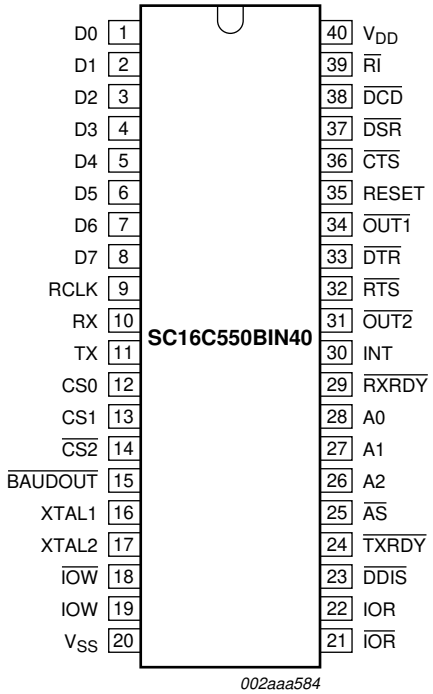


Fig 5. Pin configuration for DIP40

5.2 Pin description

Table 2. Pin description

Symbol	Pin				Type	Description
	PLCC44	LQFP48	DIP40	HVQFN32		
A0	31	28	28	19	I	**Register select.** A2 to A0 are used during read and write operations to select the UART register to read from or write to. Refer to Table 3 for register addresses and refer to $\overline{AS}$ description.
A1	30	27	27	18		
A2	29	26	26	17		
$\overline{AS}$	28	24	25	-	I	**Address strobe.** When $\overline{AS}$ is active (LOW), A0, A1, and A2 and CS0, $\overline{CS1}$, and $\overline{CS2}$ drive the internal select logic directly; when $\overline{AS}$ is HIGH, the register select and chip select signals are held at the logic levels they were in when the LOW-to-HIGH transition of $\overline{AS}$ occurred.
$\overline{BAUDOUT}$	17	12	15	-	O	**Baud out.** $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the UART. The clock rate is established by the reference oscillator frequency divided by a divisor specified in the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to RCLK. In HVQFN32 package $\overline{BAUDOUT}$ and RCLK are bonded internally.
CS0[2]	14	9	12	-	I	**Chip select.** When CS0 and CS1 are HIGH and $\overline{CS2}$ is LOW, these three inputs select the UART. When any of these inputs are inactive, the UART remains inactive (refer to $\overline{AS}$ description).
CS1[2]	15	10	13	-		
$\overline{CS2}$[2]	16	11	14	-		
$\overline{CS}$[2]	-	-	-	8		
$\overline{CTS}$[2]	40	38	36	24	I	**Clear to send.** $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 ($\overline{CTS}$) of the Modem Status Register. Bit 0 ($\overline{CTS}$) of the Modem Status Register indicates that $\overline{CTS}$ has changed states since the last read from the Modem Status Register. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. This pin has no effect on the UART's transmit or receive operation.
D7 to D0	9, 8, 7, 6, 5, 4, 3, 2	4, 3, 2, 47, 46, 45, 44, 43	8, 7, 6, 5, 4, 3, 2, 1	5, 4, 3, 1, 32, 31, 30, 29	I/O	**Data bus.** Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the UART and the CPU.
$\overline{DCD}$[2]	42	40	38	26	I	**Data carrier detect.** $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 ($\overline{DCD}$) of the Modem Status Register. Bit 3 ($\overline{DCD}$) of the Modem Status Register indicates that $\overline{DCD}$ has changed states since the last read from the Modem Status Register. If the modem status interrupt is enabled when $\overline{DCD}$ changes levels, an interrupt is generated.
$\overline{DDIS}$	26	22	23	-	O	**Driver disable.** $\overline{DDIS}$ is active (LOW) when the CPU is reading data. When inactive (HIGH), $\overline{DDIS}$ can disable an external transceiver.

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC44	LQFP48	DIP40	HVQFN32		
$\overline{DSR}$[2]	41	39	37	25	I	**Data set ready.** $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 ($\overline{DSR}$) of the Modem Status Register. Bit 1 ($\overline{DSR}$) of the Modem Status Register indicates $\overline{DSR}$ has changed levels since the last read from the Modem Status Register. If the modem status interrupt is enabled when $\overline{DSR}$ changes levels, an interrupt is generated.
$\overline{DTR}$	37	33	33	22	O	**Data terminal ready.** When active (LOW), $\overline{DTR}$ informs a modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the $\overline{DTR}$ bit of the Modem Control Register. $\overline{DTR}$ is placed in the inactive level either as a result of a Master Reset, during loopback mode operation, or clearing the $\overline{DTR}$ bit.
INT	33	30	30	20	O	**Interrupt.** When active (HIGH), INT informs the CPU that the UART has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty Transmitter Holding Register or an enabled modem status interrupt. INT is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset.
n.c.	1, 12, 23, 34	1, 6, 13, 21, 25, 36, 37, 48	-	2, 15, 16	-	not connected
$\overline{OUT1}$	38	34	34	-	O	**Outputs 1 and 2.** These are user-designated output terminals that are set to the active (LOW) level by setting respective Modem Control Register (MCR) bits ($\overline{OUT1}$ and $\overline{OUT2}$). $\overline{OUT1}$ and $\overline{OUT2}$ are set to inactive the (HIGH) level as a result of Master Reset, during loopback mode operations, or by clearing bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the MCR.
$\overline{OUT2}$	35	31	31	-		
RCLK	10	5	9	-	I	**Receiver clock.** RCLK is the 16× baud rate clock for the receiver section of the UART. In the HVQFN32 package, $\overline{BAUDOUT}$ and RCLK are bonded internally.
IOR	25	20	22	-	I	**Read inputs.** When either $\overline{IOR}$ or IOR is active (LOW or HIGH, respectively) while the UART is selected, the CPU is allowed to read status information or data from a selected UART register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (that is, IOR tied LOW or $\overline{IOR}$ tied HIGH).
$\overline{IOR}$[2]	24	19	21	14		
RESET	39	35	35	23	I	**Master reset.** When active (HIGH), RESET clears most UART registers and sets the levels of various output signals.

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC44	LQFP48	DIP40	HVQFN32		
$\overline{RI}$[2]	43	41	39	27	I	**Ring indicator.** $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 ($\overline{RI}$) of the Modem Status Register. Bit 2 ($\Delta\overline{RI}$) of the Modem Status Register indicates that $\overline{RI}$ has changed from a LOW to a HIGH level since the last read from the Modem Status Register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	36	32	32	21	O	**Request to send.** When active, $\overline{RTS}$ informs the modem or data set that the UART is ready to receive data. $\overline{RTS}$ is set to the active level by setting the $\overline{RTS}$ Modem Control Register bit and is set to the inactive (HIGH) level either as a result of a Master Reset or during loopback mode operations or by clearing bit 1 ($\overline{RTS}$) of the MCR. This pin has no effect on the UART's transmit or receive operation.
$\overline{RXRDY}$	32	29	29	-	O	**Receiver ready.** Receiver Direct Memory Access (DMA) signaling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using the FIFO Control Register bit 3 (FCR[3]). When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR[0] = 0 or FCR[0] = 1, FCR[3] = 0), when there is at least one character in the receiver FIFO or Receiver Holding Register, $\overline{RXRDY}$ is active (LOW). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (HIGH). In DMA mode 1 (FCR[0] = 1, FCR[3] = 1), when the trigger level or the time-out has been reached, $\overline{RXRDY}$ goes active (LOW); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (HIGH). This function does not exist in the HVQFN32 package.
RX	11	7	10	6	I	**Serial data input.** RX is serial data input from a connected communications device.
TX	13	8	11	7	O	**Serial data output.** TX is composite serial data output to a connected communication device. TX is set to the marking (HIGH) level as a result of Master Reset.
$\overline{TXRDY}$	27	23	24	-	O	**Transmitter ready.** Transmitter DMA signaling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using FCR[3]. When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled. This function does not exist in the HVQFN32 package.
V_{DD}	44	42	40	28	power	**2.5 V, 3.3 V or 5 V supply voltage.**
V_{SS}	22	18	20	9, 13[1]	power	**Ground voltage.**

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC44	LQFP48	DIP40	HVQFN32		
IOW	21	17	19	-	I	**Write inputs.** When either $\overline{IOW}$ or IOW is active (LOW or HIGH, respectively) and while the UART is selected, the CPU is allowed to write control words or data into a selected UART register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (that is, IOW tied LOW or $\overline{IOW}$ tied HIGH).
$\overline{IOW}$[2]	20	16	18	12		
XTAL1	18	14	16	10	I	**Crystal connection or External clock input.**
XTAL2[3]	19	15	17	11	O	**Crystal connection or the inversion of XTAL1 if XTAL1 is driven.**

[1] HVQFN32 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the Printed-Circuit Board (PCB) in the thermal pad region.

[2] This pin has a pull-up resistor.

[3] In Sleep mode, XTAL2 is left floating.

6. Functional description

The SC16C550B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C550B is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C550B is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C450. The SC16C550B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C550B by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt are provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C550B is capable of operation up to 3 Mbit/s with a 48 MHz external clock input (at 5 V).

6.1 Internal registers

The SC16C550B provides 12 internal registers for monitoring and control. These registers are shown in Table 3. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO Control Register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR). Register functions are more fully described in the following paragraphs.

Table 3. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

6.2 FIFO operation

The 16-byte transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). With 16C550 devices, the user can set the receive trigger level, but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 4. Flow control mechanism

Selected trigger level (characters)	INT pin activation	Negate $\overline{RTS}$	Assert $\overline{RTS}$
1	1	1	0
4	4	4	0
8	8	8	0
14	14	14	0

6.3 Autoflow control

Autoflow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ (see Figure 6). With auto-$\overline{\text{CTS}}$, the $\overline{\text{CTS}}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{\text{RTS}}$, $\overline{\text{RTS}}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using UART 1 and UART 2 from a SC16C550B with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

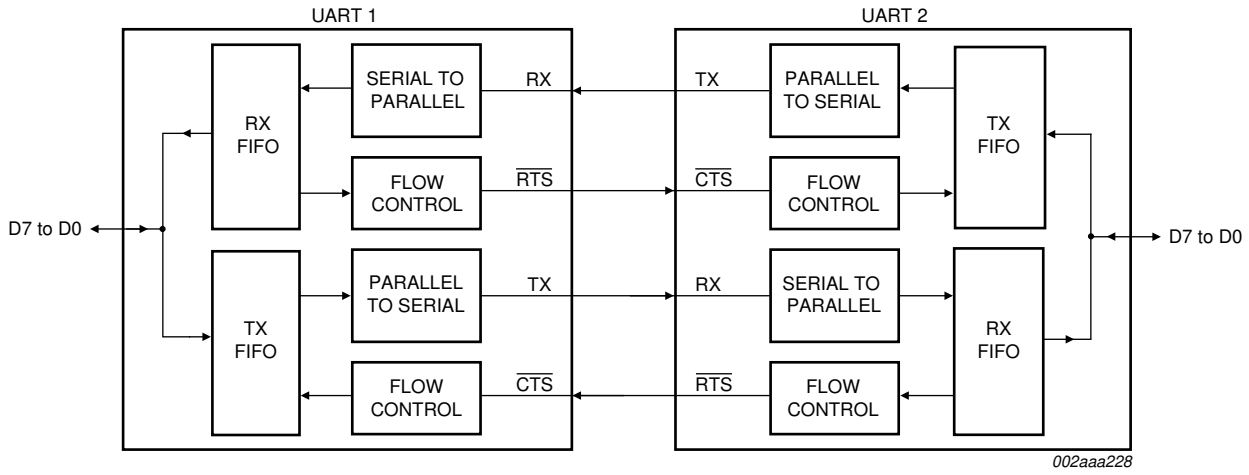


Fig 6. Autoflow control (auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$) example

6.3.1 Auto-$\overline{\text{RTS}}$

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver timing and control block (refer to Figure 1 “Block diagram of SC16C550B”) and is linked to the programmed receiver FIFO trigger level (see Figure 6). When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 8), $\overline{\text{RTS}}$ is de-asserted. With trigger levels of 1, 4, and 8, the sending UART may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it may not recognize the de-assertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the RX FIFO is emptied by reading the receiver buffer register. When the trigger level is 14 (see Figure 9), $\overline{\text{RTS}}$ is de-asserted after the first data bit of the 16th character is present on the RX line. $\overline{\text{RTS}}$ is reasserted when the RX FIFO has at least one available byte space.

6.3.2 Auto-$\overline{\text{CTS}}$

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte (see Figure 6). When $\overline{\text{CTS}}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 7). The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{\text{CTS}}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

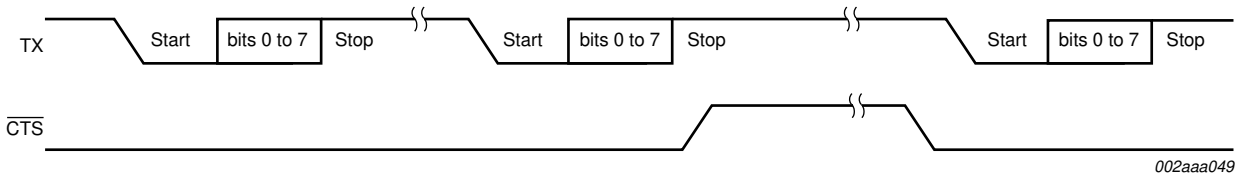
6.3.3 Enabling autoflow control and auto-$\overline{\text{CTS}}$

Autoflow control is enabled by setting MCR[5] and MCR[1].

Table 5. Enabling autoflow control and auto-$\overline{\text{CTS}}$

MCR[5]	MCR[1]	Selection
1	1	auto $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$
1	0	auto $\overline{\text{CTS}}$
0	X	disable

6.3.4 Auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ functional timing



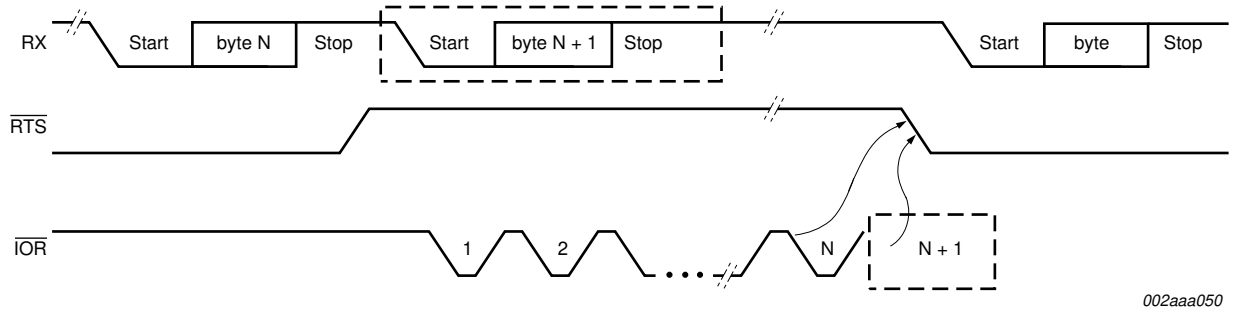
(1) When $\overline{\text{CTS}}$ is LOW, the transmitter keeps sending serial data out.

(2) If $\overline{\text{CTS}}$ goes HIGH before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte, but it does not send the next byte.

(3) When $\overline{\text{CTS}}$ goes from HIGH to LOW, the transmitter begins sending data again.

Fig 7. $\overline{\text{CTS}}$ functional timing waveforms

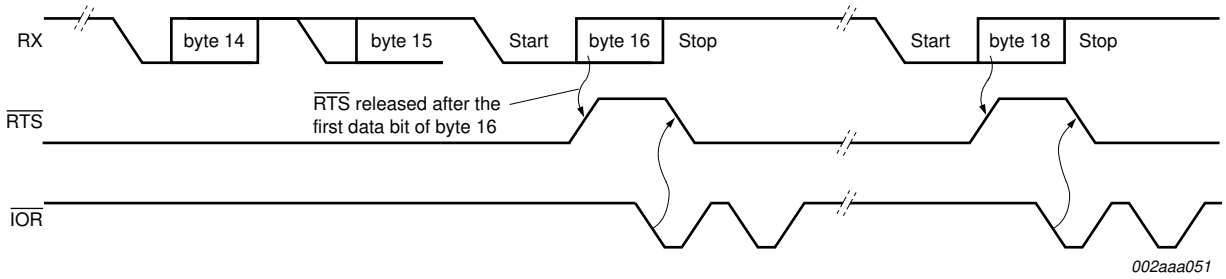
The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes. These are described in Figure 8 and Figure 9.



(1) N = RX FIFO trigger level (1, 4, or 8 bytes).

(2) The two blocks in dashed lines cover the case where an additional byte is sent as described in Section 6.3.1.

Fig 8. $\overline{\text{RTS}}$ functional timing waveforms, RX FIFO trigger level = 1, 4, or 8 bytes



(1) $\overline{RTS}$ is de-asserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.

(2) $\overline{RTS}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing, or there is more than one byte of space available.

(3) When the receive FIFO is full, the first receive buffer register read re-asserts $\overline{RTS}$.

Fig 9. $\overline{RTS}$ functional timing waveforms, RX FIFO trigger level = 14 bytes

6.4 Hardware/software and time-out interrupts

Following a reset, the transmitter interrupt is enabled, the SC16C550B will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The ISR register provides the current singular highest priority interrupt only. Only after servicing the higher pending interrupt will the lower priority be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C550B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

6.5 Programmable baud rate generator

The SC16C550B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s. The SC16C550B can support a standard data rate of 921.6 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable baud rate generator is capable of accepting an input clock up to 48 MHz, as required for supporting a 3 Mbit/s data rate. The SC16C550B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins (see Figure 10). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 6).

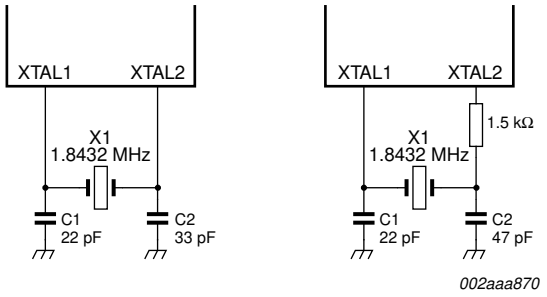


Fig 10. Crystal oscillator connection

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C550B divides the basic crystal or external clock by 16. The frequency of the $\overline{\text{BAUDOUT}}$ output pin is exactly 16× (16 times) the selected baud rate ($\overline{\text{BAUDOUT}}$ = 16 × baud rate). Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of the baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The examples in Table 6 shows selectable baud rates when using a 1.8432 MHz crystal.

For custom baud rates, the divisor value can be calculated using the following equation:

$$divisor\ (in\ decimal) = \frac{XTAL1\ clock\ frequency}{serial\ data\ rate \times 16} \quad (1)$$

Table 6. Baud rates using 1.8432 MHz or 3.072 MHz crystal

Using 1.8432 MHz crystal			Using 3.072 MHz crystal		
Desired baud rate	Divisor for 16× clock	Baud rate error	Desired baud rate	Divisor for 16× clock	Baud rate error
50	2304		50	3840	
75	1536		75	2560	
110	1047	0.026	110	1745	0.026
134.5	857	0.058	134.5	1428	0.034
150	768		150	1280	
300	384		300	640	
600	192		600	320	
1200	96		1200	160	
1800	64		1800	107	0.312
2000	58	0.69	2000	96	
2400	48		2400	80	
3600	32		3600	53	0.628
4800	24		4800	40	
7200	16		7200	27	1.23
9600	12		9600	20	
19200	6		19200	10	
38400	3		38400	5	
56000	2	2.86			

6.6 DMA operation

The SC16C550B FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). The DMA mode affects the state of the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ output pins. Table 7 and Table 8 show this.

Remark: DMA operation is not supported in the HVQFN32 package.

Table 7. Effect of DMA mode on state of $\overline{\text{RXRDY}}$ pin

Non-DMA mode	DMA mode
1 = FIFO empty	0-to-1 transition when FIFO empties
0 = at least 1 byte in FIFO	1-to-0 transition when FIFO reaches trigger level, or time-out occurs

Table 8. Effect of DMA mode on state of $\overline{\text{TXRDY}}$ pin

Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	1 = FIFO is full
0 = FIFO empty	0 = FIFO is empty

6.7 Loopback mode

The internal loopback capability allows on-board diagnostics. In the loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the loopback mode, $\overline{OUT1}$ (bit 2) and $\overline{OUT2}$ (bit 3) in the MCR register control the modem $\overline{RI}$ and $\overline{DCD}$ inputs, respectively. MCR signals $\overline{DTR}$ and $\overline{RTS}$ (bits 0:1) are used to control the modem $\overline{CTS}$ and $\overline{DSR}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 11). The inputs $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$. Loopback test data is entered into the transmit holding register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using the lower four bits of the Modem Status Register (MSR[3:0]) instead of the four Modem Status Register bits 7:4. The interrupts are still controlled by the IER.

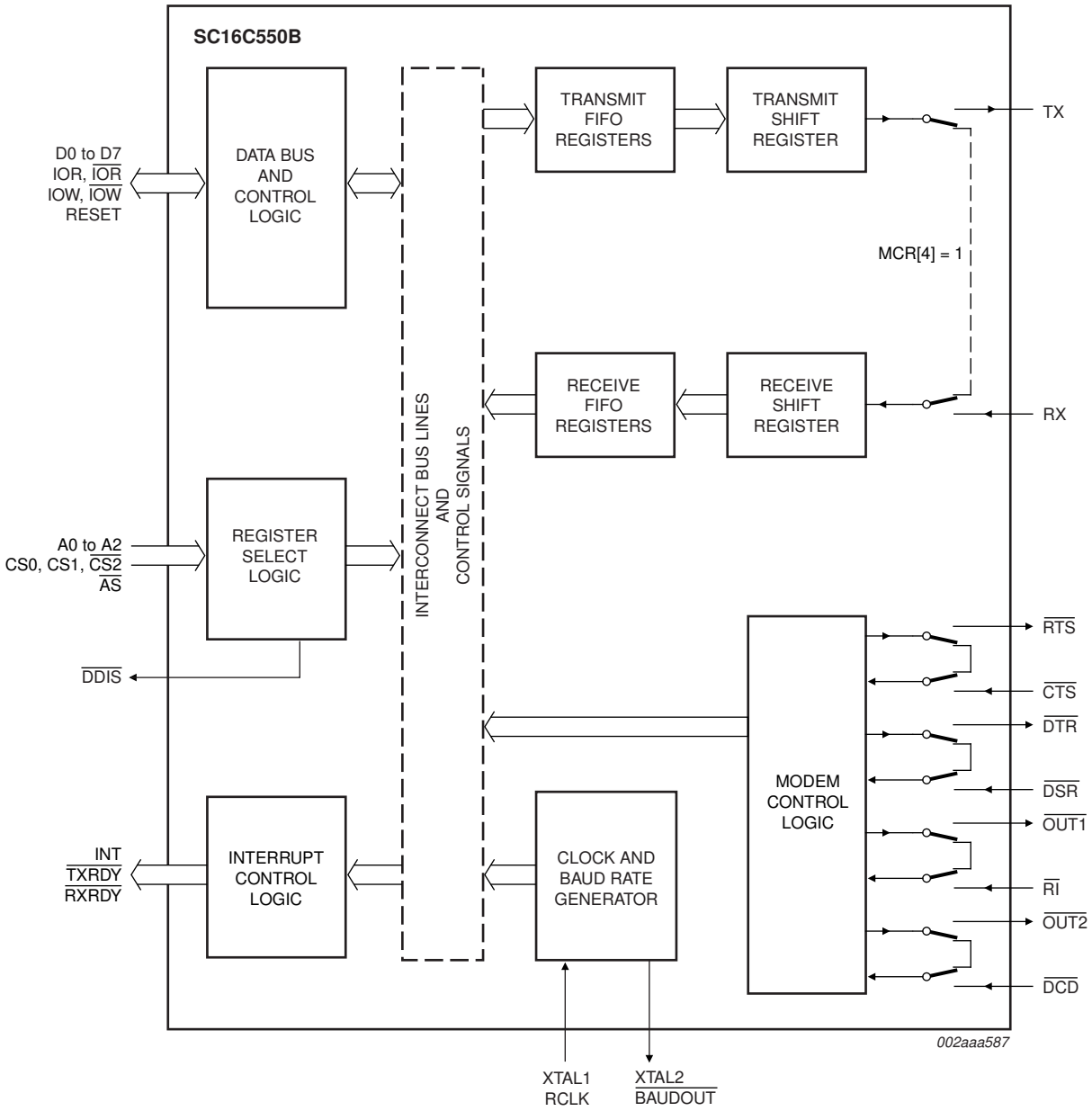


Fig 11. Internal loopback mode diagram

7. Register descriptions

Table 9 details the assigned bit functions for the twelve SC16C550B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.10.

Table 9. SC16C550B internal registers

A2	A1	A0	Register	Default [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General Register Set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00					modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	00	RX trigger (MSB)	RX trigger (LSB)	reserved	reserved	DMA mode select[3]	TX FIFO reset	RX FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	0	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	reserved		auto flow control enable	loopback	$\overline{\text{OUT2}}$, INT enable[4]	$\overline{\text{OUT1}}$[3]	$\overline{\text{RTS}}$	$\overline{\text{DTR}}$
1	0	1	LSR	60	FIFO data error	transmit empty	transmit holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	DCD	RI	DSR	CTS	$\Delta\overline{\text{DCD}}$	$\Delta\overline{\text{RI}}$	$\Delta\overline{\text{DSR}}$	$\Delta\overline{\text{CTS}}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special Register Set[5]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown represents the register's initialized hexadecimal value; X = not applicable.

[2] These registers are accessible only when LCR[7] is set to a logic 0.

[3] These functions are not supported in the HVQFN32 package, and should not be written.

[4] $\overline{\text{OUT2}}$ pin is not supported in the HVQFN32 package. MCR3 is INT enabled in the HVQFN32 package. INT is always enabled in DIP40, PLCC44 and LQFP48 packages.

[5] The Special Register set is accessible only when LCR[7] is set to a logic 1.

7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Holding Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D[7:0]) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C550B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT output pin.

Table 10. Interrupt Enable Register bits description

Bit	Symbol	Description
7:4	IER[7:4]	not used
3	IER[3]	Modem Status Interrupt. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a fully assembled receive character is transferred from RSR to the RHR/FIFO, that is, data ready, LSR[0]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1]. logic 0 = disable the transmitter empty interrupt (normal default condition) logic 1 = enable the transmitter empty interrupt
0	IER[0]	Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation. logic 0 = disable the receiver ready interrupt (normal default condition) logic 1 = enable the receiver ready interrupt

7.2.1 IER versus Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[0:3] enables the SC16C550B in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[1:4] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will indicate any FIFO data errors.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

(DMA mode does not exist in the HVQFN32 package; see Table 9.)

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is empty. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

7.3.2 FIFO mode

Table 11. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7] (MSB), FCR[6] (LSB)	RX trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 12.
5:4	FCR[5] (MSB), FCR[4] (LSB)	not used; set to 00
3	FCR[3]	DMA mode select. logic 0 = set DMA mode '0' (normal default condition) logic 1 = set DMA mode '1' **Transmit operation in mode '0':** When the SC16C550B is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode '0':** When the SC16C550B is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ pin will go to a logic 1 when there are no more characters in the receiver. **Transmit operation in mode '1':** When the SC16C550B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if the transmit FIFO is completely empty. **Receive operation in mode '1':** When the SC16C550B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDY}}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	TX FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RX FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO. **This bit must be a '1' when other FCR bits are written to, or they will not be programmed.**

Table 12. RX trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

7.4 Interrupt Status Register (ISR)

The SC16C550B provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 13 “Interrupt source” shows the data values (bits 3:0) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 13. Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 14. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled. logic 0 or cleared = default condition
5:4	ISR[5:4]	not used
3:1	ISR[3:1]	INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 13). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 15. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhance Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch and enhanced feature register enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5	LCR[5]	Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. Programs the parity conditions (see Table 16). logic 0 = parity is not forced (normal default condition) LCR[5] = logic 1 and LCR[4] = logic 0: parity bit is forced to a logical 1 for the transmit and receive data LCR[5] = logic 1 and LCR[4] = logic 1: parity bit is forced to a logical 0 for the transmit and receive data
4	LCR[4]	Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format. logic 0 = odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition). logic 1 = even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format.
3	LCR[3]	Parity enable. Parity or no parity can be selected via this bit. logic 0 = no parity (normal default condition) logic 1 = a parity bit is generated during the transmission, receiver checks the data and parity for transmission errors
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 17). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits [1:0]. These two bits specify the word length to be transmitted or received (see Table 18). logic 0 or cleared = default condition

Table 16. LCR[5] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
0	0	1	odd parity
0	1	1	even parity
1	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 17. LCR[2] stop bit length

LCR[2]	Word length	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 18. LCR[1:0] word length

LCR[1]	LCR[0]	Word length
0	0	5
0	1	6
1	0	7
1	1	8

7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 19. Modem Control Register bits description

Bit	Symbol	Description
7	MCR[7]	reserved; set to '0'
6	MCR[6]	reserved; set to '0'
5	MCR[5]	Auto flow control enable.
4	MCR[4]	Loopback. Enable the local loopback mode (diagnostics). In this mode the transmitter output (TX) and the receiver input (RX), $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$ are disconnected from the SC16C550B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 11). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable loopback mode (normal default condition) logic 1 = enable local loopback mode (diagnostics)
3	MCR[3]	$\overline{OUT2}$. Used to control the modem $\overline{DCD}$ signal in the loopback mode. logic 0 = $\overline{OUT2}$ is at logic 1. In the loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 1. logic 1 = $\overline{OUT2}$ is at logic 0. In the loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 0.
2	MCR[2]	$\overline{OUT1}$. This bit is used in the Loopback mode only. In the loopback mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal via $\overline{OUT1}$.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTS}$ output to a logic 0
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTR}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{DTR}$ output to a logic 0