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SC16C554B/554DB

5 V, 3.3 V and 2.5 V quad UART, 5 Mbit/s (max.) with 16-byte FIFOs

Rev. 4 — 8 June 2010 Product data sheet

1. General description

The SC16C554B/554DB is a 4-channel Universal Asynchronous Receiver and Transmitter (QUART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. It comes with an Intel (16 mode) or Motorola (68 mode) interface.

The SC16C554B/554DB is pin compatible with the ST16C554 and TL16C554 and it will power-up to be functionally equivalent to the 16C454. Programming of control registers enables the added features of the SC16C554B/554DB. Some of these added features are the 16-byte receive and transmit FIFOs, four receive trigger levels. The SC16C554B/554DB also provides DMA mode data transfers through FIFO trigger levels and the $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals. ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals are not available in the HVQFN48 package.) On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C554B/554DB operates at 5 V, 3.3 V and 2.5 V, and the industrial temperature range, and is available in plastic PLCC68, LQFP64, LQFP80, and HVQFN48 packages. On the HVQFN48 package only, channel C has all the modem pins. Channels A and B have only $\overline{\text{RTS}}$n and $\overline{\text{CTS}}$n pins and channel D does not have any modem pin.

2. Features and benefits

- 4 channel UART
- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range (−40 °C to +85 °C)
- The SC16C554B is pin and software compatible with the industry-standard ST16C454/554, ST68C454/554, ST16C554, TL16C554
- The SC16C554DB is pin and software compatible with ST16C554D, and software compatible with ST16C454/554, ST16C554, TL16C554
- Up to 5 Mbit/s data rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 5 V tolerant on input only pins[1]
- 16-byte transmit FIFO
- 16-byte receive FIFO with error flags
- Programmable auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$
  - In auto-$\overline{\text{CTS}}$ mode, $\overline{\text{CTS}}$ controls transmitter
  - In auto-$\overline{\text{RTS}}$ mode, RX FIFO contents and threshold control $\overline{\text{RTS}}$

1. For data bus pins D7 to D0, see Table 24 “Limiting values”.

- Automatic hardware flow control ($\overline{RTS}$/$\overline{CTS}$)
- Software selectable baud rate generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5-bit, 6-bit, 7-bit, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1^1\vee_2$, or 2-stop bit
  - Baud generation (DC to 5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{CD}$).

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16C554BIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
SC16C554BIB80	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
SC16C554BIBM	LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1
SC16C554BIBS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-3
SC16C554DBIA68	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SC16C554DBIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4. Block diagram

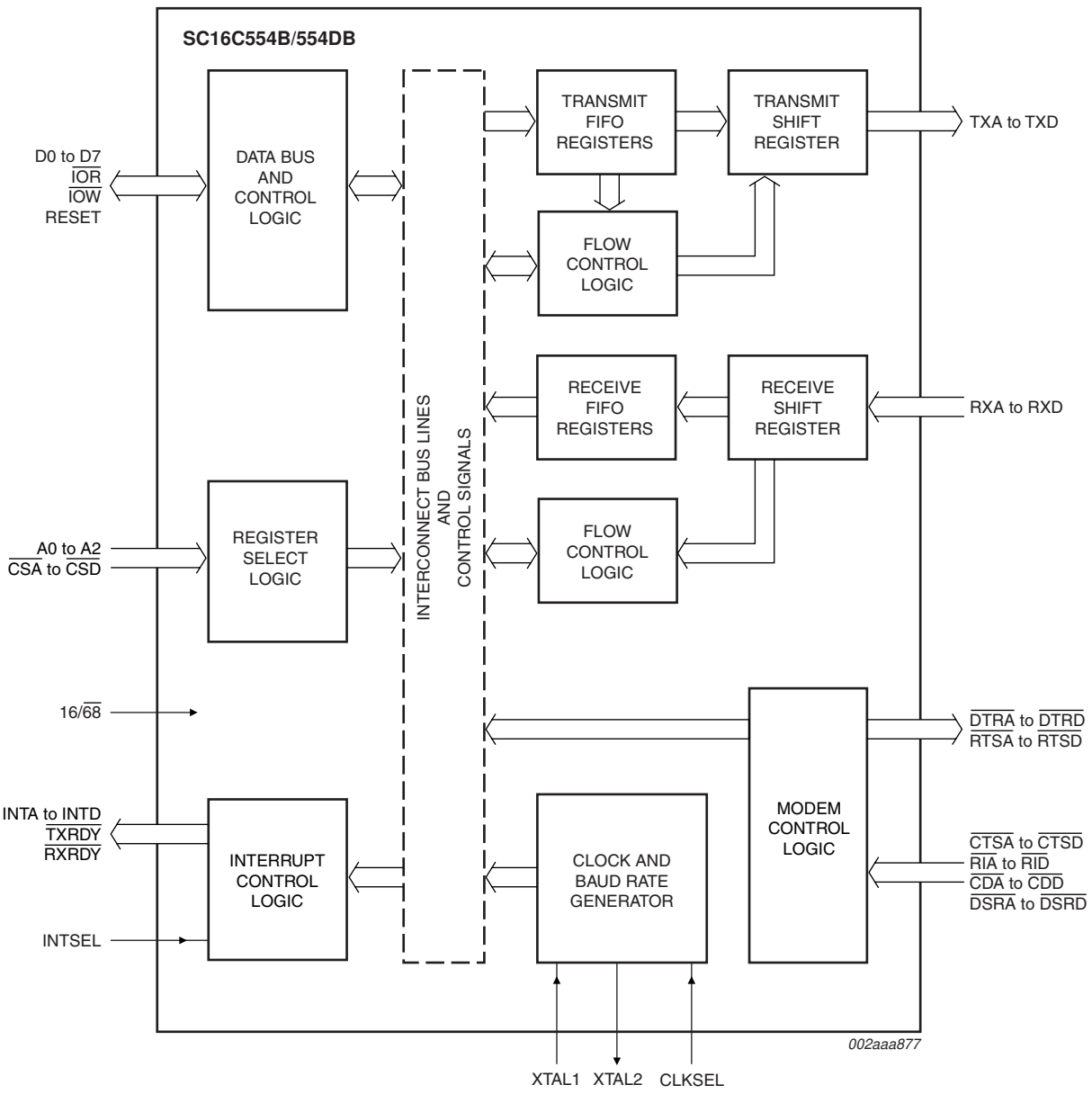


Fig 1. Block diagram of SC16C554B/554DB (16 mode)

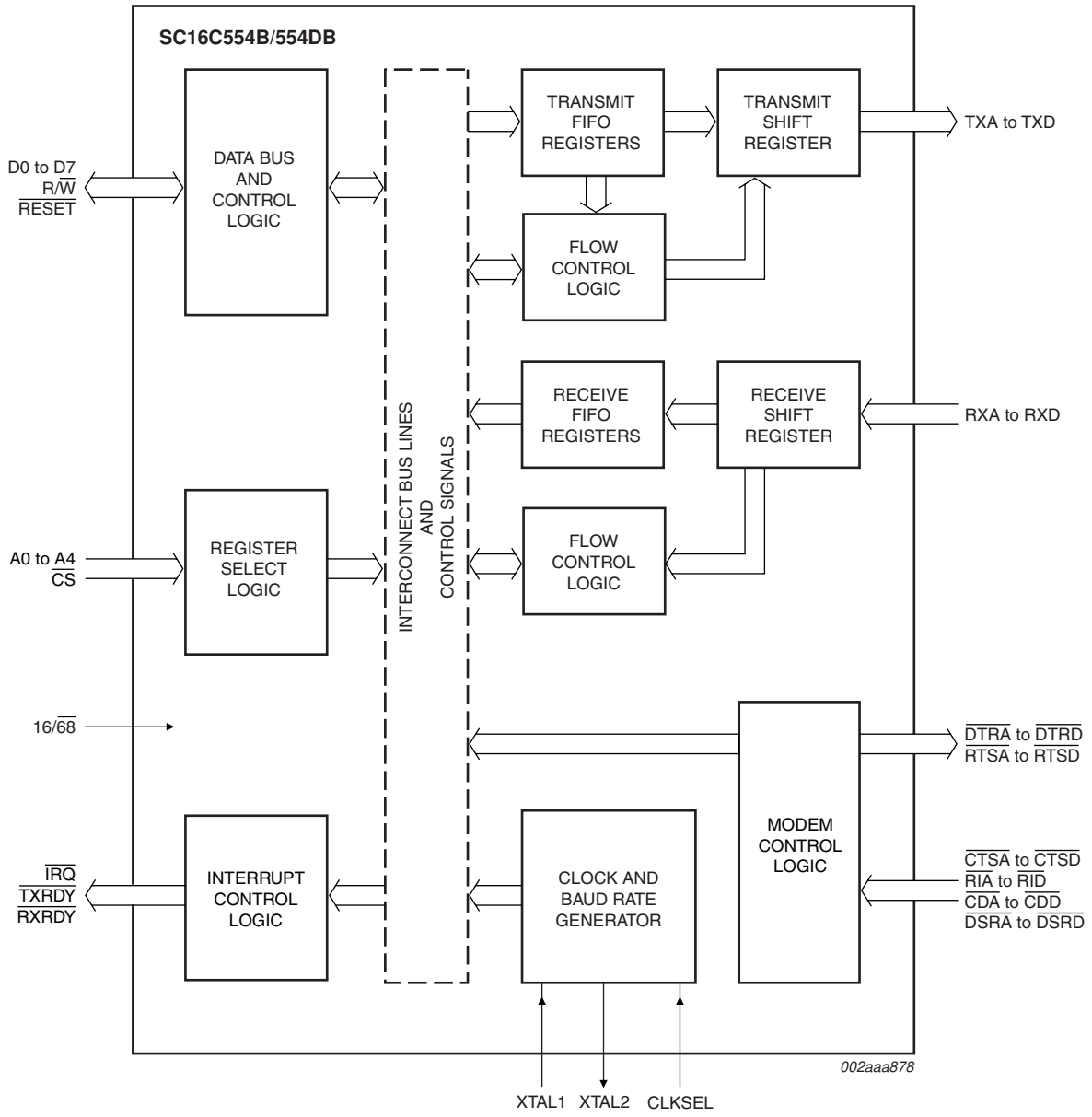


Fig 2. Block diagram of SC16C554B/554DB (68 mode)

5. Pinning information

5.1 Pinning

5.1.1 PLCC68

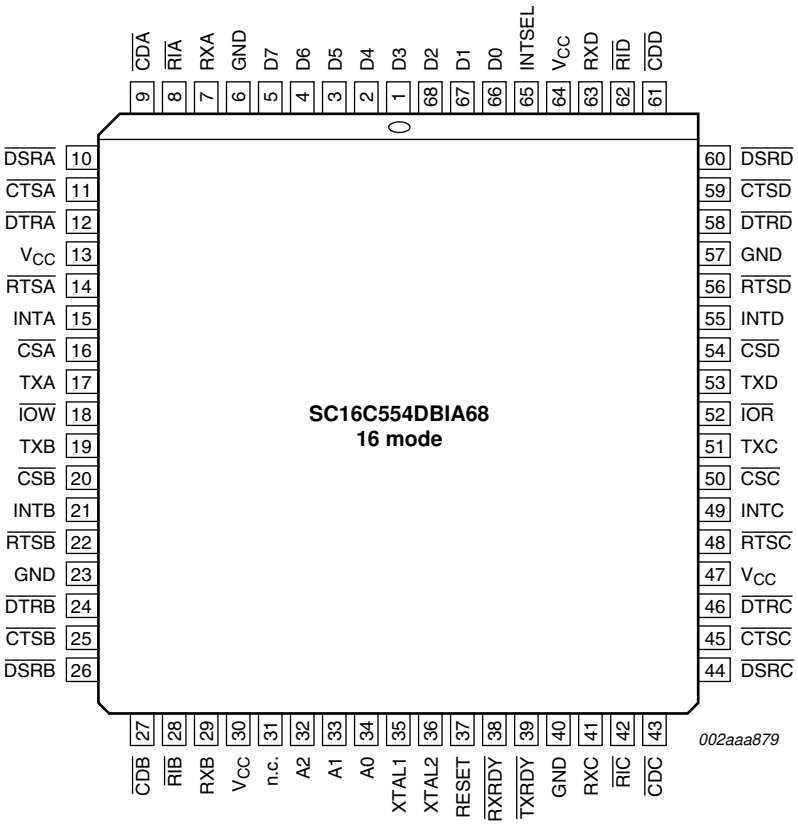


Fig 3. Pin configuration for PLCC68 (16 mode)

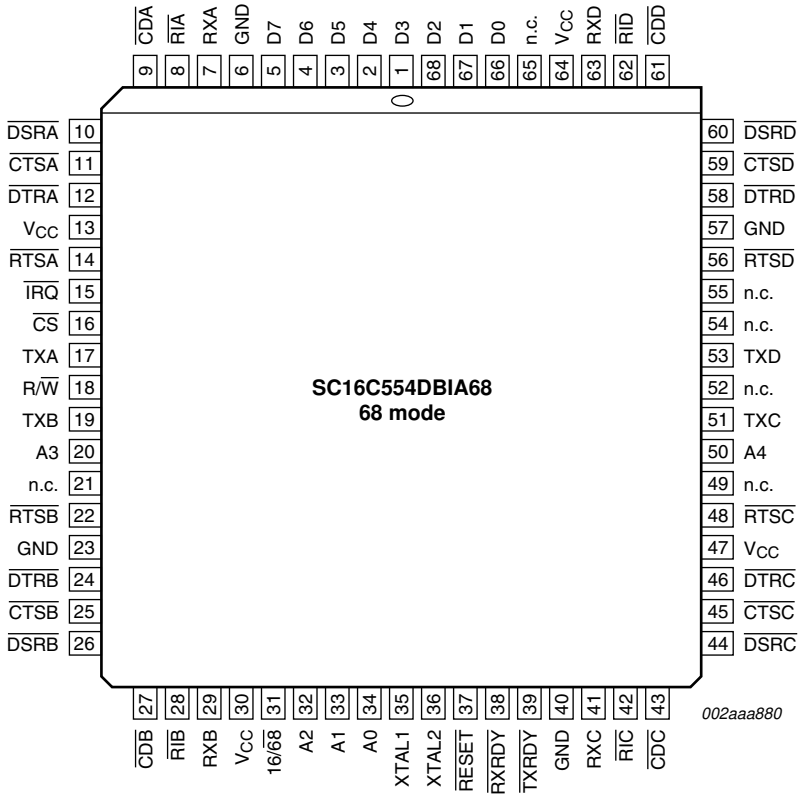


Fig 4. Pin configuration for PLCC68 (68 mode)

5.1.2 LQFP64

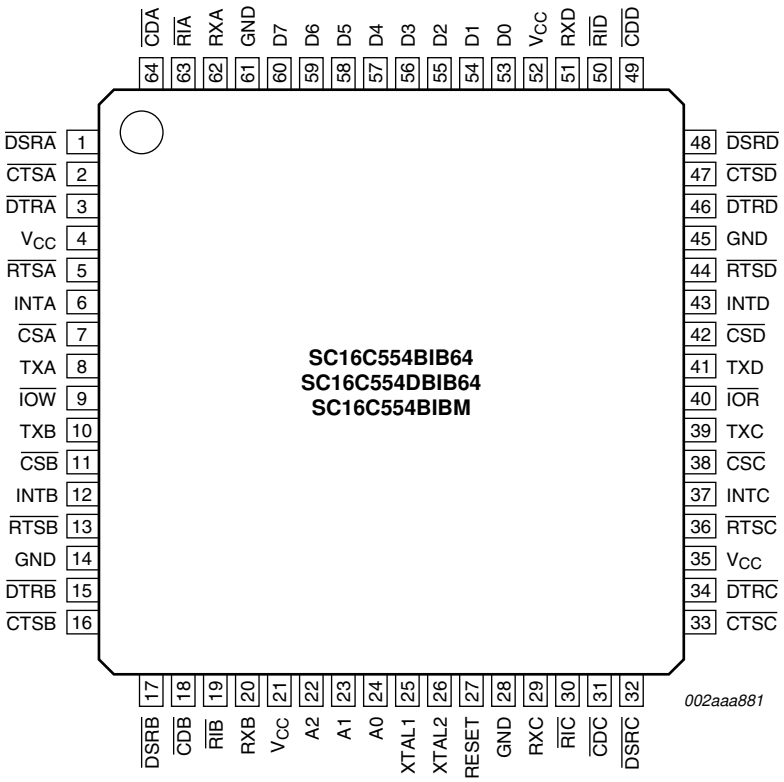


Fig 5. Pin configuration for LQFP64

5.1.3 LQFP80

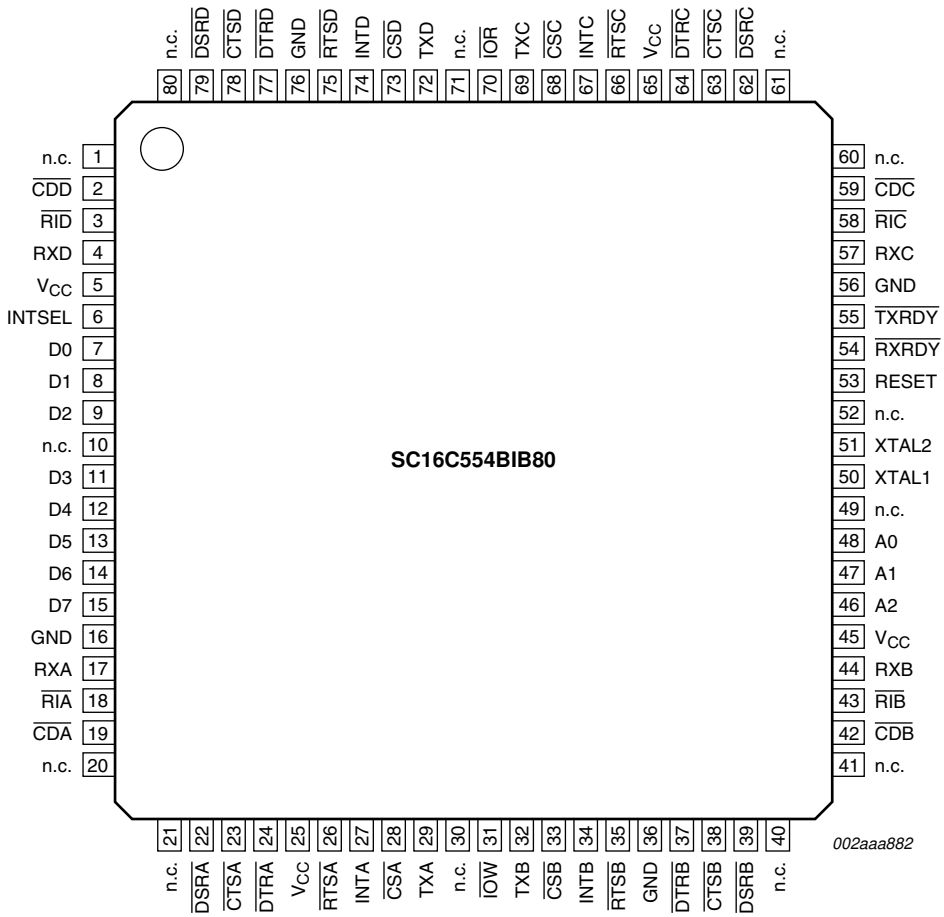
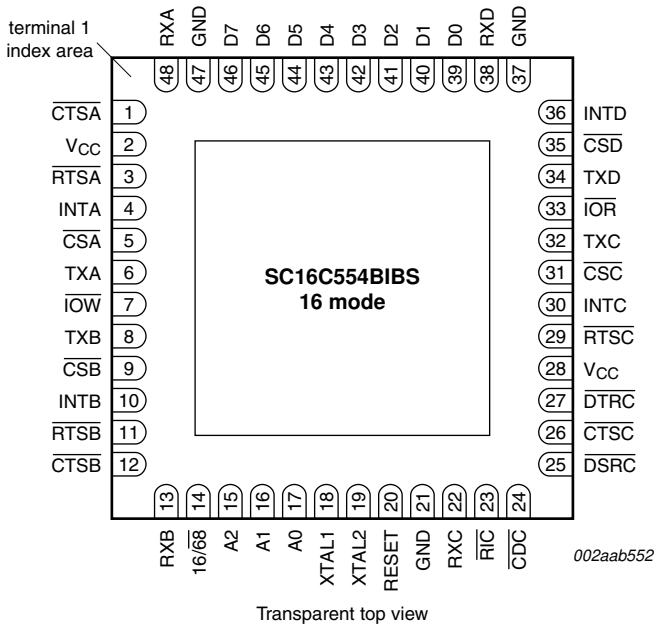


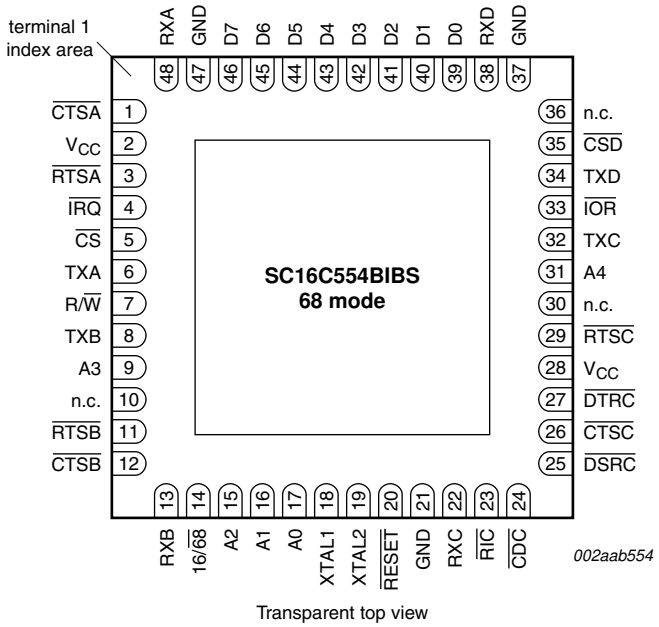
Fig 6. Pin configuration for LQFP80

5.1.4 HVQFN48



Transparent top view

Fig 7. Pin configuration for HVQFN (16 mode)



Transparent top view

Fig 8. Pin configuration for HVQFN (68 mode)

5.2 Pin description

Table 2. Pin description

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
16/$\overline{68}$	31	-	-	14	I	**16/68 Interface type select (input with internal pull-up).** This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of $\overline{IOR}$, $\overline{IOW}$, INTA to INTD, and $\overline{CSA}$ to $\overline{CSD}$ are re-assigned with the logic state of this pin. When this pin is a logic 1, the 16 mode interface (16C554) is selected. When this pin is a logic 0, the 68 mode interface (68C554) is selected. When this pin is a logic 0, $\overline{IOW}$ is re-assigned to R/$\overline{W}$, RESET is re-assigned to $\overline{RESET}$, $\overline{IOR}$ is not used, and INTA to INTD are connected in a wire-OR configuration. The wire-OR outputs are connected internally to the open-drain IRQ signal output. This pin is not available on 64-pin packages which operate in the 16 mode only.
A0	34	24	48	17	I	**Address 0 select bit.** Internal registers address selection in 16 and 68 modes.
A1	33	23	47	16	I	**Address 1 select bit.** Internal registers address selection in 16 and 68 modes.
A2	32	22	46	15	I	**Address 2 select bit.** Internal registers address selection in 16 and 68 modes.
A3	20	-	-	9	I	**Address 3 to Address 4 select bits.** When the 68 mode is selected, these pins are used to address or select individual UARTs (providing $\overline{CS}$ is a logic 0). In the 16 mode, these pins are re-assigned as chip selects, see $\overline{CSB}$ and $\overline{CSC}$.
A4	50	-	-	31	I	
$\overline{CDA}$	9	64	19	-	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	27	18	42	-	I	
$\overline{CDC}$	43	31	59	24	I	
$\overline{CDD}$	61	49	2	-	I	
$\overline{CS}$	16	-	-	5	I	**Chip Select (active LOW).** In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UARTs (A to D) are enabled when the $\overline{CS}$ pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3 to A4. when the 16 mode is selected (68-pin devices), this pin functions as $\overline{CSA}$ (see definition under $\overline{CSA}$, $\overline{CSB}$).
$\overline{CSA}$	16	7	28	5	I	**Chip Select A, B, C, D (active LOW).** This function is associated with the 16 mode only, and for individual channels 'A' through 'D'. When in 16 mode, these pins enable data transfers between the user CPU and the SC16C554B/554DB for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective $\overline{CSA}$ to $\overline{CSD}$ pin. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
$\overline{CSB}$	20	11	33	9	I	
$\overline{CSC}$	50	38	68	31	I	
$\overline{CSD}$	54	42	73	35	I	

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
$\overline{CTSA}$	11	2	23	1	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels A to D. A logic 0 on the $\overline{CTSn}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C554B/554DB. Status can be tested by reading MSR[4]. This pin only affects the transmit or receive operations when auto-$\overline{CTS}$ function is enabled via MCR[5] for hardware flow control operation.
$\overline{CTSB}$	25	16	38	12	I	
$\overline{CTSC}$	45	33	63	26	I	
$\overline{CTSD}$	59	47	78	-	I	
D0	66	53	7	39	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
D1	67	54	8	40	I/O	
D2	68	55	9	41	I/O	
D3	1	56	11	42	I/O	
D4	2	57	12	43	I/O	
D5	3	58	13	44	I/O	
D6	4	59	14	45	I/O	
D7	5	60	15	46	I/O	
$\overline{DSRA}$	10	1	22	-	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
$\overline{DSRB}$	26	17	39	-	I	
$\overline{DSRC}$	44	32	62	25	I	
$\overline{DSRD}$	60	48	79	-	I	
$\overline{DTRA}$	12	3	24	-	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the SC16C554B/554DB is powered-on and ready. This pin can be controlled via the Modem Control Register. Writing a logic 1 to MCR[0] will set the $\overline{DTRn}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation.
$\overline{DTRB}$	24	15	37	-	O	
$\overline{DTRC}$	46	34	64	27	O	
$\overline{DTRD}$	58	46	77	-	O	
GND	6, 23, 40, 57	14, 28, 45, 61	16, 36, 56, 76	21, 37, 47[1]	I	**Signal and power ground.**
INTA	15	6	27	4	O	**Interrupt A, B, C, D (active HIGH).** This function is associated with the 16 mode only. These pins provide individual channel interrupts INTA to INTD. INTA to INTD are enabled when MCR[3] is set to a logic 1, interrupts are enabled in the Interrupt Enable Register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
INTB	21	12	34	10	O	
INTC	49	37	67	30	O	
INTD	55	43	74	36	O	

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
INTSEL	65	-	6	-	I	**Interrupt Select (active HIGH, with internal pull-down).** This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR[3] to enable or disable the 3-state interrupts, INTA to INTD, or override MCR[3] and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR[3] to control the 3-state interrupt output. In this mode, MCR[3] is set to a logic 1 to enable the 3-state outputs. This pin is disabled in the 68 mode. Due to pin limitations on the 64-pin packages, this pin is not available. To cover this limitation, the SC16C554DBIB64 version operates in the continuous interrupt enable mode by bonding this pin to V_{CC} internally. The SC16C554BIB64 operates with MCR[3] control by bonding this pin to GND. The INTSEL pin is not available on the HVQFN48 package.
$\overline{IOR}$	52	40	70	33	I	**Input/Output Read strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an internal register defined by address bits A0 to A2 onto the SC16C554B/554DB data bus (D0 to D7) for access by external CPU. This pin is disabled in the 68 mode.
$\overline{IOW}$	18	9	31	7	I	**Input/Output Write strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0 to D7) from the external CPU to an internal register that is defined by address bits A0 to A2. When the 68 mode is selected, this pin functions as R/$\overline{W}$ (see definition under R/$\overline{W}$).
$\overline{IRQ}$	15	-	-	4	O	**Interrupt Request or Interrupt 'A'.** This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A to D are wire-ORed internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the Interrupt Enable Register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using $\overline{CS}$ and A3 to A4. In the 68 mode, and external pull-up resistor must be connected between this pin and V_{CC}. The function of this pin changes to INTA when operating in the 16 mode (see definition under INTA).
n.c.	21, 49, 52, 54, 55, 65	-	1, 10, 20, 21, 30, 40, 41, 49, 52, 60, 61, 71, 80	-	-	not connected

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
$\overline{\text{RESET}}$ (RESET)	37	27	53	20	I	**Reset.** In the 16 mode, a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See Section 7.10 "SC16C554B/554DB external reset conditions" for initialization details.) When 16/$\overline{68}$ is a logic 0 (68 mode), this pin functions similarly, bus as an inverted reset interface signal, $\overline{\text{RESET}}$.
$\overline{\text{RIA}}$	8	63	18	-	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A to D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
RIB	28	19	43	-	I	
RIC	42	30	58	23	I	
RID	62	50	3	-	I	
$\overline{\text{RTSA}}$	14	5	26	3	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A to D. A logic 0 on the $\overline{\text{RTS}}$n pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the Modem Control Register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when auto-$\overline{\text{RTS}}$ function is enabled via MCR[5] for hardware flow control operation.
$\overline{\text{RTSB}}$	22	13	35	11	O	
$\overline{\text{RTSC}}$	48	36	66	29	O	
$\overline{\text{RTSD}}$	56	44	75	-	O	
R/$\overline{\text{W}}$	18	-	-	7	I	**Read/Write strobe.** This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes. Logic 1 = Read from UART register selected by $\overline{\text{CS}}$ and A0 to A4. Logic 0 = Write to UART register selected by $\overline{\text{CS}}$ and A0 to A4.
RXA	7	62	17	48	I	**Receive data input RXA to RXD.** These inputs are associated with individual serial channel data to the SC16C554B/554DB. The RXn signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the RXn input pin is disabled and TX data is connected to the UART RX input internally.
RXB	29	20	44	13	I	
RXC	41	29	57	22	I	
RXD	63	51	4	38	I	
$\overline{\text{RXRDY}}$	38	-	54	-	O	**Receive Ready (active LOW).** $\overline{\text{RXRDY}}$ contains the wire-ORed status of all four receive channel FIFOs, RXRDYA to RXRDYD. A logic 0 indicates receive data ready status, that is, the RHR is full, or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is empty, or when there are no more characters available in either the FIFO or RHR. Individual channel RX status is read by examining individual internal registers via $\overline{\text{CS}}$ and A0 to A4 pin functions. The $\overline{\text{RXRDY}}$ pin is not available on the HVQFN48 package.

Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
TXA	17	8	29	6	O	**Transmit data A, B, C, D.** These outputs are associated with individual serial transmit channel data from the SC16C554B/554DB. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the TXn output pin is disabled and TX data is internally connected to the UART RX input.
TXB	19	10	32	8	O	
TXC	51	39	69	32	O	
TXD	53	41	72	34	O	
$\overline{\text{TXRDY}}$	39	-	55	-	O	**Transmit Ready (active LOW).** $\overline{\text{TXRDY}}$ contains the wire-ORed status of all four transmit channel FIFOs, TXRDYA to TXRDYD. A logic 0 indicates a buffer ready status, that is, at least one location is empty and available in one of the TX channels (A to D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR. Individual channel TX status can be read by examining individual internal registers via $\overline{\text{CS}}$ and A0 to A4 pin functions. The $\overline{\text{TXRDY}}$ pin is not available on the HVQFN48 package.
V_{CC}	13, 30, 47, 64	4, 21, 35, 52	5, 25, 45, 65	2, 28	I	**Power supply inputs.**
XTAL1	35	25	50	18	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see Figure 13). Alternatively, an external clock can be connected to this pin to provide custom data rates. (See Section 6.6 "Programmable baud rate generator".)
XTAL2	36	26	51	19	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output.

[1] HVQFN48 package die supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

The SC16C554B/554DB provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C554B/554DB represents such an integration with greatly enhanced features. The SC16C554B/554DB is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C554B/554DB is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C454. The SC16C554B/554DB is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C554B/554DB by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C554B/554DBAI68 combines the package interface modes of the 16C454/554 and 68C454/554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel-type of microprocessor bus, while the 68 mode is intended to operate with Motorola and other popular microprocessors. Following a reset, the SC16C554B/554DBAI68 is downward compatible with the 16C454/554 or the 68C454/554, dependent on the state of the interface mode selection pin, 16/$\overline{68}$.

The SC16C554B/554DB is capable of operation to 1.5 Mbit/s with a 24 MHz crystal and up to 5 Mbit/s with an external clock input (at 3.3 V and 5 V; at 2.5 V the maximum speed is 3 Mbit/s).

The rich feature set of the SC16C554B/554DB is available through internal registers. Selectable receive FIFO trigger levels, selectable transmit and receive baud rates, and modem interface controls are all standard features. In the 16 mode, INTSEL and MCR[3] can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations of the 64-pin package, this feature is offered by two different LQFP64 packages. The SC16C554DB operates in the continuous interrupt enable mode by bonding INTSEL to V_{CC} internally. The SC16C554B operates in conjunction with MCR[3] by bonding INTSEL to GND internally.

6.1 Interface options

Two user interface modes are selectable for the PLCC68 package. These interface modes are designated as the ‘16 mode’ and the ‘68 mode’. This nomenclature corresponds to the early 16C454/554 and 68C454/554 package interfaces respectively.

6.1.1 The 16 mode interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C454/554. In the 16 mode (pin 16/$\overline{68}$ = logic 1), each UART is selected with individual chip select ($\overline{CSn}$) pins, as shown in Table 3.

Table 3. Serial port channel selection, 16 mode interface

$\overline{CSA}$	$\overline{CSB}$	$\overline{CSC}$	$\overline{CSD}$	UART channel
1	1	1	1	none
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

6.1.2 The 68 mode interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode, the SC16C554B/554DB decodes two additional addresses, A3 to A4, to select one of the four UART ports. The A3 to A4 address decode function is used only when in the 68 mode (16/$\overline{68}$ = logic 0), and is shown in Table 4.

Table 4. Serial port channel selection, 68 mode interface

$\overline{CS}$	A4	A3	UART channel
1	n/a	n/a	none
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

6.2 Internal registers

The SC16C554B/554DB provides 12 internal registers for monitoring and control. These registers are shown in Table 5. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO Control Register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible Scratchpad Register (SPR). Register functions are more fully described in the following paragraphs.

Table 5. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. With SC16C554B devices, the user can set the receive trigger level, but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 6. Flow control mechanism

Selected trigger level (characters)	INTn pin activation	Negate $\overline{RTS}$	Assert $\overline{RTS}$
1	1	4	1
4	4	8	4
8	8	12	8
14	14	14	10

6.4 Autoflow control (see Figure 9)

Autoflow control is comprised of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, the $\overline{CTS}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using UART 1 and UART 2 from a SC16C554B/554DB with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

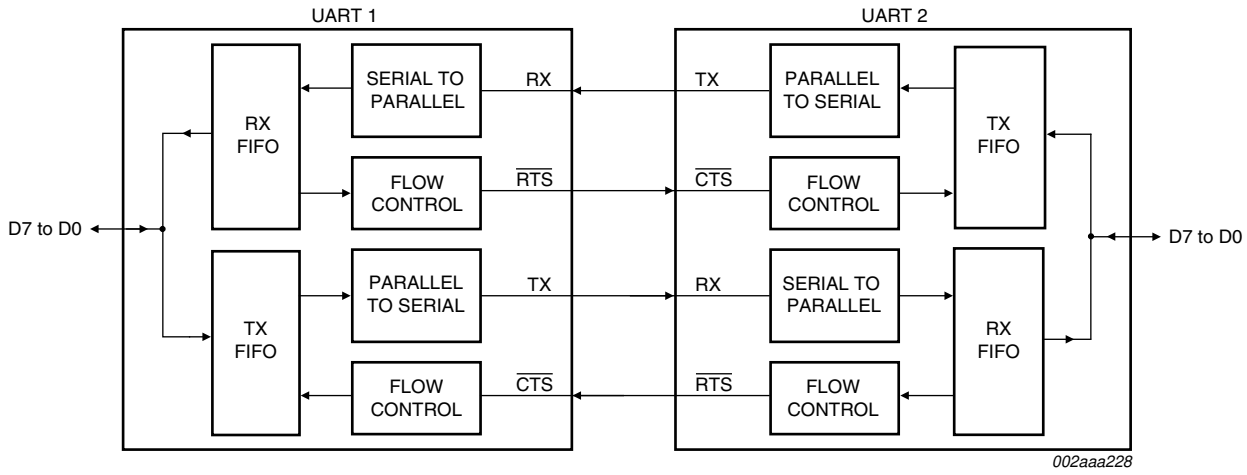


Fig 9. Autoflow control (auto-$\overline{RTS}$ and auto-$\overline{CTS}$) example

6.4.1 Auto-$\overline{RTS}$ (see Figure 9)

Auto-$\overline{RTS}$ data flow control originates in the receiver timing and control block (see block diagrams in Figure 1 and Figure 2) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 11), $\overline{RTS}$ is de-asserted. With trigger levels of 1, 4, and 8, the sending UART may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it may not recognize the de-assertion of $\overline{RTS}$ until after it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the RX FIFO is emptied by reading the receiver buffer register. When the trigger level is 14 (see Figure 12), $\overline{RTS}$ is de-asserted after the first data bit of the 16th character is present on the RX line. $\overline{RTS}$ is reasserted when the RX FIFO has at least one available byte space.

Remark: Auto-$\overline{RTS}$ is not supported in channel D of the HVQFN48 package, therefore MCR[5] of channel D should not be written.

6.4.2 Auto-$\overline{CTS}$ (see Figure 9)

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 10). The auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{CTS}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

Remark: Auto-$\overline{\text{CTS}}$ is not supported in channel D of the HVQFN48 package, therefore MCR[5] of channel D should not be written.

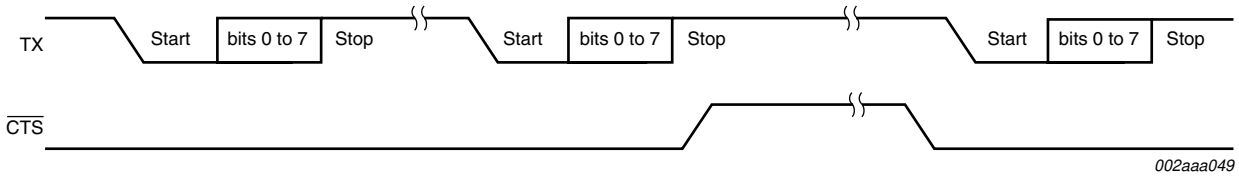
6.4.3 Enabling autoflow control and auto-$\overline{\text{CTS}}$

Autoflow control is enabled by setting MCR[5] and MCR[1].

Table 7. Enabling autoflow control and auto-$\overline{\text{CTS}}$

MCR[5]	MCR[1]	Selection
1	1	auto $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$
1	0	auto $\overline{\text{CTS}}$
0	X	disable

6.4.4 Auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ functional timing



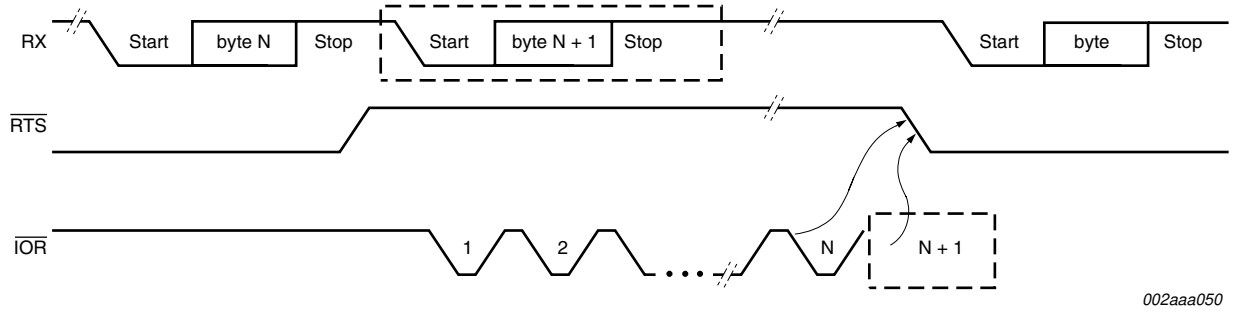
(1) When $\overline{\text{CTS}}$ is LOW, the transmitter keeps sending serial data out.

(2) If $\overline{\text{CTS}}$ goes HIGH before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte, but is does not send the next byte.

(3) When $\overline{\text{CTS}}$ goes from HIGH to LOW, the transmitter begins sending data again.

Fig 10. $\overline{\text{CTS}}$ functional timing waveforms

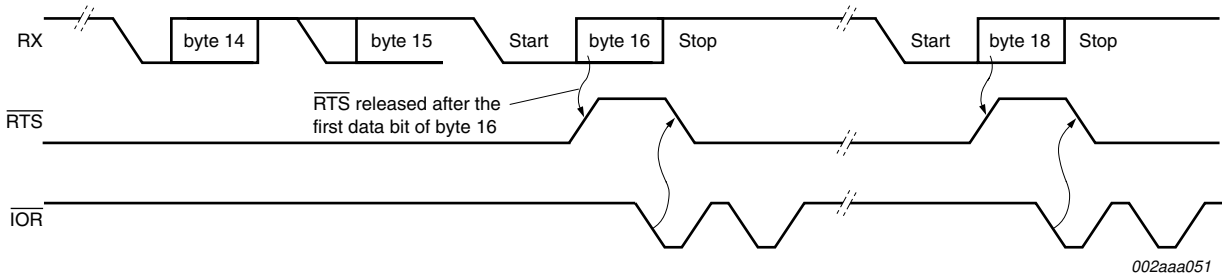
The receiver FIFO trigger level can be set to 1 byte, 4 bytes, 8 bytes, or 14 bytes. These are described in Figure 11 and Figure 12.



(1) N = RCV FIFO trigger level (1 byte, 4 bytes, or 8 bytes).

(2) The two blocks in dashed lines cover the case where an additional byte is sent as described in Section 6.4.1.

Fig 11. $\overline{\text{RTS}}$ functional timing waveforms, RCV FIFO trigger level = 1 byte, 4 bytes, or 8 bytes



(1) $\overline{RTS}$ is de-asserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.

(2) $\overline{RTS}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing, or there is more than one byte of space available.

(3) When the receive FIFO is full, the first receive buffer register read re-asserts $\overline{RTS}$.

Fig 12. $\overline{RTS}$ functional timing waveforms, RCV FIFO trigger level = 14 bytes

6.5 Hardware/software and time-out interrupts

Following a reset, if the transmitter interrupt is enabled, the SC16C554B/554DB will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C554B/554DB FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time.

In the 16 mode for the PLCC68 package, the system/board designer can optionally provide software controlled 3-state interrupt operation. This is accomplished by INTSEL and MCR[3]. When INTSEL interface pin is left open or made a logic 0, MCR[3] controls the 3-state interrupt outputs, INTA to INTD. When INTSEL is a logic 1, MCR[3] has no effect on the INTA to INTD outputs, and the package operates with interrupt outputs enabled continuously.

6.6 Programmable baud rate generator

The SC16C554B/554DB supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 80 MHz (for 3.3 V and 5 V operation), as required for supporting a 5 Mbit/s data rate. The SC16C554B/554DB can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 13). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 8).

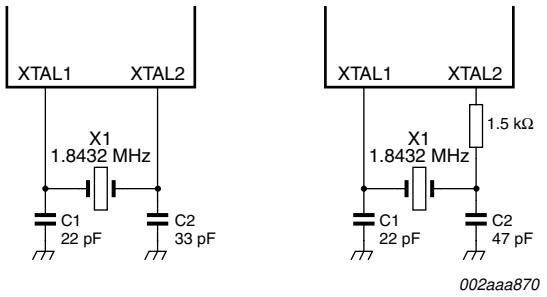


Fig 13. Crystal oscillator connection

Programming the Baud Rate Generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate.

Table 8. Baud rate generator programming table using a 7.3728 MHz clock

Output baud rate (bit/s)	User 16× clock divisor		DLM program value (hex)	DLL program value (hex)
	Decimal	Hexadecimal		
200	2304	900	09	00
1200	384	180	01	80
2400	192	C0	00	C0
4800	96	60	00	60
9600	48	30	00	30
19.2 k	24	18	00	18
38.4 k	12	0C	00	0C
76.8 k	6	06	00	06
153.6 k	3	03	00	03
230.4 k	2	02	00	02
460.8 k	1	01	00	01

6.7 DMA operation

The SC16C554B/554DB FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[6:5] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C554B/554DB activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the SC16C554B/554DB sets the interrupt output pin when the characters in the receive FIFOs are above the receive trigger level.

Remark: DMA operation is not supported in the HVQFN48 package.

6.8 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, $\overline{OP2}$ and $\overline{OP1}$ in the MCR register (bits 3:2) control the modem $\overline{RI}$ and $\overline{CD}$ inputs, respectively. MCR signals $\overline{RTS}$ and $\overline{DTR}$ (bits 1:0) are used to control the modem $\overline{CTS}$ and $\overline{DSR}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 14). The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, $\overline{OP2}$ and $\overline{OP1}$. Loopback test data is entered into the Transmit Holding Register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[3:0]) instead of the four Modem Status Register bits 7:4. The interrupts are still controlled by the IER.

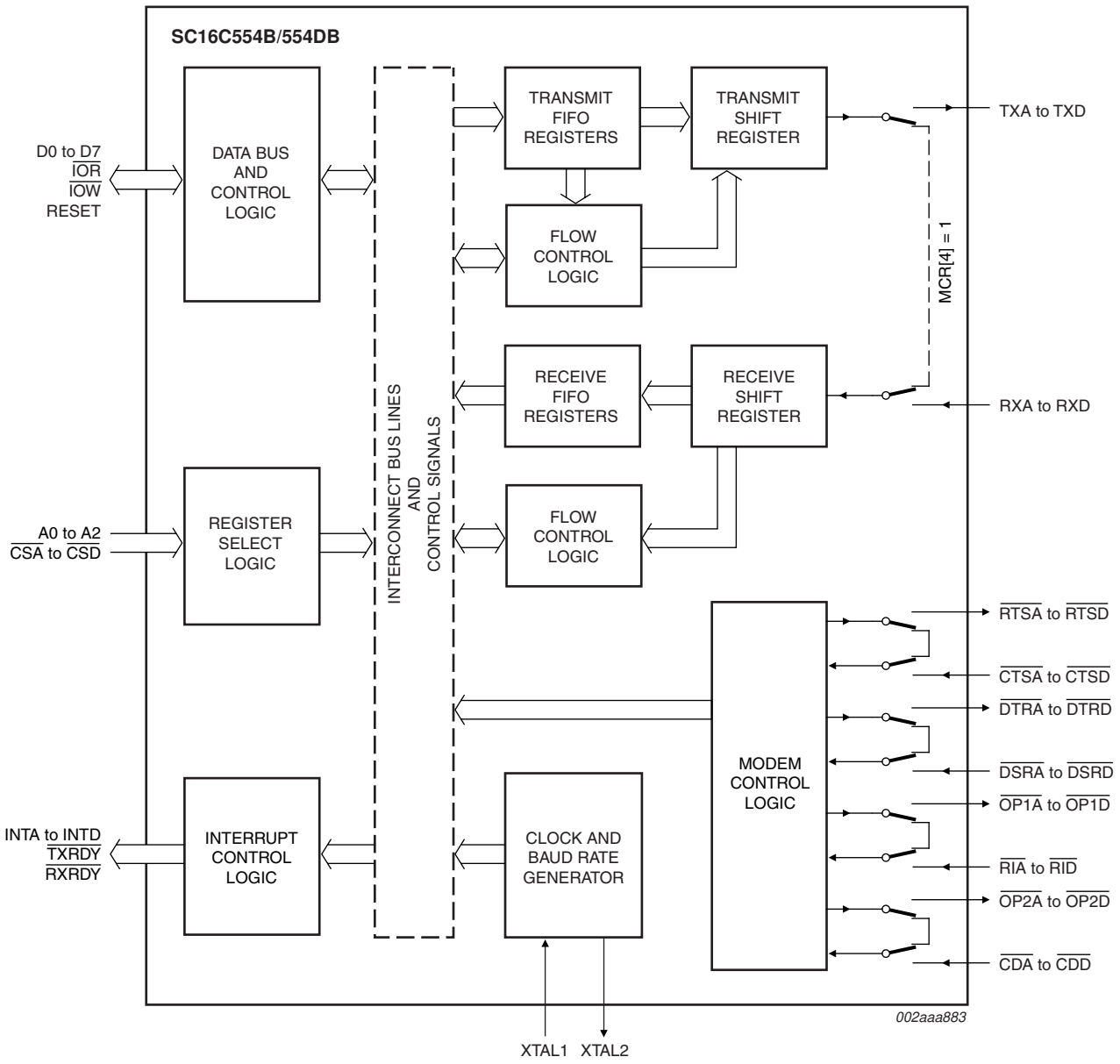


Fig 14. Internal Loopback mode diagram (16 mode)

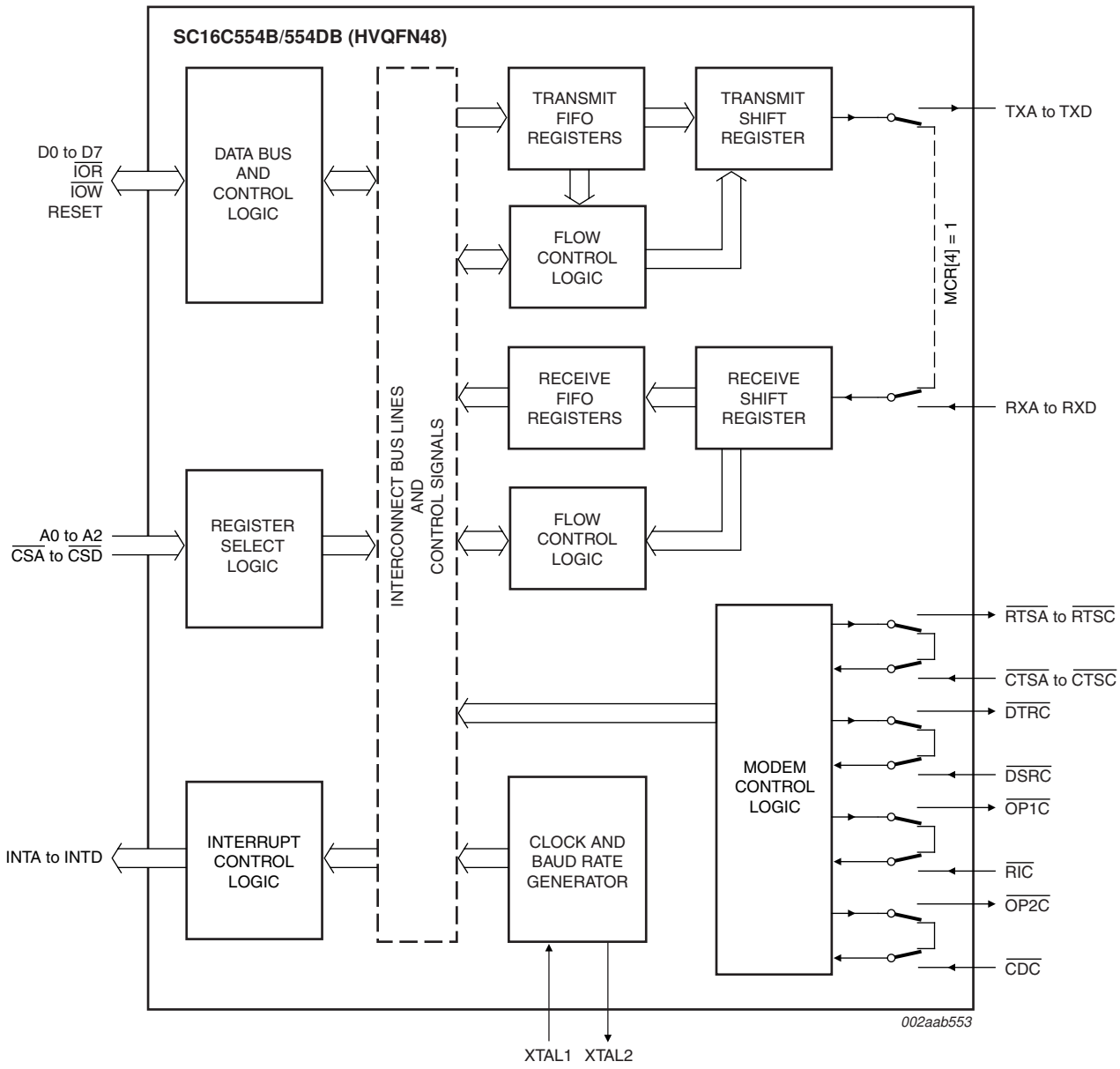


Fig 15. Internal Loopback mode diagram (16 mode) for HVQFN48 package

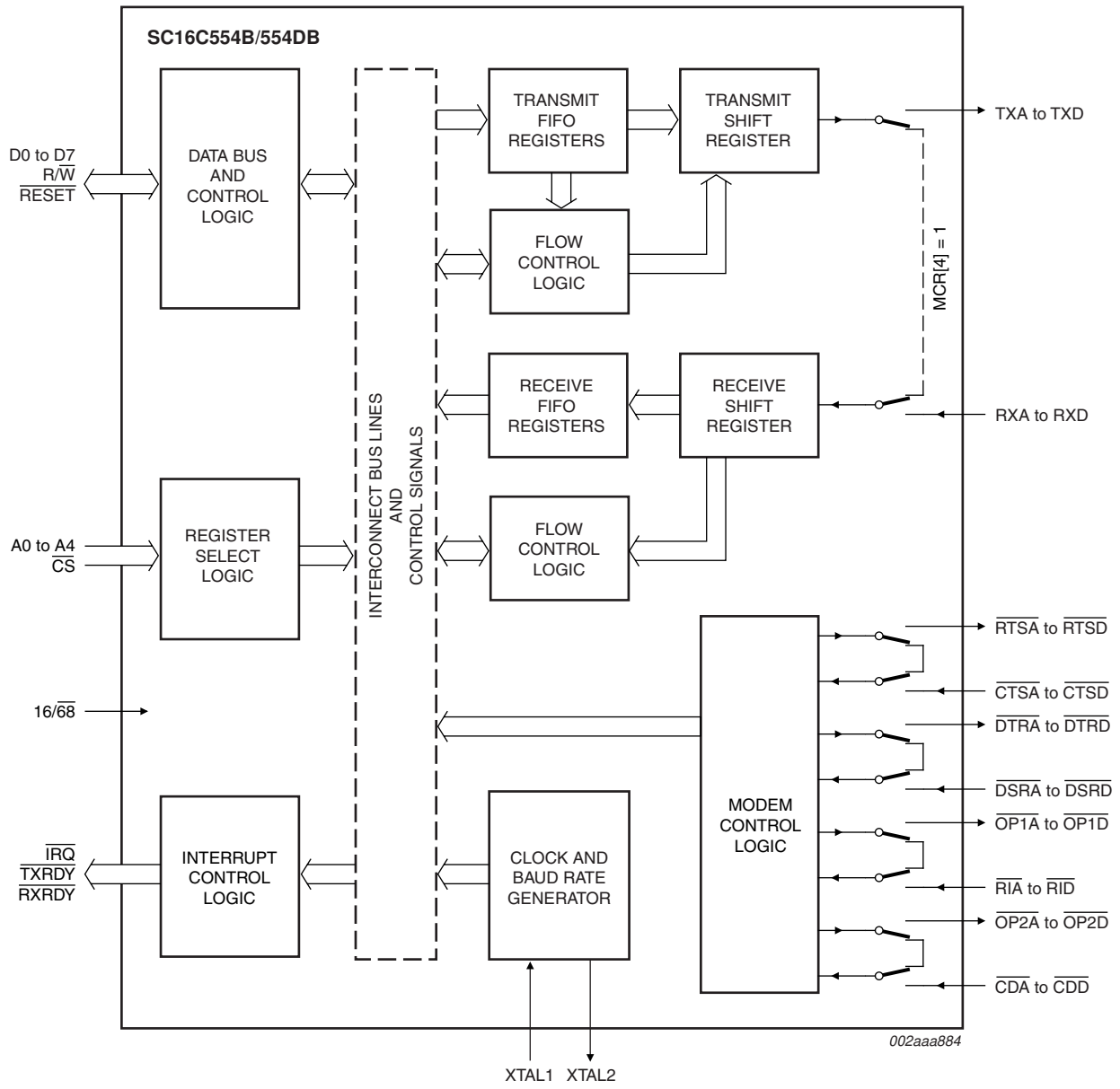


Fig 16. Internal Loopback mode diagram (68 mode)