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# SC16C554/554D

Quad UART with 16-byte FIFO and infrared (IrDA) encoder/decoder

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Product data

## 1. Description

The SC16C554/554D is a 4-channel Universal Asynchronous Receiver and Transmitter (QUART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. It comes with an Intel or Motorola interface.

The SC16C554/554D is pin compatible with the ST16C554 and TL16C554 and it will power-up to be functionally equivalent to the 16C454. Programming of control registers enables the added features of the SC16C554/554D. Some of these added features are the 16-byte receive and transmit FIFOs, automatic hardware or software flow control and Infrared encoding/decoding. The selectable auto-flow control feature significantly reduces software overload and increases system efficiency while in FIFO mode by automatically controlling serial data flow using  $\overline{\text{RTS}}$  output and  $\overline{\text{CTS}}$  input signals. The SC16C554/554D also provides DMA mode data transfers through FIFO trigger levels and the  $\overline{\text{TXRDY}}$  and  $\overline{\text{RXRDY}}$  signals. On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows on-board diagnostics.

The SC16C554/554D operates at 5 V, 3.3 V and 2.5 V, and the industrial temperature range, and is available in plastic PLCC68, LQFP64, and LQFP80 packages.

## 2. Features

- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range
- The SC16C554/554D is pin compatible with the industry-standard ST16C454/554, ST68C454/554, ST16C554, TL16C554
- Up to 5 Mbit/s data rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 16-byte transmit FIFO
- 16-byte receive FIFO with error flags
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Software selectable Baud Rate Generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Sleep mode
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled



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- Fully programmable character formatting:
  - ◆ 5, 6, 7, or 8-bit characters
  - ◆ Even, Odd, or No-Parity formats
  - ◆ 1, 1½, or 2-stop bit
  - ◆ Baud generation (DC to 5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-State output TTL drive capabilities for bi-directional data bus and control bus
- Line Break generation and detection
- Internal diagnostic capabilities:
  - ◆ Loop-back controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ( $\overline{\text{CTS}}$ ,  $\overline{\text{RTS}}$ ,  $\overline{\text{DSR}}$ ,  $\overline{\text{DTR}}$ ,  $\overline{\text{RI}}$ ,  $\overline{\text{DCD}}$ ).

### 3. Ordering information

Table 1: Ordering information

| Type number   | Package |  |          |
|---------------|---------|--|----------|
|               | Name    | Description  | Version  |
| SC16C554DIA68 | PLCC68  | plastic leaded chip carrier; 68 leads                                  | SOT188-2 |
| SC16C554DIB64 | LQFP64  | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| SC16C554IB64  | LQFP64  | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| SC16C554IB80  | LQFP80  | plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm | SOT315-1 |

4. Block diagram

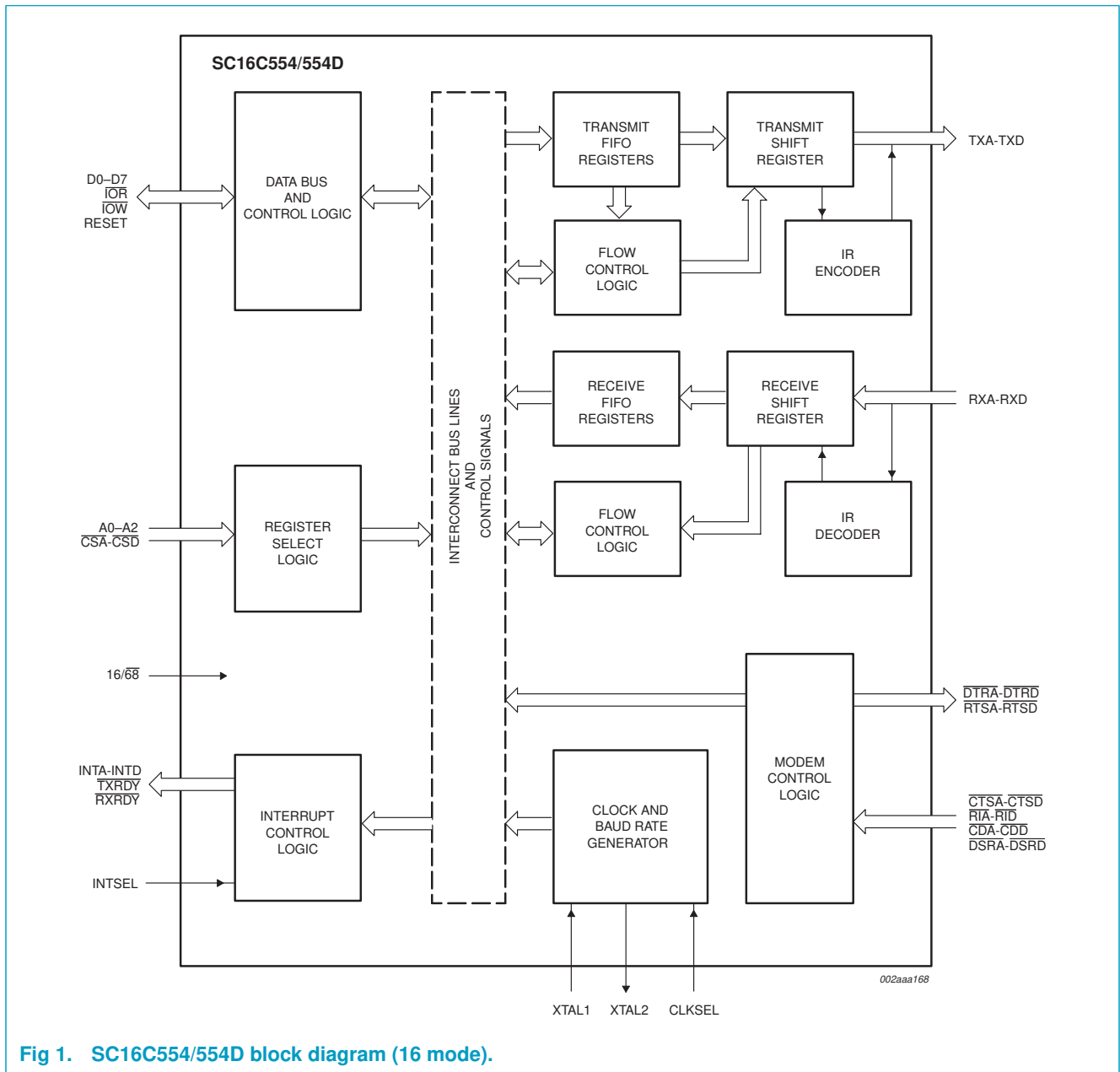


Fig 1. SC16C554/554D block diagram (16 mode).



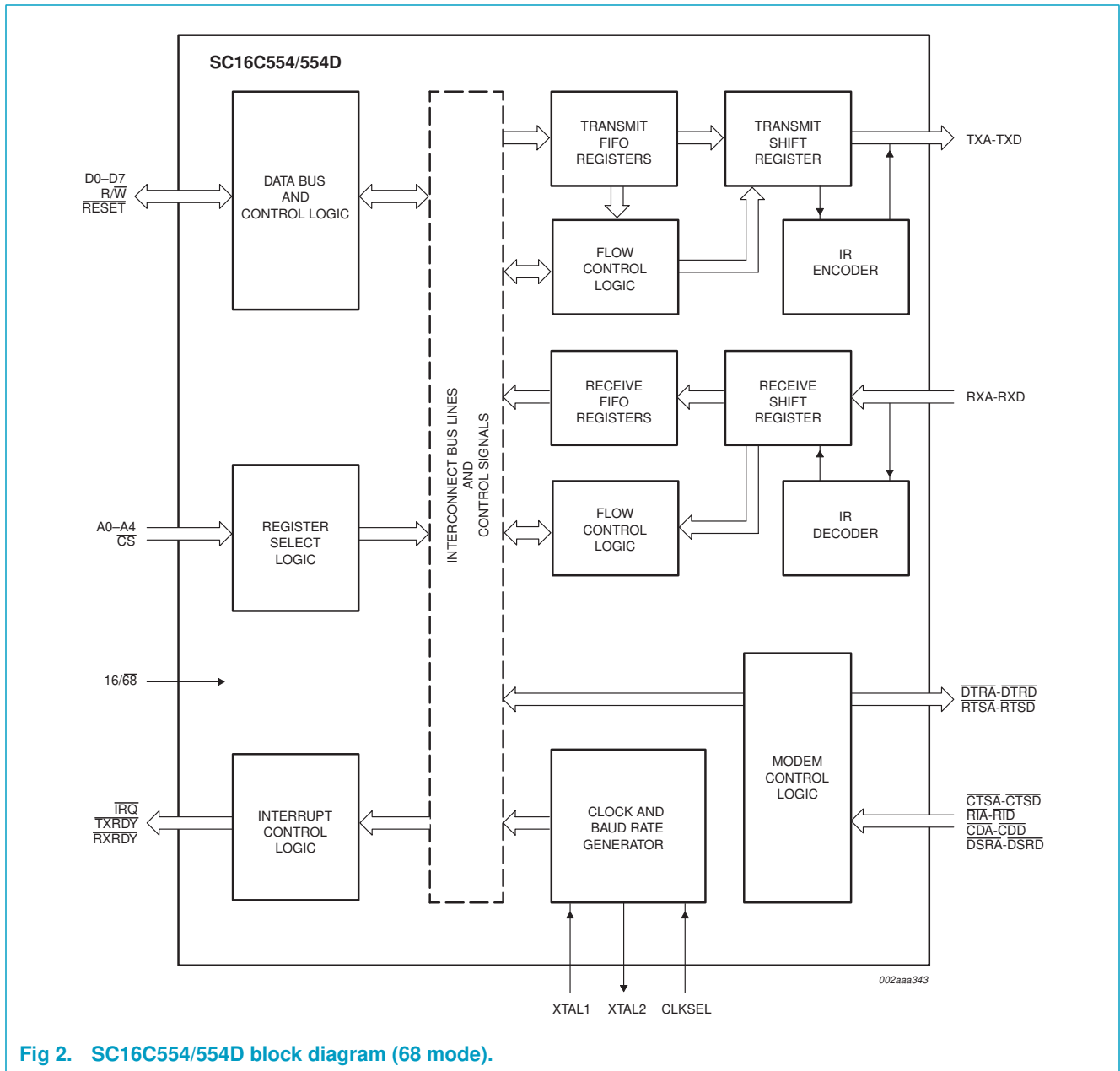


Fig 2. SC16C554/554D block diagram (68 mode).

## 5. Pinning information

### 5.1 Pinning

#### 5.1.1 PLCC68

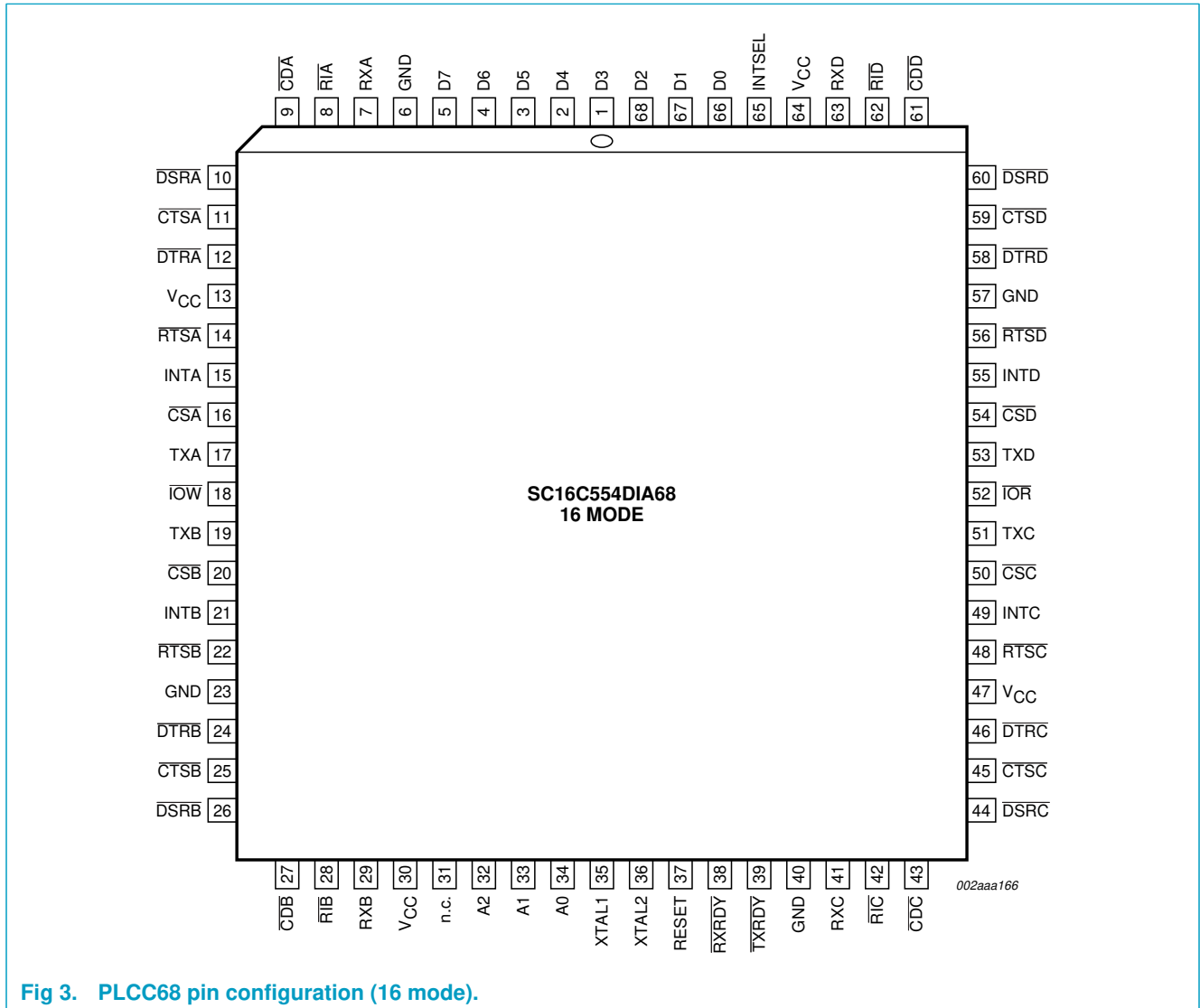


Fig 3. PLCC68 pin configuration (16 mode).

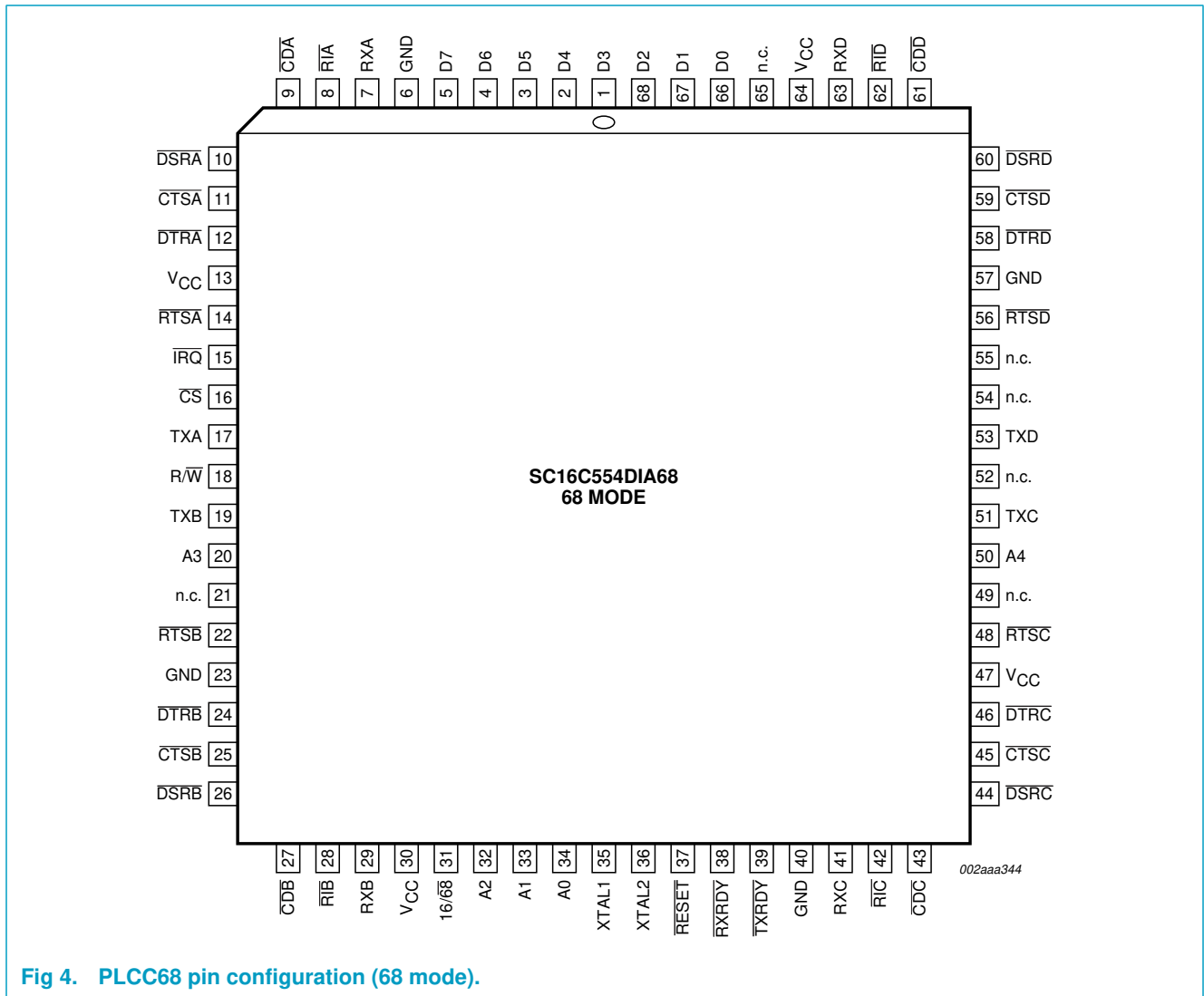


Fig 4. PLCC68 pin configuration (68 mode).

5.1.2 LQFP64

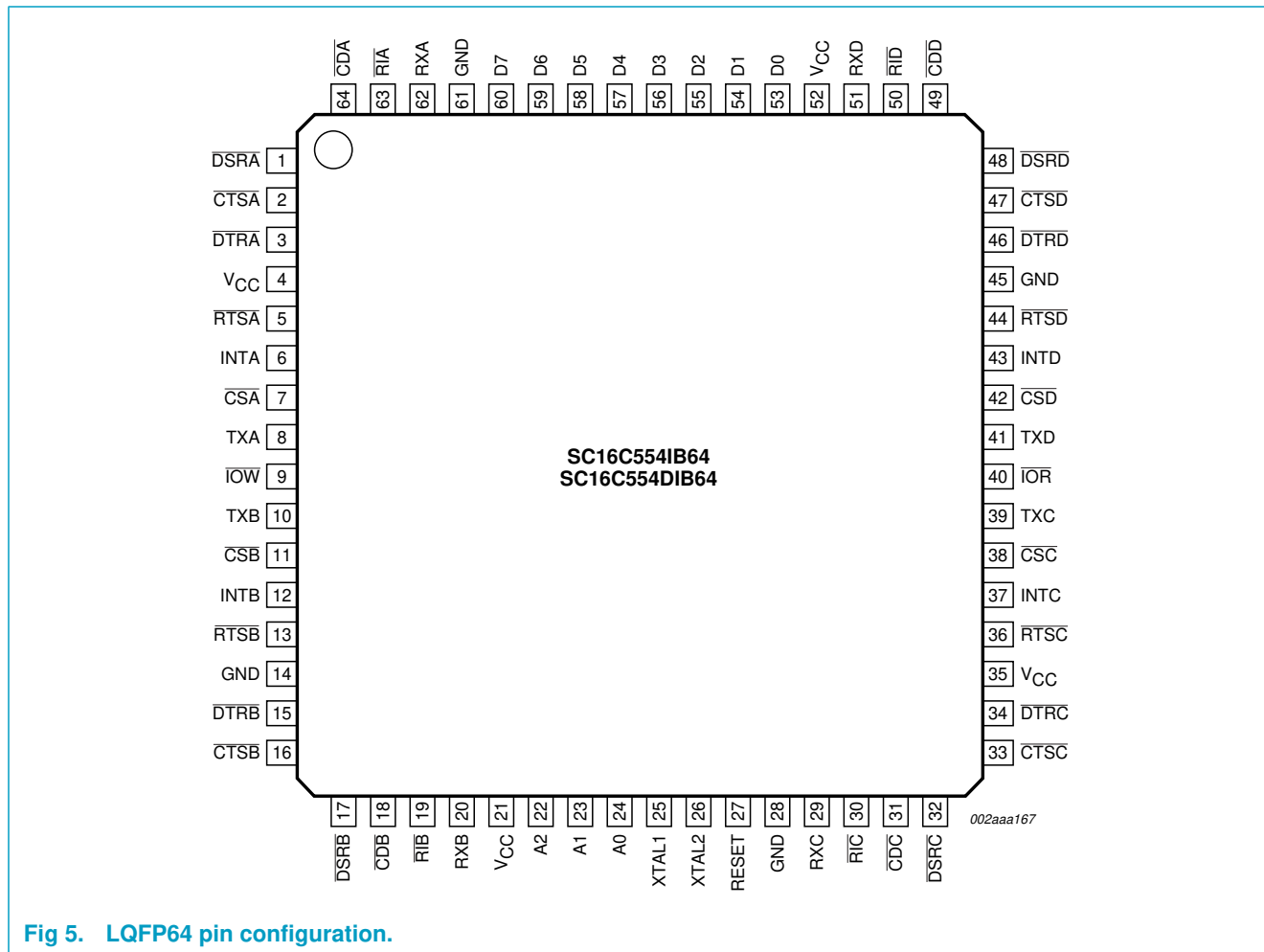


Fig 5. LQFP64 pin configuration.



5.1.3 LQFP80

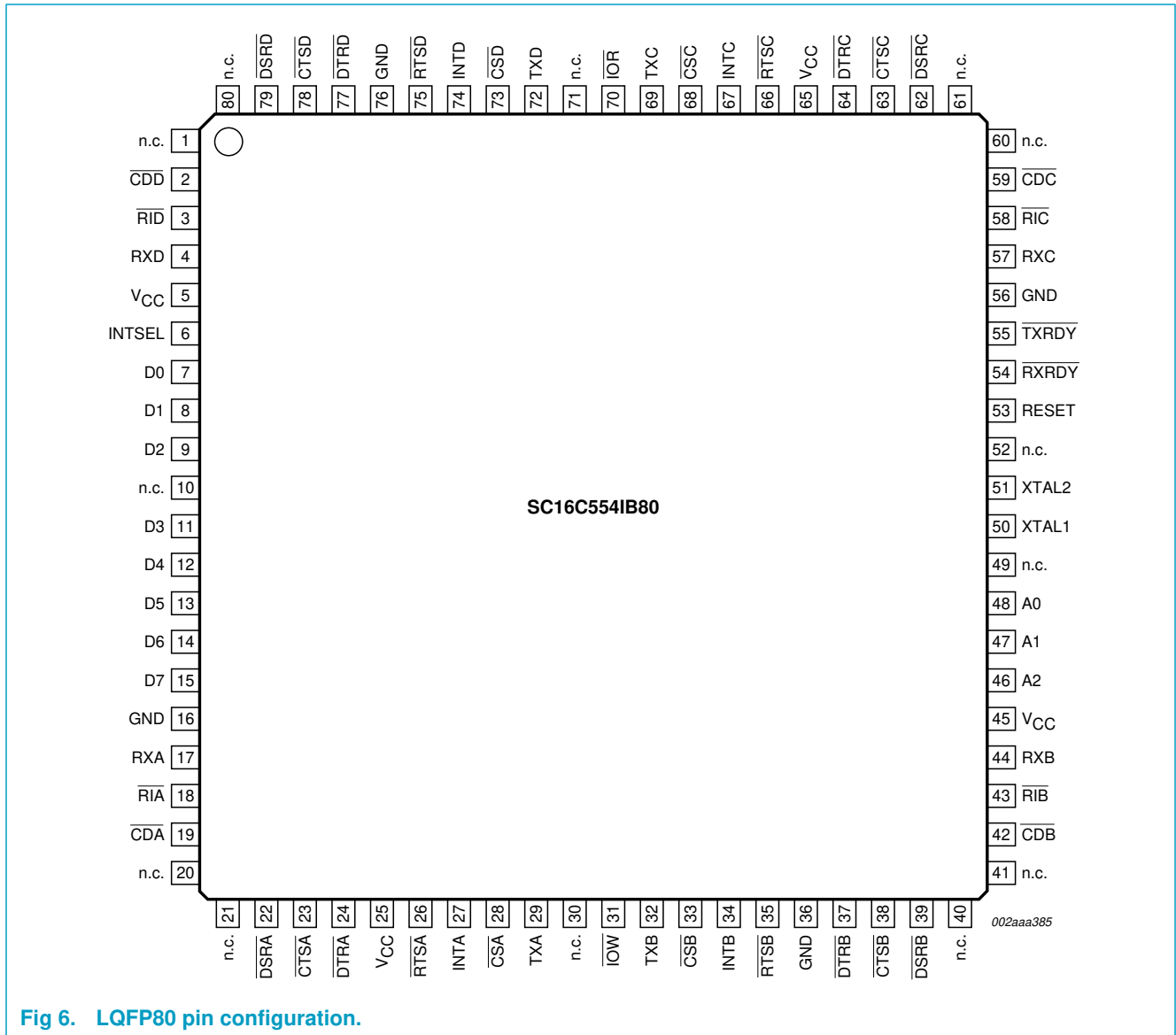


Fig 6. LQFP80 pin configuration.

## 5.2 Pin description

Table 2: Pin description

| Symbol   | Pin               |                   |                   | Type | Description  |
|--|-------------------|-------------------|-------------------|------|--|
|  | PLCC68            | LQFP64            | LQFP80            |      |  |
| 16/68  | 31                | -                 | -                 | I    | <b>16/68 Interface type select (input with internal pull-up).</b> This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of $\overline{\text{IOR}}$ , $\overline{\text{IOW}}$ , INTA-INTD, and $\overline{\text{CSA-CSD}}$ are re-assigned with the logical state of this pin. When this pin is a logic 1, the 16 mode interface (16C554) is selected. When this pin is a logic 0, the 68 mode interface (68C554) is selected. When this pin is a logic 0, $\overline{\text{IOW}}$ is re-assigned to R/W, RESET is re-assigned to $\overline{\text{RESET}}$ , $\overline{\text{IOR}}$ is not used, and INTA-INTD are connected in a wire-OR configuration. The wire-OR outputs are connected internally to the open drain IRQ signal output. This pin is not available on 64-pin packages which operate in the 16 mode only. |
| A0   | 34                | 24                | 48                | I    | <b>Address 0 select bit.</b> Internal registers address selection in 16 and 68 modes.  |
| A1   | 33                | 23                | 47                | I    | <b>Address 1 select bit.</b> Internal registers address selection in 16 and 68 modes.  |
| A2   | 32                | 22                | 46                | I    | <b>Address 2 select bit.</b> Internal registers address selection in 16 and 68 modes.  |
| A3, A4   | 20, 50            | -                 | -                 | I    | <b>Address 3-4 select bits.</b> When the 68 mode is selected, these pins are used to address or select individual UARTs (providing $\overline{\text{CS}}$ is a logic 0). In the 16 mode, these pins are re-assigned as chip selects, see $\overline{\text{CSB}}$ and $\overline{\text{CSC}}$ .   |
| $\overline{\text{CDA}}$ , $\overline{\text{CDB}}$ ,<br>$\overline{\text{CDC}}$ , $\overline{\text{CDD}}$     | 9, 27,<br>43, 61  | 64, 18,<br>31, 49 | 19, 42,<br>59, 2  | I    | <b>Carrier Detect (Active-LOW).</b> These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.   |
| $\overline{\text{CS}}$   | 16                | -                 | -                 | I    | <b>Chip Select (Active-LOW).</b> In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UARTs (A-D) are enabled when the $\overline{\text{CS}}$ pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3-A4. when the 16 mode is selected (68-pin devices), this pin functions as $\overline{\text{CSA}}$ (see definition under $\overline{\text{CSA}}$ , $\overline{\text{CSB}}$ ).   |
| $\overline{\text{CSA}}$ , $\overline{\text{CSB}}$ ,<br>$\overline{\text{CSC}}$ , $\overline{\text{CSD}}$     | 16, 20,<br>50, 54 | 7, 11,<br>38, 42  | 28, 33,<br>68, 73 | I    | <b>Chip Select A, B, C, D (Active-LOW).</b> This function is associated with the 16 mode only, and for individual channels 'A' through 'D'. When in 16 mode, these pins enable data transfers between the user CPU and the SC16C554/554D for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective $\overline{\text{CSA-CSD}}$ pin. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.  |
| $\overline{\text{CTSA}}$ , $\overline{\text{CTSB}}$ ,<br>$\overline{\text{CTSC}}$ , $\overline{\text{CTSD}}$ | 11, 25,<br>45, 59 | 2, 16,<br>33, 47  | 23, 38,<br>63, 78 | I    | <b>Clear to Send (Active-LOW).</b> These inputs are associated with individual UART channels A through D. A logic 0 on the $\overline{\text{CTS}}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C554/554D. Status can be tested by reading MSR[4]. This pin only affects the transmit or receive operations when Auto CTS function is enabled via the Enhanced Feature Register EFR[7] for hardware flow control operation.   |

Table 2: Pin description...continued

| Symbol                       | Pin               |                   |                   | Type | Description   |
|------------------------------|-------------------|-------------------|-------------------|------|---|
|                              | PLCC68            | LQFP64            | LQFP80            |      |   |
| D0-D2,<br>D3-D7              | 66-68,<br>1-5     | 53-55,<br>56-60   | 7-9,<br>11-15     | I/O  | <b>Data bus (bi-directional).</b> These pins are the 8-bit, 3-State data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.   |
| DSRA,<br>DSRB,<br>DSRC, DSRD | 10, 26,<br>44, 60 | 1, 17,<br>32, 48  | 22, 39,<br>62, 79 | I    | <b>Data Set Ready (Active-LOW).</b> These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.   |
| DTRA,<br>DTRB,<br>DTRC, DTRD | 12, 24,<br>46, 58 | 3, 15,<br>34, 46  | 24, 37,<br>64, 77 | O    | <b>Data Terminal Ready (Active-LOW).</b> These outputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the SC16C554/554D is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation.  |
| GND                          | 6, 23,<br>40, 57  | 14, 28,<br>45, 61 | 16, 36,<br>56, 76 | I    | <b>Signal and power ground.</b>   |
| INTA, INTB,<br>INTC, INTD    | 15, 21,<br>49, 55 | 6, 12,<br>37, 43  | 27, 34,<br>67, 74 | O    | <b>Interrupt A, B, C, D (Active-HIGH).</b> This function is associated with the 16 mode only. These pins provide individual channel interrupts INTA-INTD. INTA-INTD are enabled when MCR[3] is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.   |
| INTSEL                       | 65                | -                 | 6                 | I    | <b>Interrupt Select (Active-HIGH, with internal pull-down).</b> This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR[3] to enable or disable the 3-State interrupts, INTA-INTD, or override MCR[3] and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR[3] to control the 3-State interrupt output. In this mode, MCR[3] is set to a logic 1 to enable the 3-State outputs. This pin is disabled in the 68 mode. Due to pin limitations on the 64-pin packages, this pin is not available. To cover this limitation, the SC16C654DIB64 version operates in the continuous interrupt enable mode by bonding this pin to V <sub>CC</sub> internally. The SC16C654IB64 operates with MCR[3] control by bonding this pin to GND. |
| I $\overline{O}R$            | 52                | 40                | 70                | I    | <b>Input/Output Read strobe (Active-LOW).</b> This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an internal register defined by address bits A0-A2 onto the SC16C554/554D data bus (D0-D7) for access by external CPU. This pin is disabled in the 68 mode.   |

Table 2: Pin description...continued

| Symbol   | Pin                          |                   |   | Type | Description   |
|--|------------------------------|-------------------|---|------|---|
|  | PLCC68                       | LQFP64            | LQFP80  |      |   |
| $\overline{IOW}$   | 18                           | 9                 | 31  | I    | <b>Input/Output Write strobe (Active-LOW).</b> This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2. When the 68 mode is selected, this pin functions as $R/\overline{W}$ (see definition under $R/\overline{W}$ ).   |
| $\overline{IRQ}$   | 15                           | -                 | -   | O    | <b>Interrupt Request or Interrupt 'A'.</b> This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A-D are wire-ORed internally to function as a single $\overline{IRQ}$ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using CS and A3-A4. In the 68 mode, an external pull-up resistor must be connected between this pin and $V_{CC}$ . The function of this pin changes to INTA when operating in the 16 mode (see definition under INTA). |
| n.c.   | 21, 49,<br>52, 54,<br>55, 65 | -                 | 1, 10,<br>20, 21,<br>30, 40,<br>41, 49,<br>52, 60,<br>61, 71,<br>80 | -    | Not connected.  |
| $\overline{RESET}$<br>(RESET)  | 37                           | 27                | 53  | I    | <b>Reset.</b> In the 16 mode, a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See <a href="#">Section 7.11 "SC16C554/554D external reset conditions"</a> for initialization details.) When 16/68 is a logic 0 (68 mode), this pin functions similarly, but as an inverted reset interface signal, $\overline{RESET}$ .   |
| $\overline{RIA}$ , $\overline{RIB}$ ,<br>$\overline{RIC}$ , $\overline{RID}$     | 8, 28,<br>42, 62             | 63, 19,<br>30, 50 | 18, 43,<br>58, 3  | I    | <b>Ring Indicator (Active-LOW).</b> These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.   |
| $\overline{RTSA}$ , $\overline{RTSB}$ ,<br>$\overline{RTSC}$ , $\overline{RTSD}$ | 14, 22,<br>48, 56            | 5, 13,<br>36, 44  | 26, 35,<br>66, 75   | O    | <b>Request to Send (Active-LOW).</b> These outputs are associated with individual UART channels, A through D. A logic 0 on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when Auto RTS function is enabled via the Enhanced Feature Register (EFR[6]) for hardware flow control operation.   |
| $R/\overline{W}$   | 18                           | -                 | -   | I    | <b>Read/Write strobe.</b> This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes.<br>Logic 1 = Read from UART register selected by $\overline{CS}$ and A0-A4.<br>Logic 0 = Write to UART register selected by $\overline{CS}$ and A0-A4.   |

Table 2: Pin description...continued

| Symbol                    | Pin               |                   |                   | Type | Description  |
|---------------------------|-------------------|-------------------|-------------------|------|--|
|                           | PLCC68            | LQFP64            | LQFP80            |      |  |
| RXA, RXB,<br>RXC, RXD     | 7, 29,<br>41, 63  | 62, 20,<br>29, 51 | 17, 44,<br>57, 4  | I    | <b>Receive data input RXA-RXD.</b> These inputs are associated with individual serial channel data to the SC16C554/554D. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is connected to the UART RX input internally.  |
| $\overline{\text{RXRDY}}$ | 38                | -                 | 54                | O    | <b>Receive Ready (Active-LOW).</b> $\overline{\text{RXRDY}}$ contains the wire-ORed status of all four receive channel FIFOs, RXRDYA-RXRDYD. A logic 0 indicates receive data ready status, i.e., the RHR is full, or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is empty, or when there are no more characters available in either the FIFO or RHR. Individual channel RX status is read by examining individual internal registers via $\overline{\text{CS}}$ and A0-A4 pin functions. |
| TXA, TXB,<br>TXC, TXD     | 17, 19,<br>51, 53 | 8, 10,<br>39, 41  | 29, 32,<br>69, 72 | O    | <b>Transmit data A, B, C, D.</b> These outputs are associated with individual serial transmit channel data from the SC16C554/554D. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.   |
| $\overline{\text{TXRDY}}$ | 39                | -                 | 55                | O    | <b>Transmit Ready (Active-LOW).</b> $\overline{\text{TXRDY}}$ contains the wire-ORed status of all four transmit channel FIFOs, TXRDYA-TXRDYD. A logic 0 indicates a buffer ready status, i.e., at least one location is empty and available in one of the TX channels (A-D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR. Individual channel TX status can be read by examining individual internal registers via $\overline{\text{CS}}$ and A0-A4 pin functions.                                |
| V <sub>CC</sub>           | 13, 30,<br>47, 64 | 4, 21,<br>35, 52  | 5, 25,<br>45, 65  | I    | <b>Power supply inputs.</b>  |
| XTAL1                     | 35                | 25                | 50                | I    | <b>Crystal or external clock input.</b> Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see Figure 7). Alternatively, an external clock can be connected to this pin to provide custom data rates. (See Section 6.10 "Programmable baud rate generator".)  |
| XTAL2                     | 36                | 26                | 51                | O    | <b>Output of the crystal oscillator or buffered clock.</b> (See also XTAL1.) Crystal oscillator output or buffered clock output.   |

## 6. Functional description

The SC16C554/554D provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C554/554D represents such an integration with greatly enhanced features. The SC16C554/554D is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C554/554D is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C454. The SC16C554/554D is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C554/554D by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C554/554DAI68 combines the package interface modes of the 16C454/554 and 68C454/554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel-type of microprocessor bus, while the 68 mode is intended to operate with Motorola and other popular microprocessors. Following a reset, the SC16C554/554DAI68 is downward compatible with the 16C454/554 or the 68C454/554, dependent on the state of the interface mode selection pin, 16/68.

The SC16C554/554D is capable of operation to 1.5 Mbit/s with a 24 MHz crystal and up to 5 Mbit/s with an external clock input (at 3.3 V and 5 V; at 2.5 V the maximum speed is 3 Mbit/s).

The rich feature set of the SC16C554/554D is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. In the 16 mode, INTSEL and MCR[3] can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations of the 64-pin package, this feature is offered by two different LQFP64 packages. The SC16C554D operates in the continuous interrupt enable mode by bonding INTSEL to V<sub>CC</sub> internally. The SC16C554 operates in conjunction with MCR[3] by bonding INTSEL to GND internally.



## 6.1 Interface options

Two user interface modes are selectable for the PLCC68 package. These interface modes are designated as the '16 mode' and the '68 mode'. This nomenclature corresponds to the early 16C454/554 and 68C454/554 package interfaces respectively.

## 6.2 The 16 mode interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C454/554. In the 16 mode (pin 16/ $\overline{68}$  = logic 1), each UART is selected with individual chip select ( $\overline{CS}_x$ ) pins, as shown in [Table 3](#).

**Table 3:** Serial port channel selection, 16 mode interface

| $\overline{CS}_A$ | $\overline{CS}_B$ | $\overline{CS}_C$ | $\overline{CS}_D$ | UART channel |
|-------------------|-------------------|-------------------|-------------------|--------------|
| 1                 | 1                 | 1                 | 1                 | none         |
| 0                 | 1                 | 1                 | 1                 | A            |
| 1                 | 0                 | 1                 | 1                 | B            |
| 1                 | 1                 | 0                 | 1                 | C            |
| 1                 | 1                 | 1                 | 0                 | D            |

## 6.3 The 68 mode interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode, the SC16C554/554D decodes two additional addresses, A3-A4, to select one of the four UART ports. The A3-A4 address decode function is used only when in the 68 mode (16/ $\overline{68}$  = logic 0), and is shown in [Table 4](#).

**Table 4:** Serial port channel selection, 68 mode interface

| $\overline{CS}$ | A4  | A3  | UART channel |
|-----------------|-----|-----|--------------|
| 1               | n/a | n/a | none         |
| 0               | 0   | 0   | A            |
| 0               | 0   | 1   | B            |
| 0               | 1   | 0   | C            |
| 0               | 1   | 1   | D            |

## 6.4 Internal registers

The SC16C554/554D provides 17 internal registers for monitoring and control. These registers are shown in Table 5. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR). Beyond the general 16C554 features and capabilities, the SC16C554/554D offers an enhanced feature register set (EFR, Xon/Xoff1-2) that provides on-board hardware/software flow control. Register functions are more fully described in the following paragraphs.

**Table 5: Internal registers decoding**

| A2   | A1 | A0 | READ mode                 | WRITE mode                |
|--|----|----|---------------------------|---------------------------|
| <b>General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)<sup>[1]</sup></b> |    |    |                           |                           |
| 0  | 0  | 0  | Receive Holding Register  | Transmit Holding Register |
| 0  | 0  | 1  | Interrupt Enable Register | Interrupt Enable Register |
| 0  | 1  | 0  | Interrupt Status Register | FIFO Control Register     |
| 0  | 1  | 1  | Line Control Register     | Line Control Register     |
| 1  | 0  | 0  | Modem Control Register    | Modem Control Register    |
| 1  | 0  | 1  | Line Status Register      | n/a                       |
| 1  | 1  | 0  | Modem Status Register     | n/a                       |
| 1  | 1  | 1  | Scratchpad Register       | Scratchpad Register       |
| <b>Baud rate register set (DLL/DLM)<sup>[2]</sup></b>                                |    |    |                           |                           |
| 0  | 0  | 0  | LSB of Divisor Latch      | LSB of Divisor Latch      |
| 0  | 0  | 1  | MSB of Divisor Latch      | MSB of Divisor Latch      |
| <b>Enhanced register set (EFR, Xon/off 1-2)<sup>[3]</sup></b>                        |    |    |                           |                           |
| 0  | 1  | 0  | Enhanced Feature Register | Enhanced Feature Register |
| 1  | 0  | 0  | Xon1 word                 | Xon1 word                 |
| 1  | 0  | 1  | Xon2 word                 | Xon2 word                 |
| 1  | 1  | 0  | Xoff1 word                | Xoff1 word                |
| 1  | 1  | 1  | Xoff2 word                | Xoff2 word                |

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Enhanced Feature Register, Xon1, 2 and Xoff1, 2 are accessible only when the LCR is set to 'BF' (HEX).

## 6.5 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. With SC16C554 devices, the user can set the receive trigger level, but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 6: Flow control mechanism

| Selected trigger level (characters) | INT pin activation | Negate $\overline{\text{RTS}}$ or send Xoff | Assert $\overline{\text{RTS}}$ or send Xon |
|-------------------------------------|--------------------|---|--|
| 1                                   | 1                  | 4   | 1  |
| 4                                   | 4                  | 8   | 4  |
| 8                                   | 8                  | 12  | 8  |
| 14                                  | 14                 | 14  | 10   |

## 6.6 Hardware flow control

When automatic hardware flow control is enabled, the SC16C554/554D monitors the  $\overline{\text{CTS}}$  pin for a remote buffer overflow indication and controls the  $\overline{\text{RTS}}$  pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] ( $\overline{\text{RTS}}$ ) and EFR[7] ( $\overline{\text{CTS}}$ ) to a logic 1. If  $\overline{\text{CTS}}$  transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[6,7]), and the SC16C554/554D will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the  $\overline{\text{CTS}}$  input returns to a logic 0, indicating more data may be sent.

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The  $\overline{\text{RTS}}$  pin will not be forced to a logic 1 ( $\overline{\text{RTS}}$  off), until the receive FIFO reaches the next trigger level. However, the  $\overline{\text{RTS}}$  pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger. However, under the above described conditions, the SC16C554/554D will continue to accept data until the receive FIFO is full.

## 6.7 Software flow control

When software flow control is enabled, the SC16C554/554D compares one or two sequential receive data characters with the programmed Xon/Xoff or Xoff1,2 character value(s). If received character(s) match the programmed values, the SC16C554/554D will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER[5]) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16C554/554D will monitor the receive data stream for a match to the Xon1,2 character value(s). If a match is found, the SC16C554/554D will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the SC16C554/554D compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the SC16C554/554D automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The SC16C554/554D sends the Xoff1,2

characters as soon as received data passes the programmed trigger level. To clear this condition, the SC16C554/554D will transmit the programmed Xon1,2 characters as soon as receive data drops below the programmed trigger level.

## 6.8 Special feature software flow control

A special feature is provided to detect an 8-bit character when EFR[5] is set. When 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[0-3]. Note that software flow control should be turned off when using this special mode by setting EFR[0-3] to a logic 0.

The SC16C554/554D compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although the Internal Register Table (Table 8) shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[0-1] define the number of character bits, i.e., either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[0-1] also determine the number of bits that will be used for the special character comparison. Bit 0 in the X-registers corresponds with the LSB bit for the receive character.

## 6.9 Hardware/software and time-out interrupts

Three special interrupts have been added to monitor the hardware and software flow control. The interrupts are enabled by IER[5-7]. Care must be taken when handling these interrupts. Following a reset, if the transmitter interrupt is enabled, the SC16C554/554D will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/TRS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C554/554D FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

In the 16 mode for the PLCC68 package, the system/board designer can optionally provide software controlled 3-State interrupt operation. This is accomplished by INTSEL and MCR[3]. When INTSEL interface pin is left open or made a logic 0, MCR[3] controls the 3-State interrupt outputs, INTA-INTD. When INTSEL is a logic 1, MCR[3] has no effect on the INTA-INTD outputs, and the package operates with interrupt outputs enabled continuously.

### 6.10 Programmable baud rate generator

The SC16C554/554D supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 80 MHz (for 3.3 V and 5 V operation), as required for supporting a 5 Mbit/s data rate. The SC16C554/554D can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 7). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 7).

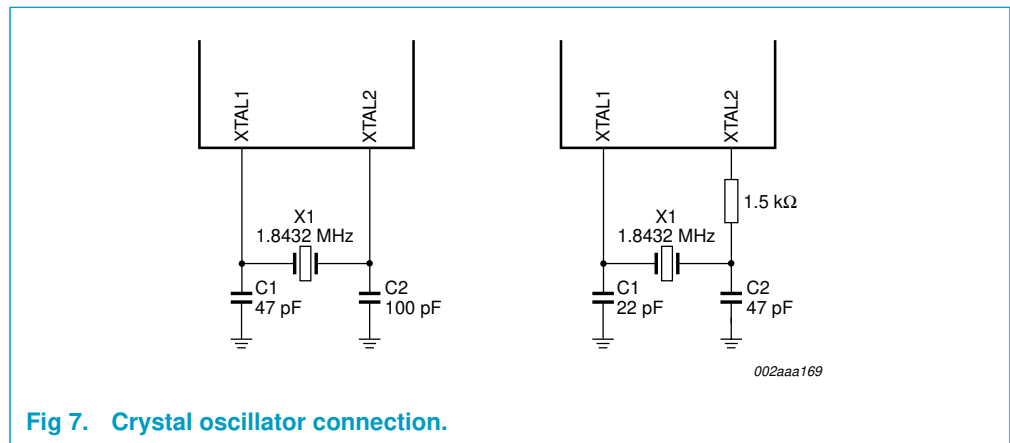


Fig 7. Crystal oscillator connection.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate.

Table 7: Baud rate generator programming table using a 7.3728 MHz clock

| Output baud rate | User 16× clock divisor |     | DLM program value (HEX) | DLL program value (HEX) |
|------------------|------------------------|-----|-------------------------|-------------------------|
|                  | Decimal                | HEX |                         |                         |
| 200              | 2304                   | 900 | 09                      | 00                      |
| 1200             | 384                    | 180 | 01                      | 80                      |
| 2400             | 192                    | C0  | 00                      | C0                      |
| 4800             | 96                     | 60  | 00                      | 60                      |
| 9600             | 48                     | 30  | 00                      | 30                      |
| 19.2 k           | 24                     | 18  | 00                      | 18                      |
| 38.4 k           | 12                     | 0C  | 00                      | 0C                      |
| 76.8 k           | 6                      | 06  | 00                      | 06                      |
| 153.6 k          | 3                      | 03  | 00                      | 03                      |
| 230.4 k          | 2                      | 02  | 00                      | 02                      |
| 460.8 k          | 1                      | 01  | 00                      | 01                      |

### 6.11 DMA operation

The SC16C554/554D FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[5,6] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C554/554D activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the SC16C554/554D sets the interrupt output pin when characters in the transmit FIFOs are below the transmit trigger level, or the characters in the receive FIFOs are above the receive trigger level.

### 6.12 Sleep mode

The SC16C554/554D is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. With EFR[4] and IER[4] enabled (set to a logic 1), the SC16C554/554D enters the sleep mode, but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins  $\overline{RX}$ ,  $\overline{RI}$ ,  $\overline{CTS}$ ,  $\overline{DSR}$ ,  $\overline{CD}$ , or a transmit data is provided by the user. If the sleep mode is enabled and the SC16C554/554D is awakened by one of the conditions described above, it will return to the sleep mode automatically after the last character is transmitted or read by the user. In any case, the sleep mode will not be entered while an interrupt(s) is pending. The SC16C554/554D will stay in the sleep mode of operation until it is disabled by setting IER[4] to a logic 0.

### 6.13 Loop-back mode

The internal loop-back capability allows on-board diagnostics. In the loop-back mode, the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR[0-3] register bits are used for controlling loop-back diagnostic testing. In the loop-back mode,  $\overline{OPT1}$  and  $\overline{OP2}$  in the MCR register (bits 2-3) control the modem  $\overline{RI}$  and  $\overline{CD}$  inputs, respectively. MCR signals  $\overline{DTR}$  and  $\overline{RTS}$  (bits 0-1) are used to control the modem  $\overline{DSR}$  and  $\overline{CTS}$  inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 8). The  $\overline{CTS}$ ,  $\overline{DSR}$ ,  $\overline{CD}$ , and  $\overline{RI}$  are disconnected from their normal modem control input pins, and instead are connected internally to  $\overline{RTS}$ ,  $\overline{DTR}$ ,  $\overline{OP2}$  and  $\overline{OPT1}$ . Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[0:3]) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.



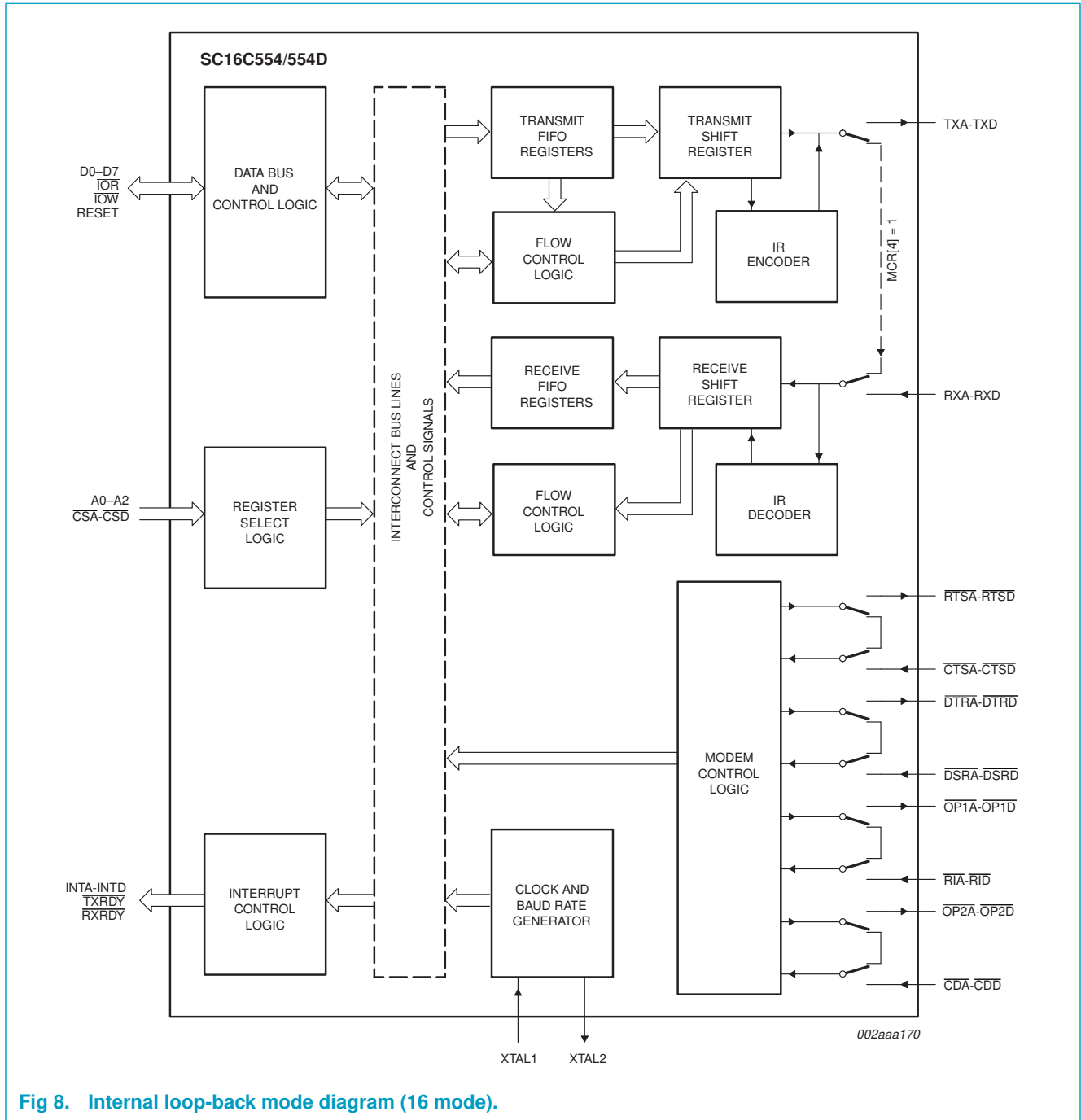


Fig 8. Internal loop-back mode diagram (16 mode).

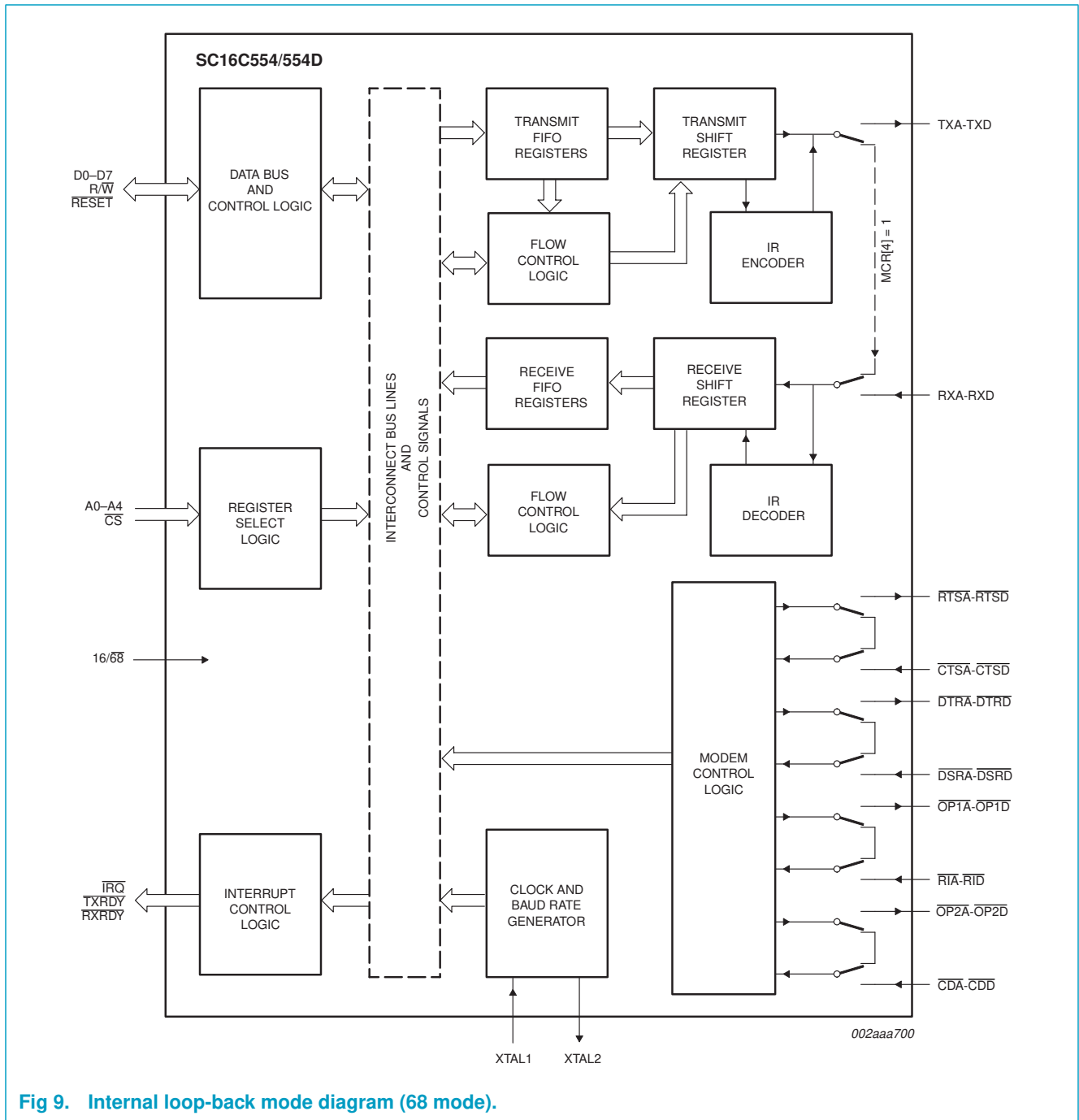


Fig 9. Internal loop-back mode diagram (68 mode).

## 7. Register descriptions

Table 8 details the assigned bit functions for the SC16C554/554D internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.11.

**Table 8: SC16C554/554D internal registers**

Shaded bits are only accessible when EFR[4] is set.

| A2   | A1 | A0 | Register | Default <sup>[1]</sup> | Bit 7                | Bit 6              | Bit 5                | Bit 4                             | Bit 3                  | Bit 2                         | Bit 1                     | Bit 0                    |
|--|----|----|----------|------------------------|----------------------|--------------------|----------------------|-----------------------------------|------------------------|-------------------------------|---------------------------|--------------------------|
| <b>General Register Set<sup>[2]</sup></b>  |    |    |          |                        |                      |                    |                      |                                   |                        |                               |                           |                          |
| 0  | 0  | 0  | RHR      | XX                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| 0  | 0  | 0  | THR      | XX                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| 0  | 0  | 1  | IER      | 00                     | CTS interrupt        | RTS interrupt      | Xoff interrupt       | Sleep mode                        | modem status interrupt | receive line status interrupt | transmit holding register | receive holding register |
| 0  | 1  | 0  | FCR      | 00                     | RCVR trigger (MSB)   | RCVR trigger (LSB) | reserved             | reserved                          | DMA mode select        | XMIT FIFO reset               | RCVR FIFO reset           | FIFO enable              |
| 0  | 1  | 0  | ISR      | 01                     | FIFOs enabled        | FIFOs enabled      | INT priority bit 4   | INT priority bit 3                | INT priority bit 2     | INT priority bit 1            | INT priority bit 0        | INT status               |
| 0  | 1  | 1  | LCR      | 00                     | divisor latch enable | set break          | set parity           | even parity                       | parity enable          | stop bits                     | word length bit 1         | word length bit 0        |
| 1  | 0  | 0  | MCR      | 00                     | 0                    | IR enable          | 0                    | loop back                         | OP2, INTx enable       | OP1                           | RTS                       | DTR                      |
| 1  | 0  | 1  | LSR      | 60                     | FIFO data error      | trans. empty       | trans. holding empty | break interrupt                   | framing error          | parity error                  | overrun error             | receive data ready       |
| 1  | 1  | 0  | MSR      | X0                     | CD                   | RI                 | DSR                  | CTS                               | $\Delta\overline{CD}$  | $\Delta\overline{RI}$         | $\Delta\overline{DSR}$    | $\Delta\overline{CTS}$   |
| 1  | 1  | 1  | SPR      | FF                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| <b>Special Register Set<sup>[3]</sup></b>  |    |    |          |                        |                      |                    |                      |                                   |                        |                               |                           |                          |
| 0  | 0  | 0  | DLL      | XX                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| 0  | 0  | 1  | DLM      | XX                     | bit 15               | bit 14             | bit 13               | bit 12                            | bit 11                 | bit 10                        | bit 9                     | bit 8                    |
| <b>Enhanced Register Set<sup>[4]</sup></b> |    |    |          |                        |                      |                    |                      |                                   |                        |                               |                           |                          |
| 0  | 1  | 0  | EFR      | 00                     | Auto CTS             | Auto RTS           | Special char. select | Enable IER[4:7], ISR[4:5], MCR[6] | Cont-3 Tx, Rx Control  | Cont-2 Tx, Rx Control         | Cont-1 Tx, Rx Control     | Cont-0 Tx, Rx Control    |
| 1  | 0  | 0  | Xon-1    | 00                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| 1  | 0  | 1  | Xon-2    | 00                     | bit 15               | bit 14             | bit 13               | bit 12                            | bit 11                 | bit 10                        | bit 9                     | bit 8                    |
| 1  | 1  | 0  | Xoff-1   | 00                     | bit 7                | bit 6              | bit 5                | bit 4                             | bit 3                  | bit 2                         | bit 1                     | bit 0                    |
| 1  | 1  | 1  | Xoff-2   | 00                     | bit 15               | bit 14             | bit 13               | bit 12                            | bit 11                 | bit 10                        | bit 9                     | bit 8                    |

[1] The value shown represents the register's initialized HEX value; X = n/a.

[2] These registers are accessible only when LCR[7] = 0.

[3] The Special Register set is accessible only when LCR[7] is set to a logic 1.

[4] Enhanced Feature Register, Xon-1,2 and Xoff-1,2 are accessible only when LCR is set to 'BF<sub>Hex</sub>'.

## 7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C554/554D and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After 7-1/2 clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

## 7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA-INTD output pins in the 16 mode, or on wire-OR IRQ output pin in the 68 mode.

**Table 9: Interrupt Enable Register bits description**

| Bit | Symbol | Description  |
|-----|--------|--|
| 7   | IER[7] | CTS interrupt.<br>Logic 0 = Disable the CTS interrupt (normal default condition).<br>Logic 1 = Enable the CTS interrupt. The SC16C554/554D issues an interrupt when the CTS pin transitions from a logic 0 to a logic 1.                                       |
| 6   | IER[6] | RTS interrupt.<br>Logic 0 = Disable the RTS interrupt (normal default condition).<br>Logic 1 = Enable the RTS interrupt. The SC16C554/554D issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1.                                       |
| 5   | IER[5] | Xoff interrupt.<br>Logic 0 = Disable the software flow control, receive Xoff interrupt (normal default condition).<br>Logic 1 = Enable the software flow control, receive Xoff interrupt. See <a href="#">Section 6.7 “Software flow control”</a> for details. |
| 4   | IER[4] | Sleep mode.<br>Logic 0 = Disable sleep mode (normal default condition).<br>Logic 1 = Enable sleep mode. See <a href="#">Section 6.12 “Sleep mode”</a> for details.   |
| 3   | IER[3] | Modem Status Interrupt.<br>Logic 0 = Disable the modem status register interrupt (normal default condition).<br>Logic 1 = Enable the modem status register interrupt.  |

**Table 9:** Interrupt Enable Register bits description...continued

| Bit | Symbol | Description  |
|-----|--------|--|
| 2   | IER[2] | Receive Line Status interrupt.<br>Logic 0 = Disable the receiver line status interrupt (normal default condition).<br>Logic 1 = Enable the receiver line status interrupt.   |
| 1   | IER[1] | Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1].<br>Logic 0 = Disable the transmitter empty interrupt (normal default condition).<br>Logic 1 = Enable the transmitter empty interrupt.   |
| 0   | IER[0] | Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation.<br>Logic 0 = Disable the receiver ready interrupt (normal default condition).<br>Logic 1 = Enable the receiver ready interrupt. |

### 7.2.1 IER versus Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

### 7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[0:3] enables the SC16C554/554D in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[1:4] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will indicate any FIFO data errors.

### 7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode.

#### 7.3.1 DMA mode

**Mode 0 (FCR bit 3 = 0):** Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C454 mode. Transmit Ready ( $\overline{\text{TXRDY}}$ ) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ( $\overline{\text{RXRDY}}$ ) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

**Mode 1 (FCR bit 3 = 1):** Set and enable the interrupt in a block mode operation. The transmit interrupt is set when there are one or more FIFO locations empty. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full.  $\overline{\text{RXRDY}}$  remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

#### 7.3.2 FIFO mode

**Table 10: FIFO Control Register bits description**

| Bit | Symbol   | Description   |
|-----|----------|---|
| 7:6 | FCR[7:6] | RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt.<br><br>An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to <a href="#">Table 11</a> .   |
| 5:4 | FCR[5:4] | Not used; initialized to logic 0.   |
| 3   | FCR[3]   | DMA mode select.<br><br>Logic 0 = Set DMA mode '0' (normal default condition).<br>Logic 1 = Set DMA mode '1'<br><br><b>Transmit operation in mode '0':</b> When the SC16C554/554D is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register.<br><br><b>Receive operation in mode '0':</b> When the SC16C554/554D is in mode '0' (FCR[0] = logic 0), or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ pin will go to a logic 1 when there are no more characters in the receiver. |