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SC16C654B/654DB

5 V, 3.3 V and 2.5 V quad UART, 5 Mbit/s (max.), with 64-byte FIFOs and infrared (IrDA) encoder/decoder

Rev. 02 — 20 June 2005 Product data sheet

1. General description

The SC16C654B/654DB is a Quad Universal Asynchronous Receiver and Transmitter (QUART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. It comes with an Intel or Motorola interface.

The SC16C654B/654DB is pin compatible with the ST16C654 and TL16C754 and it will power-up to be functionally equivalent to the 16C454. Programming of control registers enables the added features of the SC16C654B/654DB. Some of these added features are the 64-byte receive and transmit FIFOs, automatic hardware or software flow control and infrared encoding/decoding. The selectable auto-flow control feature significantly reduces software overload and increases system efficiency while in FIFO mode by automatically controlling serial data flow using $\overline{\text{RTS}}$ output and $\overline{\text{CTS}}$ input signals. The SC16C654B/654DB also provides DMA mode data transfers through FIFO trigger levels and the $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals. ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals are not available in the HVQFN48 package.) On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows on-board diagnostics.

The SC16C654B/654DB operates at 5 V, 3.3 V and 2.5 V, and the industrial temperature range, and is available in plastic PLCC68, LQFP64, HVQFN48 and LFBGA64 packages.

On the HVQFN48 package, only channel C has all the modem pins. Channel A and channel B have only $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ pins, and channel D does not have any modem pin.

2. Features

- 4 channel UART
- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range (–40 °C to +85 °C)
- SC16C654B is pin and software compatible with the industry-standard ST16C454/554, ST16C654, ST68C454/554, TL16C554
- SC16C654DB is pin and software compatible with ST16C654D, and software compatible with ST16C454/554, ST68C454/554, TL16C554
- Up to 5 Mbit/s data rate at 5 V and 3.3 V and 3 Mbit/s at 2.5 V
- 5 V tolerant inputs
- 64-byte transmit FIFO
- 64-byte receive FIFO with error flags
- Automatic software (Xon/Xoff)/hardware ($\overline{\text{RTS}}$/$\overline{\text{CTS}}$) flow control
- Programmable Xon/Xoff characters

- Software selectable baud rate generator
- Four selectable Receive and Transmit FIFO interrupt trigger levels
- Standard modem interface or infrared (IrDA) encoder/decoder interface
- Sleep mode
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5, 6, 7, or 8-bit characters
  - Even, Odd, or No Parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (DC to 5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bi-directional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, $\overline{\text{CD}}$).

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SC16C654BIA68	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SC16C654BIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
SC16C654BIBM	LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1
SC16C654BIBS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-3
SC16C654BIEC	LFBGA64	plastic low profile fine-pitch ball grid array package; 64 balls; body 6 × 6 × 1.05 mm	SOT686-1
SC16C654DBIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4. Block diagram

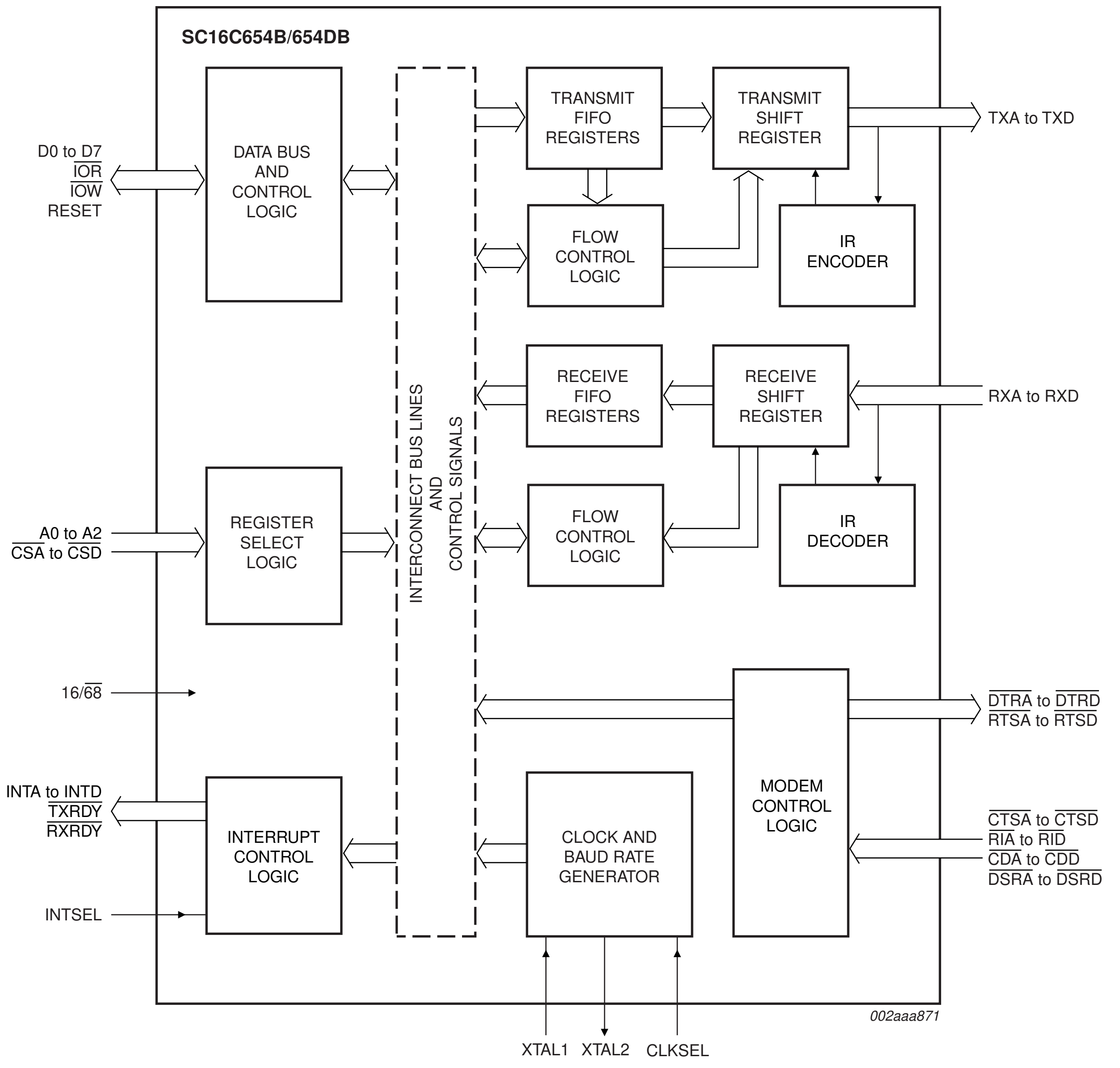

Fig 1. Block diagram of SC16C654B/654DB (16 mode)

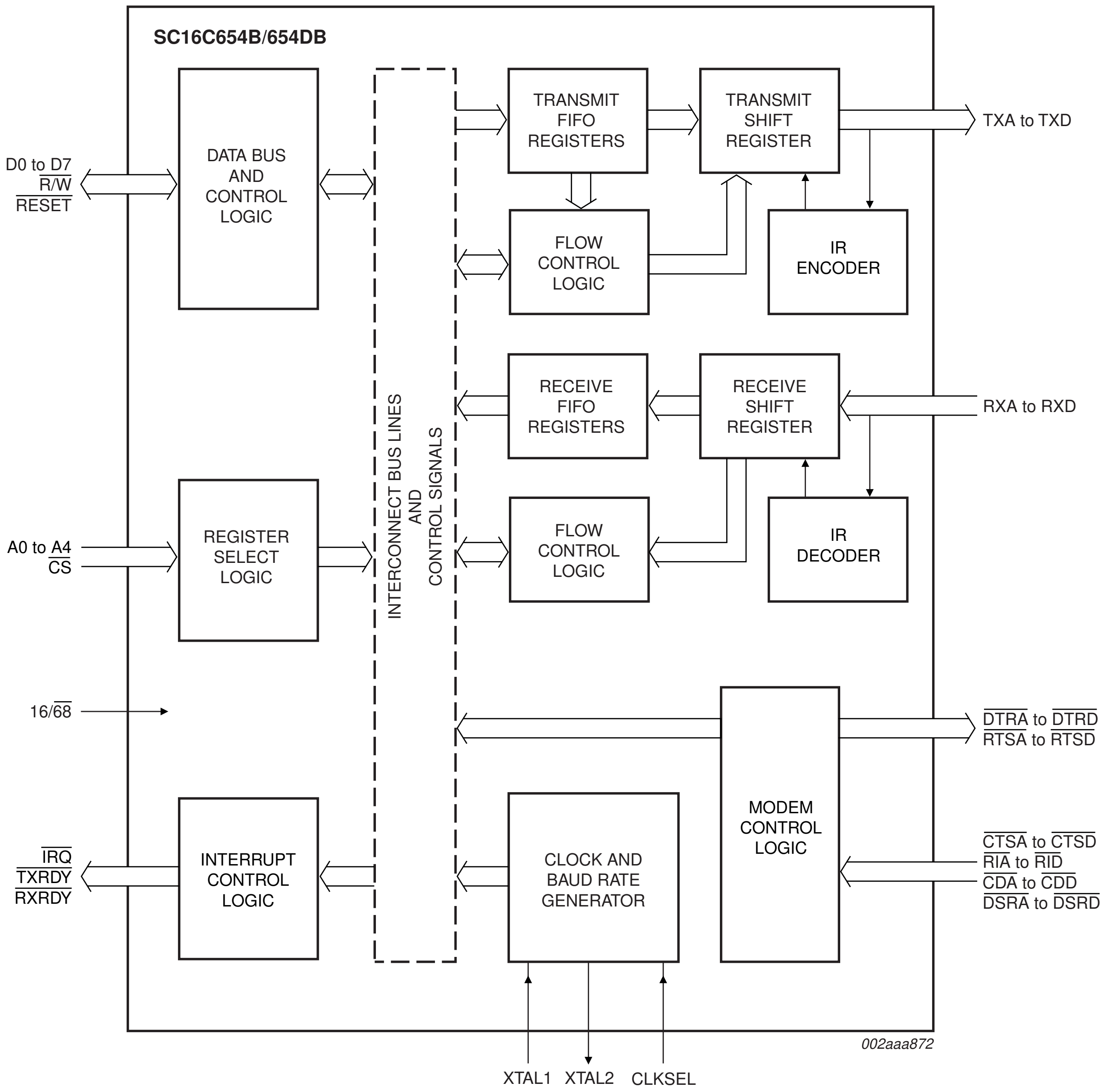

Fig 2. Block diagram of SC16C654B/654DB (68 mode)

5. Pinning information

5.1 Pinning

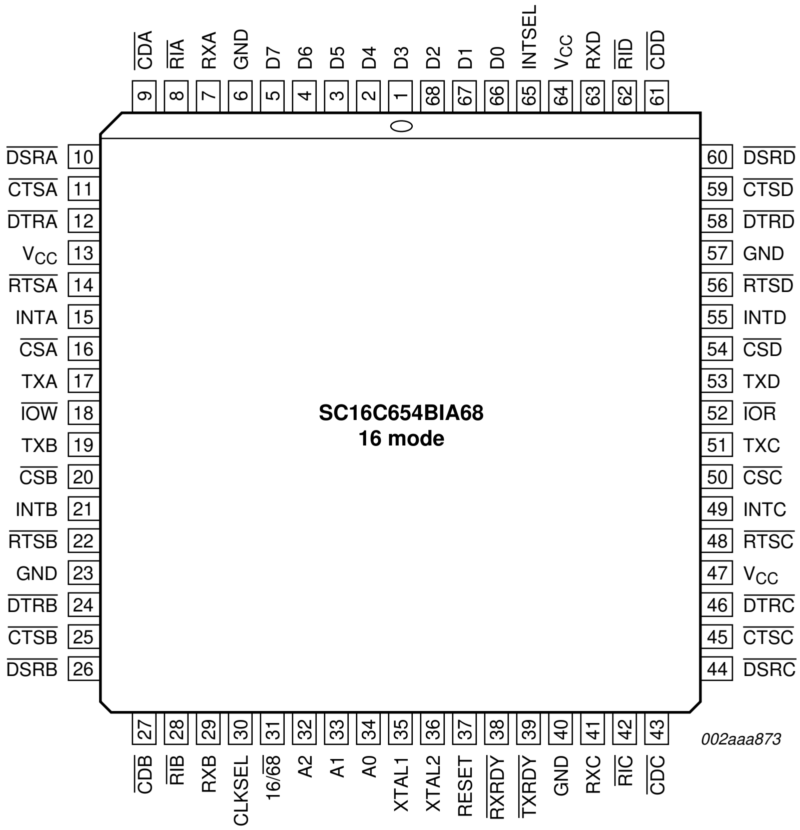

Fig 3. Pin configuration for PLCC68 (16 mode)

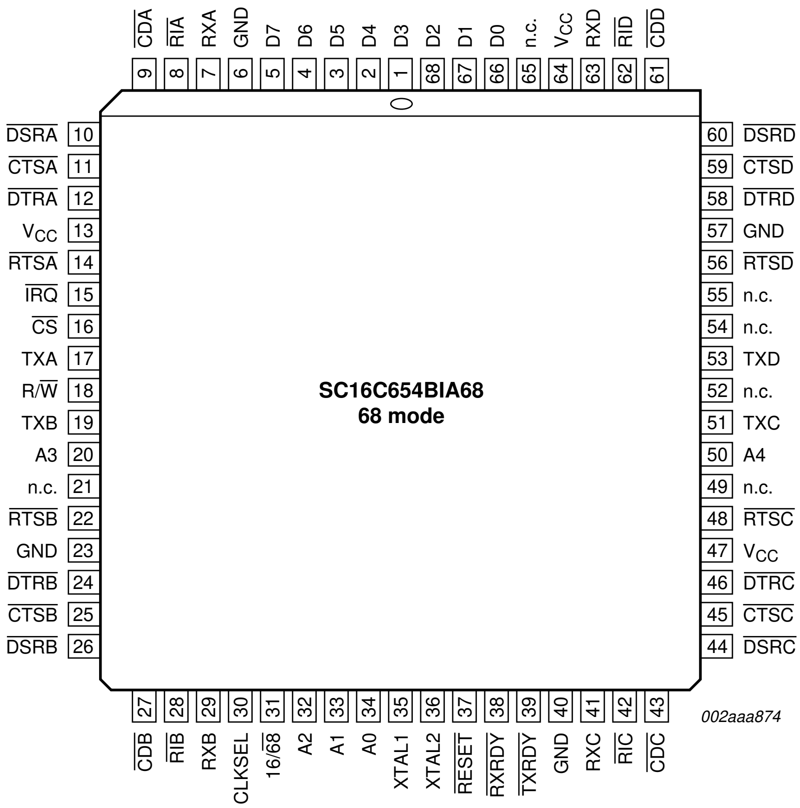

Fig 4. Pin configuration for PLCC68 (68 mode)

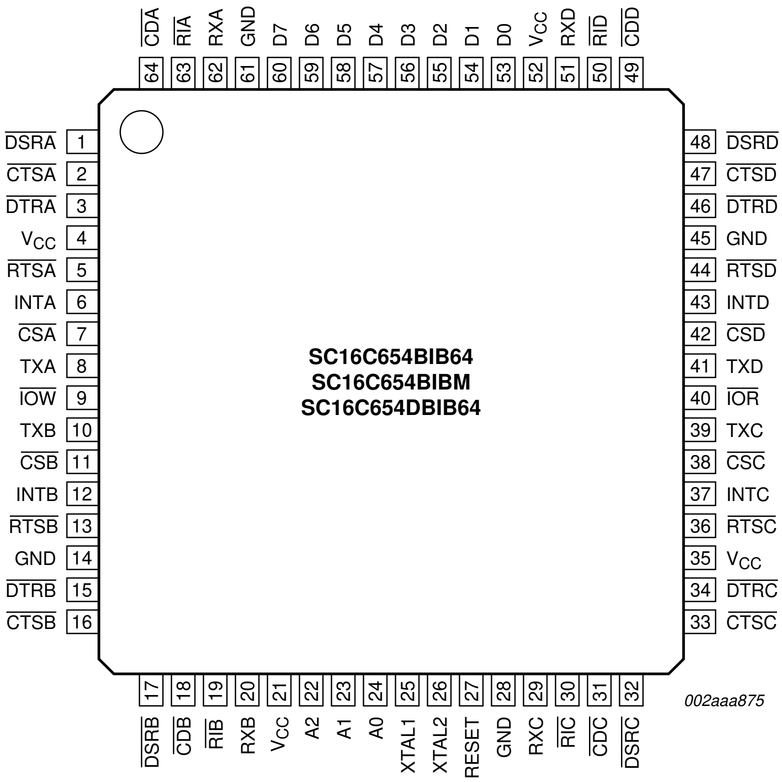

Fig 5. Pin configuration for LQFP64

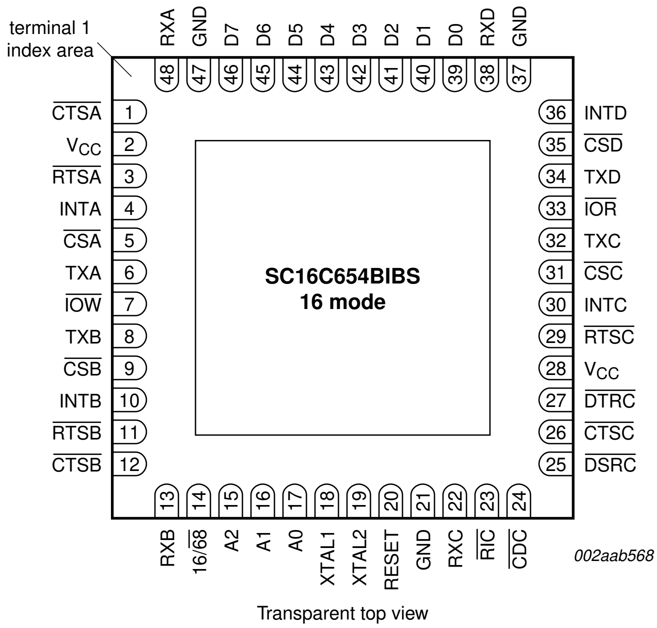

Fig 6. Pin configuration for HVQFN48 (16 mode)

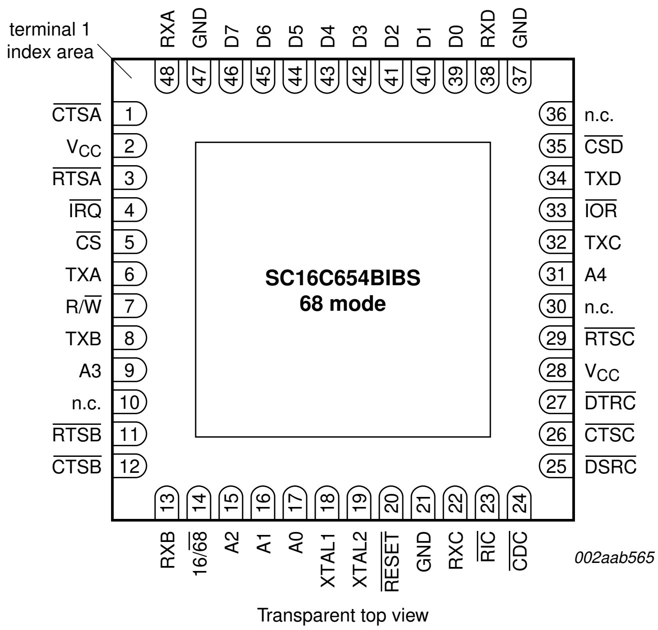

Fig 7. Pin configuration for HVQFN48 (68 mode)

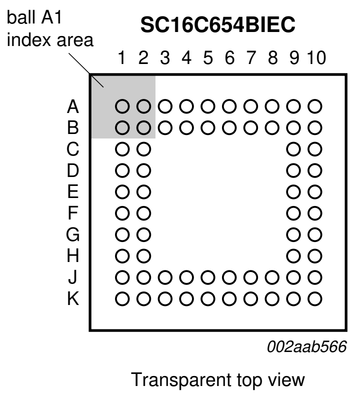

Fig 8. Pin configuration for LFBGA64

	1	2	3	4	5	6	7	8	9	10
A	$\overline{CDA}$	$\overline{RIA}$	RXA	D7	D5	D3	D1	V_{CC}	$\overline{RID}$	$\overline{CDD}$
B	$\overline{DSRA}$	V_{CC}	GND	D6	D4	D2	D0	RXD	$\overline{DSRD}$	$\overline{CTSD}$
C	$\overline{CTSA}$	$\overline{RTSA}$							$\overline{DTRD}$	$\overline{RTSD}$
D	$\overline{DTRA}$	INTA							GND	INTD
E	$\overline{CSA}$	TXA							$\overline{CSD}$	TXD
F	$\overline{IOW}$	TXB							$\overline{IOR}$	TXC
G	$\overline{CSB}$	INTB							$\overline{CSC}$	INTC
H	GND	$\overline{RTSB}$							$\overline{RTSC}$	V_{CC}
J	$\overline{DTRB}$	$\overline{CTSB}$	$\overline{RIB}$	V_{CC}	A1	XTAL1	RESET	RXC	$\overline{CDC}$	$\overline{DTRC}$
K	$\overline{DSRB}$	$\overline{CDB}$	RXB	A2	A0	XTAL2	GND	$\overline{RIC}$	$\overline{DSRC}$	$\overline{CTSC}$

002aab567

Fig 9. Ball mapping for LFBGA64

5.2 Pin description

Table 2: Pin description

Symbol	Pin				Type	Description
	PLCC68	LQFP64	HVQFN48	LFBGA64		
16/$\overline{68}$	31	-	14	-	I	**16/68 Interface type select (input with internal pull-up).** This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of $\overline{IOR}$, $\overline{IOW}$, INTA to INTD, and $\overline{CSA}$ to $\overline{CSD}$ are re-assigned with the logical state of this pin. When this pin is a logic 1, the 16 mode interface (16C654) is selected. When this pin is a logic 0, the 68 mode interface (68C654) is selected. When this pin is a logic 0, $\overline{IOW}$ is re-assigned to R/$\overline{W}$, RESET is re-assigned to $\overline{RESET}$, $\overline{IOR}$ is not used, and INTA to INTD are connected in a wire-OR configuration. The wire-OR outputs are connected internally to the open-drain IRQ signal output. This pin is not available on 64-pin packages which operate in the 16 mode only.
A0	34	24	17	K5	I	**Address 0 select bit.** Internal registers address selection in 16 and 68 modes.
A1	33	23	16	J5	I	**Address 1 select bit.** Internal registers address selection in 16 and 68 modes.
A2	32	22	15	K4	I	**Address 2 select bit.** Internal registers address selection in 16 and 68 modes.
A3	20	-	9	-	I	**Address 3, Address 4 select bits.** When the 68 mode is selected, these pins are used to address or select individual UARTs (providing $\overline{CS}$ is a logic 0). In the 16 mode, these pins are re-assigned as chip selects, see $\overline{CSB}$ and $\overline{CSC}$. These pins are not available on 64-pin packages which operate in the 16 mode only.
A4	50	-	31	-		
$\overline{CDA}$	9	64	-	A1	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	27	18	-	K2		
$\overline{CDC}$	43	31	24	J9		
$\overline{CDD}$	61	49	-	A10		
CLKSEL	30	-	-	-	I	**Clock Select.** The 1× or 4× pre-scalable clock is selected by this pin. The 1× clock is selected when CLKSEL is a logic 1 (connected to V_{CC}) or the 4× is selected when CLKSEL is a logic 0 (connected to GND). MCR[7] can override the state of this pin following reset or initialization (see MCR[7]). This pin is not available on 64-pin packages which provide MCR[7] selection only.
$\overline{CS}$	16	-	5	-	I	**Chip Select (active LOW).** In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UARTs (A to D) are enabled when the $\overline{CS}$ pin is a logic 0. An individual UART channel is selected by the data contents of address bits A[3:4]. when the 16 mode is selected (68-pin devices), this pin functions as $\overline{CSA}$ (see definition under $\overline{CSA}$, $\overline{CSB}$). This pin is not available on 64-pin packages which operate in the 16 mode only.

Table 2: Pin description *…continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	HVQFN48	LFBGA64		
$\overline{CSA}$	16	7	5	E1	I	**Chip Select A, B, C, D (active LOW).** This function is associated with the 16 mode only, and for individual channels 'A' through 'D'. When in 16 mode, these pins enable data transfers between the user CPU and the SC16C654B/654DB for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective $\overline{CSA}$ to $\overline{CSD}$ pin. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
$\overline{CSB}$	20	11	9	G1		
$\overline{CSC}$	50	38	31	G9		
$\overline{CSD}$	54	42	35	E9		
$\overline{CTSA}$	11	2	1	C1	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels A through D. A logic 0 on the $\overline{CTS}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C654B/654DB. Status can be tested by reading MSR[4]. This pin only affects the transmit or receive operations when Auto CTS function is enabled via the Enhanced Feature Register EFR[7] for hardware flow control operation.
$\overline{CTSB}$	25	16	12	J2		
$\overline{CTSC}$	45	33	26	K10		
$\overline{CTSD}$	59	47	-	B10		
D0 to D2, D3 to D7	66 to 68 , 1 to 5	53 to 55, 56 to 60	39 to 41, 42 to 46	B7, A7, B6, A6, B5, A5, B4, A4	I/O	**Data bus (bi-directional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$	10	1	-	B1	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
$\overline{DSRB}$	26	17	-	K1		
$\overline{DSRC}$	44	32	25	K9		
$\overline{DSRD}$	60	48	-	B9		
$\overline{DTRA}$	12	3	-	D1	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the SC16C654B/654DB is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTR}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation.
$\overline{DTRB}$	24	15	-	J1		
$\overline{DTRC}$	46	34	27	J10		
$\overline{DTRD}$	58	46	-	C9		
GND	6, 23, 40, 57	14, 28, 45, 61	21, 37, 47	B3, K7, H1, D9	I	**Signal and power ground.**
INTA	15	6	4	D2	O	**Interrupt A, B, C, D (active HIGH).** This function is associated with the 16 mode only. These pins provide individual channel interrupts INTA to INTD. INTA to INTD are enabled when MCR[3] is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
INTB	21	12	10	G2		
INTC	49	37	30	G10		
INTD	55	43	36	D10		

Table 2: Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	HVQFN48	LFBGA64		
INTSEL	65	-	-	-	I	**Interrupt Select (active HIGH, with internal pull-down).** This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR[3] to enable or disable the 3-state interrupts, INTA to INTD, or override MCR[3] and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR[3] to control the 3-state interrupt output. In this mode, MCR[3] is set to a logic 1 to enable the 3-state outputs. This pin is disabled in the 68 mode. Due to pin limitations on the 64-pin packages, this pin is not available. To cover this limitation, the SC16C654DBIB64 version operates in the continuous interrupt enable mode by bonding this pin to V_{CC} internally. The SC16C654BIB64 operates with MCR[3] control by bonding this pin to GND.
$\overline{IOR}$	52	40	33	F9	I	**Input/Output Read strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an internal register defined by address bits A[0:2] onto the SC16C654B/654DB data bus (D[0:7]) for access by external CPU. This pin is disabled in the 68 mode.
$\overline{IOW}$	18	9	7	F1	I	**Input/Output Write strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D[0:7]) from the external CPU to an internal register that is defined by address bits A[0:2]. When the 68 mode is selected (PLCC68), this pin functions as R/$\overline{W}$ (see definition under R/$\overline{W}$).
$\overline{IRQ}$	15	-	4	-	O	**Interrupt Request or Interrupt 'A'.** This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A-D are wire-ORed internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using CS and A[3:4]. In the 68 mode, and external pull-up resistor must be connected between this pin and V_{CC}. The function of this pin changes to INTA when operating in the 16 mode (see definition under INTA).
n.c.	21, 49, 52, 54, 55, 65	-	-	-	-	not connected
$\overline{RESET}$, RESET	37	27	20	J7	I	**Reset.** In the 16 mode, a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See Section 7.11 "SC16C654B/654DB external reset conditions" for initialization details.) When 16/$\overline{68}$ is a logic 0 (68 mode), this pin functions similarly, but as an inverted reset interface signal, $\overline{RESET}$.

Table 2: Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	HVQFN48	LFBGA64		
$\overline{RIA}$	8	63	-	A2	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
$\overline{RIB}$	28	19	-	J3		
$\overline{RIC}$	42	30	23	K8		
$\overline{RID}$	62	50	-	A9		
$\overline{RTSA}$	14	5	3	C2	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A through D. A logic 0 on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when Auto RTS function is enabled via the Enhanced Feature Register (EFR[6]) for hardware flow control operation.
$\overline{RTSB}$	22	13	11	H2		
$\overline{RTSC}$	48	36	29	H9		
$\overline{RTSD}$	56	44	-	C10		
R/$\overline{W}$	18	-	7	-	I	**Read/Write strobe.** This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes. Logic 1 = Read from UART register selected by $\overline{CS}$ and A[0:4]. Logic 0 = Write to UART register selected by $\overline{CS}$ and A[0:4].
RXA	7	62	48	A3	I	**Receive data input RXA-RXD.** These inputs are associated with individual serial channel data to the SC16C654B/654DB. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is connected to the UART RX input internally.
RXB	29	20	13	K3		
RXC	41	29	22	J8		
RXD	63	51	38	B8		
$\overline{RXRDY}$	38	-	-	-	O	**Receive Ready (active LOW).** This function is associated with 68-pin package only. $\overline{RXRDY}$ contains the wire-ORed status of all four receive channel FIFOs, RXRDYA-RXRDYD. A logic 0 indicates receive data ready status, that is, the RHR is full, or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is empty, or when there are no more characters available in either the FIFO or RHR. Individual channel RX status is read by examining individual internal registers via $\overline{CS}$ and A[0:4] pin functions.
TXA	17	8	6	E2	O	**Transmit data A, B, C, D.** These outputs are associated with individual serial transmit channel data from the SC16C654B/654DB. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.
TXB	19	10	8	F2		
TXC	51	39	32	F10		
TXD	53	41	34	E10		

Table 2: Pin description *…continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	HVQFN48	LFBGA64		
$\overline{TXRDY}$	39	-	-	-	O	**Transmit Ready (active LOW).** This function is associated with the 68-pin package only. $\overline{TXRDY}$ contains the wire-ORed status of all four transmit channel FIFOs, TXRDYA-TXRDYD. A logic 0 indicates a buffer ready status, that is, at least one location is empty and available in one of the TX channels (A to D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR. Individual channel TX status can be read by examining individual internal registers via $\overline{CS}$ and A[0:4] pin functions.
V_{CC}	13, 47, 64	4, 21, 35, 52	2, 28	A8, B2, J4, H10	I	**Power supply inputs.**
XTAL1	35	25	18	J6	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit; see Figure 10. Alternatively, an external clock can be connected to this pin to provide custom data rates; see Section 6.9 “Programmable baud rate generator”.
XTAL2	36	26	19	K6	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output.

6. Functional description

The SC16C654B/654DB provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C654B/654DB represents such an integration with greatly enhanced features. The SC16C654B/654DB is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C654B/654DB is an upward solution that provides 64 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16C554, or none in the 16C454. The SC16C654B/654DB is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C654B/654DB by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the SC16C554 with a 16-byte FIFO unloads 16 bytes of receive data in 1.53 ms. (This example uses a character length of 11 bits, including start/stop bits at 115.2 kbit/s.) This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However, with the 64-byte FIFO in the SC16C654B/654DB, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval, giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the four selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C654B/654DB combines the package interface modes of the 16C454/554 and 68C454/554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel-type of microprocessor bus, while the 68 mode is intended to operate with Motorola and other popular microprocessors. Following a reset, the SC16C654B/654DB is downward compatible with the 16C454/554 or the 68C454/554, dependent on the state of the interface mode selection pin, 16/$\overline{68}$.

The SC16C654B/654DB is capable of operation to 1.5 Mbit/s with a 24 MHz crystal and up to 5 Mbit/s with an external clock input (at 3.3 V and 5 V; at 2.5 V the max speed is 3 Mbit/s). With a crystal of 14.7464 MHz, and through a software option, the user can select data rates up to 460.8 kbit/s or 921.6 kbit/s, 8 times faster than the 16C554.

The rich feature set of the SC16C654B/654DB is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR[5] provides a facility for turning off (Xon) software flow control with any incoming (RX) character. In the 16 mode, INTSEL and MCR[3] can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations of the 64-pin package, this feature is offered by two different LQFP64 packages. The SC16C654DB operates in the continuous interrupt enable mode by bonding INTSEL to V_{CC} internally. The SC16C654B operates in conjunction with MCR[3] by bonding INTSEL to GND internally.

The PLCC68 SC16C654B package offers a clock select pin to allow system/board designers to preset the default baud rate table. The CLKSEL pin selects the 1× or 4× pre-scalable baud rate generator table during initialization, but can be overridden following initialization by MCR[7].

6.1 Interface options

Two user interface modes are selectable for the PLCC68 package. These interface modes are designated as the '16 mode' and the '68 mode'. This nomenclature corresponds to the early 16C454/554 and 68C454/554 package interfaces respectively.

6.1.1 The 16 mode interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C454/554. In the 16 mode (pin 16/$\overline{68}$ = logic 1), each UART is selected with individual chip select ($\overline{CS}$x) pins, as shown in Table 3.

Table 3: Serial port channel selection, 16 mode interface

$\overline{CSA}$	$\overline{CSB}$	$\overline{CSC}$	$\overline{CSD}$	UART channel
1	1	1	1	none
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

6.1.2 The 68 mode interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode, the SC16C654B/654DB decodes two additional addresses, A3-A4, to select one of the four UART ports. The A[3:4] address decode function is used only when in the 68 mode (16/$\overline{68}$ = logic 0), and is shown in Table 4.

Table 4: Serial port channel selection, 68 mode interface

$\overline{CS}$	A4	A3	UART channel
1	n/a	n/a	none
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

6.2 Internal registers

The SC16C654B/654DB provides 17 internal registers for monitoring and control. These registers are shown in Table 5. Twelve registers are similar to those already available in the standard 16C554. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR). Beyond the general 16C554 features and capabilities, the SC16C654B/654DB offers an enhanced feature register set (EFR, Xon/Xoff1-2) that provides on-board hardware/software flow control. Register functions are more fully described in the following paragraphs.

Table 5: Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR) [1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM) [2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Enhanced register set (EFR, Xon/off 1-2) [3]				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon1 word	Xon1 word
1	0	1	Xon2 word	Xon2 word
1	1	0	Xoff1 word	Xoff1 word
1	1	1	Xoff2 word	Xoff2 word

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Enhanced Feature Register, Xon1, 2 and Xoff1, 2 are accessible only when the LCR is set to ‘BFh’.

6.3 FIFO operation

The 64-byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. With SC16C554 devices, the user can set the receive trigger level, but not the transmit trigger level. The SC16C654B/654DB provides independent trigger levels for both receiver and transmitter. To remain compatible with SC16C554, the transmit interrupt trigger level is set to 8 following a reset. It should be noted that the user can set the transmit trigger levels by writing to the FCR register, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive

Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached. (For a description of this timing, see Section 6.4 “Hardware flow control”.)

Table 6: RX trigger levels

Selected trigger level (characters)	INT pin activation	Negate $\overline{RTS}$ or send Xoff (characters)	Assert $\overline{RTS}$ or send Xon (characters)
8	8	16	0
16	16	56	8
56	56	60	16
60	60	60	56

6.4 Hardware flow control

When automatic hardware flow control is enabled, the SC16C654B/654DB monitors the $\overline{CTS}$ pin for a remote buffer overflow indication and controls the $\overline{RTS}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If $\overline{CTS}$ transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[6,7]), and the SC16C654B/654DB will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTS}$ input returns to a logic 0, indicating more data may be sent.

With the Auto $\overline{RTS}$ function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{RTS}$ pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the $\overline{RTS}$ pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger. However, under the above described conditions, the SC16C654B/654DB will continue to accept data until the receive FIFO is full.

Remark: Hardware flow control is not supported on channel D in the HVQFN48 package.

6.5 Software flow control

When software flow control is enabled, the SC16C654B/654DB compares one or two sequential receive data characters with the programmed Xon/Xoff or Xoff1,2 character value(s). If received character(s) match the programmed values, the SC16C654B/654DB will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER[5]) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters’ values, the SC16C654B/654DB will monitor the receive data stream for a match to the Xon1,2 character value(s). If a match is found, the SC16C654B/654DB will resume operation and clear the flags (ISR[4]). The SC16C654B/654DB offers a special Xon mode via MCR[5]. The initialized default setting of MCR[5] is a logic 0. In this state, Xoff and Xon will operate as defined above. Setting MCR[5] to a logic 1 sets a special operational mode for the Xon function. In this case, Xoff operates normally, however, transmission (Xon) will resume with the next character received, that is, a match is declared simply by the receipt of an incoming (RX) character.

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the SC16C654B/654DB compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the SC16C654B/654DB automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The SC16C654B/654DB sends the Xoff1,2 characters as soon as received data passes the programmed trigger level. To clear this condition, the SC16C654B/654DB will transmit the programmed Xon1,2 characters as soon as receive data drops below the programmed trigger level.

6.6 Special feature software flow control

A special feature is provided to detect an 8-bit character when EFR[5] is set. When 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[0:3]. Note that software flow control should be turned off when using this special mode by setting EFR[0:3] to a logic 0.

The SC16C654B/654DB compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although the Internal Register Table (Table 8) shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[0:1] define the number of character bits, that is, either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[0:1] also determine the number of bits that will be used for the special character comparison. Bit 0 in the X-registers corresponds with the LSB bit for the receive character.

6.7 Xon any feature

A special feature is provided to return the Xoff flow control to the inactive state following its activation. In this mode, any RX character received will return the Xoff flow control to the inactive state so that transmissions may be resumed with a remote buffer. This feature is more fully defined in Section 6.5 “Software flow control”.

6.8 Hardware/software and time-out interrupts

Three special interrupts have been added to monitor the hardware and software flow control. The interrupts are enabled by IER[5:7]. Care must be taken when handling these interrupts. Following a reset, the transmitter interrupt is enabled, the SC16C654B/654DB will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/TRS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C654B/654DB FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

In the 16 mode for the PLCC68 package, the system/board designer can optionally provide software controlled 3-state interrupt operation. This is accomplished by INTSEL and MCR[3]. When INTSEL interface pin is left open or made a logic 0, MCR[3] controls the 3-state interrupt outputs, INTA to INTD. When INTSEL is a logic 1, MCR[3] has no effect on the INTA to INTD outputs, and the package operates with interrupt outputs enabled continuously.

6.9 Programmable baud rate generator

The SC16C654B/654DB supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 80 MHz (for 3.3 V and 5 V operation), as required for supporting a 5 Mbit/s data rate. The SC16C654B/654DB can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins; see Figure 10. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates; see Table 7.

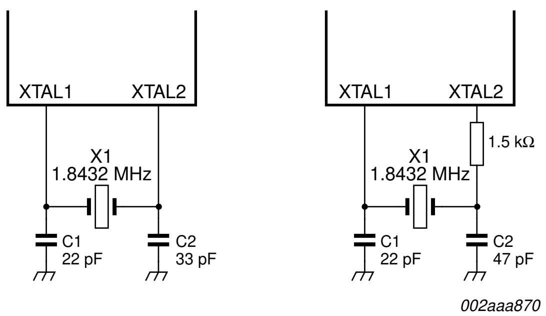

Fig 10. Crystal oscillator connection

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C654B/654DB divides the basic external clock by 16. Further division of this 16× clock provides two table rates to support low and high data rate applications using the same system design. After a hardware reset and during initialization, the

SC16C654B/654DB sets the default baud rate table according to the state of the CLKSEL pin. A logic 1 on CLKSEL will set the 1× clock default, whereas logic 0 will set the 4× clock default table. Following the default clock rate selection during initialization, the rate tables can be changed by the internal register MCR[7]. Setting MCR[7] to a logic 1 when CLKSEL is a logic 1 provides an additional divide-by-4, whereas setting MCR[7] to a logic 0 only divides by 1; see Table 7 and Figure 11. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 7 shows the two selectable baud rate tables available when using a 7.3728 MHz crystal.

Table 7: Baud rate generator programming table using a 7.3728 MHz clock

Output baud rate		User 16× clock divisor		DLM program value (HEX)	DLL program value (HEX)
MCR[7] = 1	MCR[7] = 0	Decimal	HEX		
50	200	2304	900	09	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2 k	24	18	00	18
9600	38.4 k	12	0C	00	0C
19.2 k	76.8 k	6	06	00	06
38.4 k	153.6 k	3	03	00	03
57.6 k	230.4 k	2	02	00	02
115.2 k	460.8 k	1	01	00	01

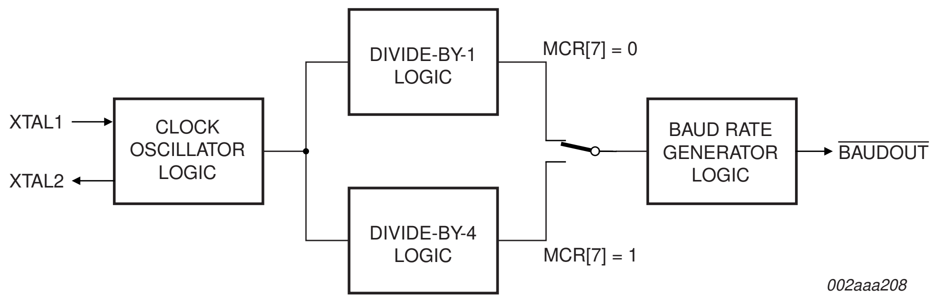

Fig 11. Baud rate generator circuitry

6.10 DMA operation

The SC16C654B/654DB FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[5:6] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C654B/654DB activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the SC16C654B/654DB sets the interrupt output pin when characters in the transmit FIFOs are below the transmit trigger level, or the characters in the receive FIFOs are above the receive trigger level.

Remark: DMA operation is not supported in the HVQFN48 package option.

6.11 Sleep mode

The SC16C654B/654DB is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. With EFR[4] and IER[4] enabled (set to a logic 1), the SC16C654B/654DB enters the sleep mode, but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins RX, $\overline{\text{RI}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{CD}}$, or a transmit data is provided by the user. If the sleep mode is enabled and the SC16C654B/654DB is awakened by one of the conditions described above, it will return to the sleep mode automatically after the last character is transmitted or read by the user. In any case, the sleep mode will not be entered while an interrupt(s) is pending. The SC16C654B/654DB will stay in the sleep mode of operation until it is disabled by setting IER[4] to a logic 0.

6.12 Loop-back mode

The internal loop-back capability allows on-board diagnostics. In the loop-back mode, the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR[0:3] register bits are used for controlling loop-back diagnostic testing. In the loop-back mode, OP1 and OP2 in the MCR register (bits 2:3) control the modem $\overline{\text{RI}}$ and $\overline{\text{CD}}$ inputs, respectively. MCR signals $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ (bits 0:1) are used to control the modem $\overline{\text{DSR}}$ and $\overline{\text{CTS}}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally; see Figure 12. The $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{CD}}$, and $\overline{\text{RI}}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, $\overline{\text{OP2}}$ and $\overline{\text{OP1}}$. Loop-back test data is entered into the transmit holding register via the user data bus interface, D[0:7]. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D[0:7]. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[0:3]) instead of the four Modem Status Register bits 4:7. The interrupts are still controlled by the IER.

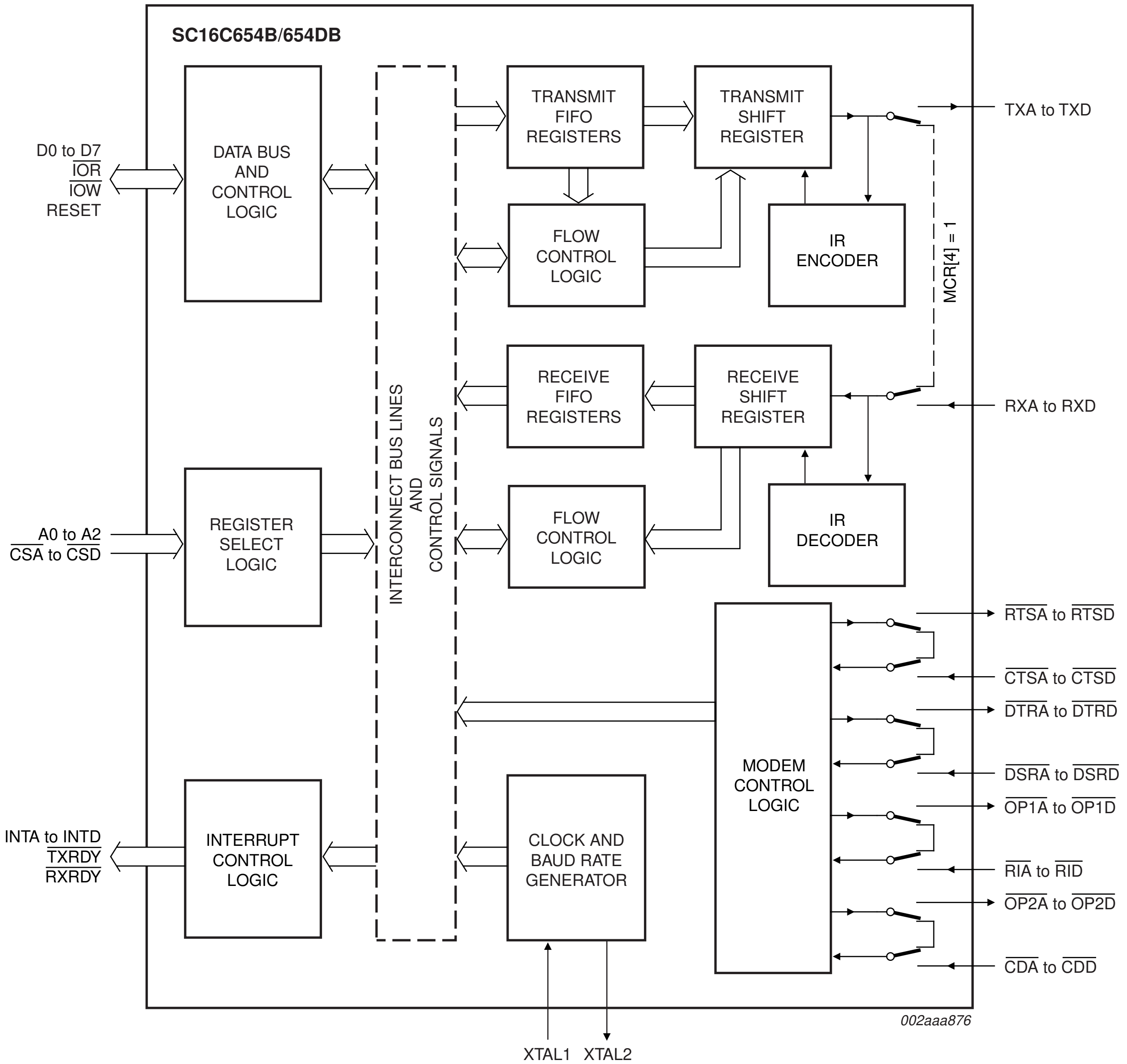

Fig 12. Internal loop-back mode diagram

7. Register descriptions

Table 8 details the assigned bit functions for the SC16C654B/654DB internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.11.

Table 8: SC16C654B/654DB internal registers

A2	A1	A0	Register	Default [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General Register Set [2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	CTS interrupt [3]	RTS interrupt [3]	Xoff interrupt [3]	Sleep mode [3]	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB) [3]	TX trigger (LSB) [3]	DMA mode select [4]	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	INT priority bit 4	INT priority bit 3	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	Clock select [3]	IR enable [3]	Xon Any [3]	loop back	$\overline{\text{OP2}}$, INTx enable	$\overline{\text{OP1}}$	$\overline{\text{RTS}}$	$\overline{\text{DTR}}$
1	0	1	LSR	60	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{\text{CD}}$	$\Delta\overline{\text{RI}}$	$\Delta\overline{\text{DSR}}$	$\Delta\overline{\text{CTS}}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special Register Set [5]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Enhanced Register Set [6]												
0	1	0	EFR	00	Auto CTS	Auto RTS	Special char. select	Enable IER[4:7], ISR[4:5], FCR[4:5], MCR[5:7]	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control
1	0	0	Xon-1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	0	1	Xon-2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
1	1	0	Xoff-1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	1	1	Xoff-2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown represents the register's initialized HEX value; X = not applicable.

[2] These registers are accessible only when LCR[7] = 0.

[3] These bits are only accessible when EFR[4] is set.

[4] This function is not supported in the HVQFN48 package; $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ are removed.

[5] The Special Register set is accessible only when LCR[7] is set to a logic 1.

[6] Enhanced Feature Register, Xon1/Xon2 and Xoff1/Xoff2 are accessible only when LCR is set to 'BFh'.

7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C654B/654DB and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA to INTD output pins in the 16 mode, or on wire-OR IRQ output pin in the 68 mode.

Table 9: Interrupt Enable Register bits description

Bit	Symbol	Description
7	IER[7]	CTS interrupt. logic 0 = disable the CTS interrupt (normal default condition) logic 1 = enable the CTS interrupt. The SC16C654B/654DB issues an interrupt when the CTS pin transitions from a logic 0 to a logic 1.
6	IER[6]	RTS interrupt. logic 0 = disable the RTS interrupt (normal default condition) logic 1 = enable the RTS interrupt. The SC16C654B/654DB issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1.
5	IER[5]	Xoff interrupt. logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition) logic 1 = enable the software flow control, receive Xoff interrupt. See Section 6.5 “Software flow control” for details.
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode. See Section 6.11 “Sleep mode” for details.
3	IER[3]	Modem Status Interrupt. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt