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SC16C751B

5 V, 3.3 V and 2.5 V UART with 64-byte FIFOs

Rev. 02 — 10 October 2008 Product data sheet

1. General description

The SC16C751B is a Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 5 Mbit/s.

The SC16C751B is functionally equivalent to the SC16C750B, and requires a special software initialization sequence to configure the device to operate (see Section 6.6). Programming of control registers enables the added features of the SC16C751B. Some of these added features are the 64-byte receive and transmit FIFOs, automatic hardware flow control. The selectable auto-flow control feature significantly reduces software overload and increases system efficiency while in FIFO mode by automatically controlling serial data flow using $\overline{RTS}$ output and $\overline{CTS}$ input signals. On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C751B operates at 5 V, 3.3 V and 2.5 V, the industrial temperature range and is available in the plastic HVQFN24 package.

2. Features

- Single channel
- 5 V, 3.3 V and 2.5 V operation
- 5 V tolerant on input only pins[1]
- Industrial temperature range (−40 °C to +85 °C)
- After reset, all registers are identical to the typical 16C450 register set
- Capable of running with all existing generic 16C450 software
- Up to 5 Mbit/s transmit/receive operation at 5 V, 3.3 V; 3 Mbit/s at 2.5 V
- 64-byte transmit FIFO
- 64-byte receive FIFO with error flags
- Programmable auto-$\overline{RTS}$ and auto-$\overline{CTS}$
  - In auto-$\overline{CTS}$ mode, $\overline{CTS}$ controls transmitter
  - In auto-$\overline{RTS}$ mode, receive FIFO contents and threshold control $\overline{RTS}$
- Automatic hardware flow control
- Software selectable baud rate generator
- Four selectable receive interrupt trigger levels
- Standard modem interface
- Sleep mode

1. For data bus pins D7 to D0, see Table 22 “Limiting values”.

- Standard asynchronous error and framing bits (start, stop, and parity overrun break)
- Independent receiver clock input
- Transmit, receive, line status, and data set interrupts independently controlled
- Fully programmable character formatting:
  - 5-bit, 6-bit, 7-bit, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (DC to 5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$)

3. Ordering information

Table 1. Ordering information

Industrial: V_{DD} = 2.5 V, 3.3 V or 5 V ± 10 %; T_{amb} = −40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
SC16C751BIBS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

4. Block diagram

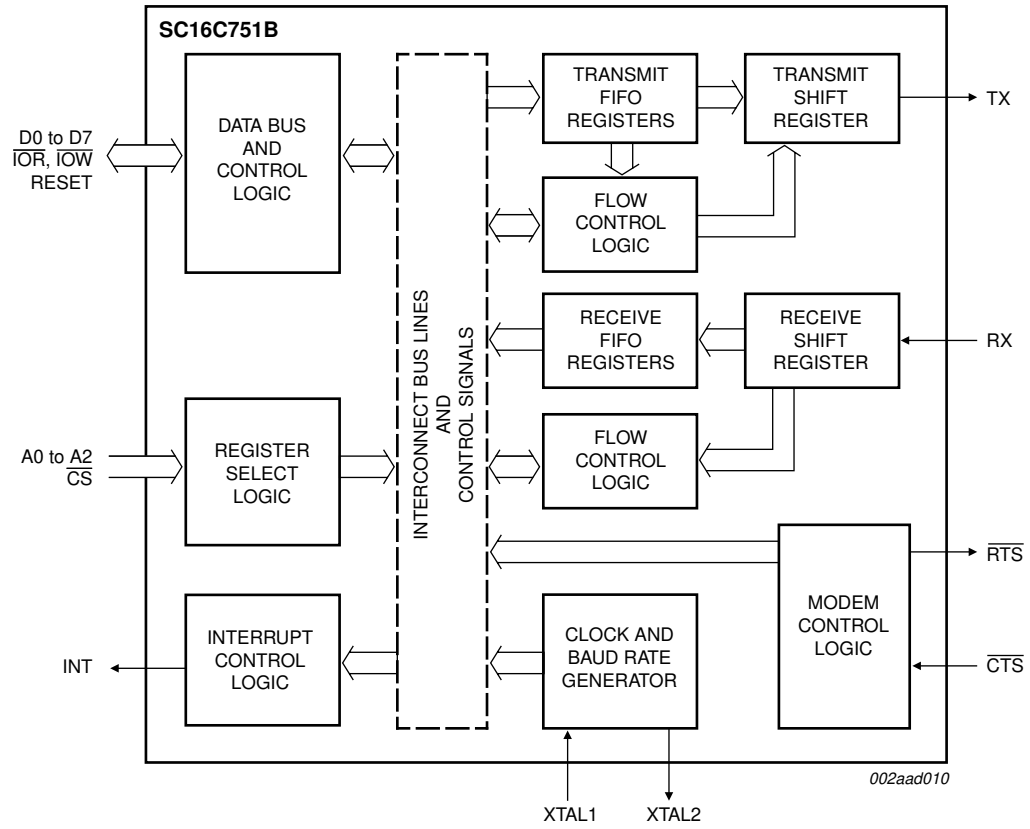


Fig 1. Block diagram of SC16C751B

5. Pinning information

5.1 Pinning

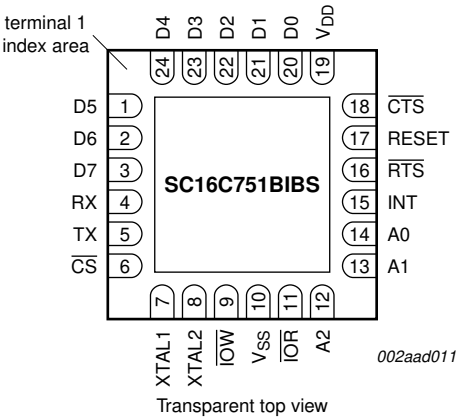


Fig 2. Pin configuration for HVQFN24

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	14	I	**Register select.** A0 to A2 are used during read and write operations to select the UART register to read from or write to. Refer to Table 3 for register addresses.
A1	13	I	
A2	12	I	
$\overline{CS}$	6	I	**Chip select.** When $\overline{CS}$ is LOW, the UART is selected.
$\overline{CTS}$	18	I	**Clear to send.** $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the Modem Status Register (MSR). MSR[3] ($\Delta\overline{CTS}$) indicates that $\overline{CTS}$ has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter.
D0	20	I/O	**Data bus.** Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the UART and the CPU.
D1	21	I/O	
D2	22	I/O	
D3	23	I/O	
D4	24	I/O	
D5	1	I/O	
D6	2	I/O	
D7	3	I/O	
INT	15	O	**Interrupt.** When active (HIGH), INT informs the CPU that the UART has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register or an enabled modem status interrupt. INT is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset.
RESET	17	I	**Master Reset.** When active (HIGH), RESET clears most UART registers and sets the levels of various output signals.
$\overline{IOR}$	11	I	**Read input.** When $\overline{IOR}$ is active (LOW) while the UART is selected, the CPU is allowed to read status information or data from a selected UART register.
$\overline{RTS}$	16	O	**Request to send.** When active, $\overline{RTS}$ informs the modem or data set that the UART is ready to receive data. $\overline{RTS}$ is set to the active level by setting the $\overline{RTS}$ Modem Control Register bit and is set to the inactive (HIGH) level either as a result of a Master Reset or during Loopback mode operations or by clearing bit 1 ($\overline{RTS}$) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to the inactive level by the receiver threshold control logic.
RX	4	I	**Serial data input.** RX is serial data input from a connected communications device.
TX	5	O	**Serial data output.** TX is composite serial data output to a connected communication device. TX is set to the marking (HIGH) level as a result of Master Reset.
V_{DD}	19	power	**2.5 V, 3 V or 5 V supply voltage.**
V_{SS}[1]	10	power	**Ground voltage.**

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{IOW}$	9	I	**Write input.** When $\overline{IOW}$ is active (LOW) and while the UART is selected, the CPU is allowed to write control words or data into a selected UART register.
XTAL1	7	I	**Crystal connection or External clock input.**
XTAL2[2]	8	O	**Crystal connection or the inversion of XTAL1 if XTAL1 is driven.**

[1] HVQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

[2] In Sleep mode, XTAL2 is left floating.

6. Functional description

The SC16C751B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C751B is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C751B is an upward solution that provides 64 bytes of transmit and receive FIFO memory, instead of none in the 16C450, or 16 bytes in the 16C550. The SC16C751B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C751B by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt and automatic hardware flow control is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C751B is capable of operation up to 5 Mbit/s with an 80 MHz external clock input (at 5 V).

The rich feature set of the SC16C751B is available through internal registers. Automatic hardware flow control, selectable transmit and receive FIFO trigger level, selectable TX and RX baud rates, modem interface controls, and a Sleep mode are some of these features.

6.1 Internal registers

The SC16C751B provides 12 internal registers for monitoring and control. These registers are shown in Table 3. These twelve registers are similar to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt

status and control registers (IER/ISR), a FIFO Control Register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible Scratchpad Register (SPR). Register functions are more fully described in the following paragraphs.

Table 3. Internal registers decoding

A2	A1	A0	READ mode	WRITE mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

6.2 FIFO operation

The 64-byte transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 4. Flow control mechanism

Selected trigger level (characters)	INT pin activation	Negate $\overline{RTS}$	Assert $\overline{RTS}$
16-byte FIFO			
1	1	1	0
4	4	4	0
8	8	8	0
14	14	14	0
64-byte FIFO			
1	1	1	0
16	16	16	0
32	32	32	0
56	56	56	0

6.3 Hardware flow control

When automatic hardware flow control is enabled, the SC16C751B monitors the $\overline{CTS}$ pin for a remote buffer overflow indication and controls the $\overline{RTS}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting MCR[5] (RTS) and MCR[1] (CTS) to a logic 1. If $\overline{CTS}$ transitions from a logic 0 to a logic 1 indicating a flow control request, the SC16C751B will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTS}$ input returns to a logic 0, indicating more data may be sent.

With the auto-$\overline{RTS}$ function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{RTS}$ pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the $\overline{RTS}$ pin will return to a logic 0 after the data buffer (FIFO) is emptied. However, under the above described conditions, the SC16C751B will continue to accept data until the receive FIFO is full.

6.4 Time-out interrupts

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C751B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time.

6.5 Programmable baud rate generator

The SC16C751B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable baud rate generator is capable of accepting an input clock up to 80 MHz, as required for supporting a 5 Mbit/s data rate. The SC16C751B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant, 22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 3). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 5).

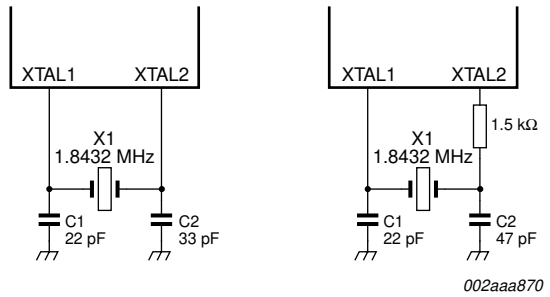


Fig 3. Crystal oscillator connection

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows selectable baud rates when using a 1.8432 MHz crystal.

For custom baud rates, the divisor value can be calculated using Equation 1:

$$divisor\ (in\ decimal) = \frac{XTAL1\ clock\ frequency}{serial\ data\ rate \times 16} \quad (1)$$

Table 5. Baud rates using 1.8432 MHz or 3.072 MHz crystal

Using 1.8432 MHz crystal			Using 3.072 MHz crystal		
Desired baud rate	**Divisor for 16× clock**	**Baud rate error**	**Desired baud rate**	**Divisor for 16× clock**	**Baud rate error**
50	2304		50	3840	
75	1536		75	2560	
110	1047	0.026	110	1745	0.026
134.5	857	0.058	134.5	1428	0.034
150	768		150	1280	
300	384		300	640	
600	192		600	320	
1200	96		1200	160	
1800	64		1800	107	0.312
2000	58	0.69	2000	96	
2400	48		2400	80	
3600	32		3600	53	0.628
4800	24		4800	40	
7200	16		7200	27	1.23
9600	12		9600	20	
19200	6		19200	10	
38400	3		38400	5	
56000	2	2.86			

6.6 Special software initialization sequence

Upon reset, the SC16C751B will not be able to receive. A special software initialization sequence must be sent to the device to enable its receiver clock.

The following software sequence can be added to the UART initialization routine, and this must be done before other registers are initialized.

```
WRITE LCR 00
WRITE MSR AA
WRITE MSR 55
WRITE MSR CC
WRITE MSR 33
WRITE MSR A5
WRITE MSR C3
WRITE MSR 5C
WRITE MSR 3A
WRITE LSR 20
```

6.7 Sleep mode

The SC16C751B is designed to operate with low power consumption. A special Sleep mode is included to further reduce power consumption (the internal oscillator driver is disabled) when the chip is not being used. With IER[4] enabled (set to a logic 1), the SC16C751B enters the Sleep mode, but resumes normal operation when a start bit is detected, a change of state of RX, $\overline{CTS}$, or a transmit data is provided by the user. If the Sleep mode is enabled and the SC16C751B is awakened by one of the conditions described above, it will return to the Sleep mode automatically after the last character is transmitted or read by the user. In any case, the Sleep mode will not be entered while an interrupt(s) is pending. The SC16C751B will stay in the Sleep mode of operation until it is disabled by setting IER[4] to a logic 0.

6.8 Low power mode

In Low power mode the oscillator is still running and only the clock to the UART core is cut off. This helps to reduce the operating current to about $\frac{1}{3}$. The UART wakes up under the same conditions as in Sleep mode.

6.9 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 4). The $\overline{CTS}$ is disconnected from its normal modem control input pins, and instead is connected internally to $\overline{RTS}$. Loopback test data is entered into the Transmit Holding Register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

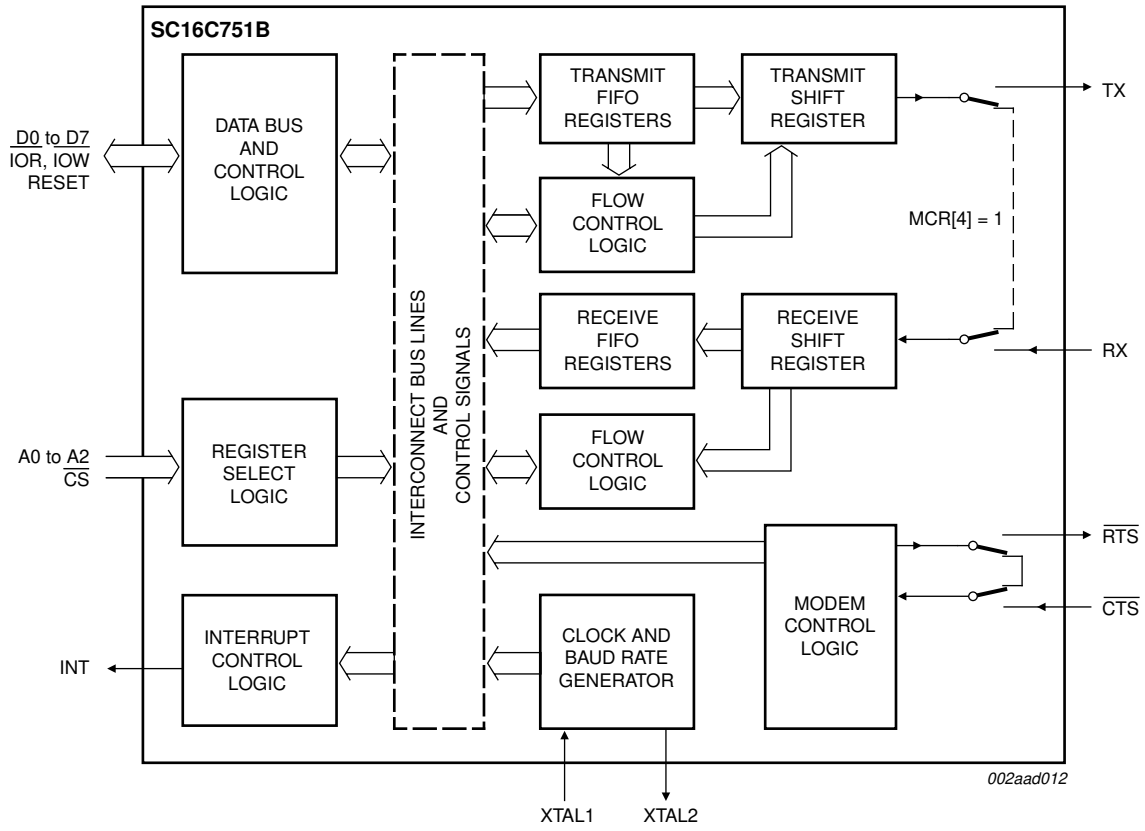


Fig 4. Internal Loopback mode diagram

7. Register descriptions

Table 6 details the assigned bit functions for the fifteen SC16C751B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.10.

Table 6. SC16C751B internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General register set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	Low power mode	Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	64-byte FIFO enable	reserved [3]	reserved [3]	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	64-byte FIFO enable	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	flow control enable	loopback	reserved [3]	reserved [3]	$\overline{RTS}$	reserved [3]
1	0	1	LSR	60	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	reserved	reserved	reserved	CTS	reserved	reserved	reserved	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special register set[4]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown represents the register's initialized hex value; X = n/a.

[2] These registers are accessible only when LCR[7] = 0.

[3] Do not write a logic 1 to the reserved bits. Read of the reserved bits reflect unknown values.

[4] The 'Special register set' is accessible only when LCR[7] is set to a logic 1.

7.1 Transmit and Receive Holding Registers (THR and RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C751B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After 7½ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT output pin.

Table 7. Interrupt Enable Register bits description

Bit	Symbol	Description
7:6	IER[7:6]	Not used.
5	IER[5]	Low power mode. logic 0 = disable Low power mode (normal default condition) logic 1 = enable Low power mode
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode. See Section 6.7 “Sleep mode” for details.
3	IER[3]	Modem Status Interrupt. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a fully assembled receive character is transferred from RSR to the RHR/FIFO, i.e., data ready, LSR[0]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1]. logic 0 = disable the transmitter empty interrupt (normal default condition) logic 1 = enable the transmitter empty interrupt

Table 7. Interrupt Enable Register bits description *...continued*

Bit	Symbol	Description
0	IER[0]	Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation. logic 0 = disable the receiver ready interrupt (normal default condition) logic 1 = enable the receiver ready interrupt

7.2.1 IER versus Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC16C751B in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will indicate any FIFO data errors.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs and set the receive FIFO trigger levels.

7.3.1 FIFO mode

Table 8. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7] (MSB), FCR[6] (LSB)	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 9.
5	FCR[5]	64-byte FIFO enable. logic 0 = 16-byte mode (normal default condition) logic 1 = 64-byte mode
4:3	FCR[4:3]	reserved
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO

Table 9. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level (bytes)	
		16-byte operation	64-byte operation
0	0	1	1
0	1	4	16
1	0	8	32
1	1	14	56

7.4 Interrupt Status Register (ISR)

The SC16C751B provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 10 “Interrupt source” shows the data values (bit 0 to bit 4) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 10. Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 11. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled. logic 0 or cleared = default condition
5	ISR[5]	64-byte FIFO enable. logic 0 = 16-byte operation logic 1 = 64-byte operation
4	ISR[4]	not used
3:1	ISR[3:1]	INT priority bit 2 to bit 0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 10). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 12. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch and enhanced feature register enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5	LCR[5]	Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. Programs the parity conditions (see Table 13). logic 0 = parity is not forced (normal default condition) LCR[5] = logic 1 and LCR[4] = logic 0: parity bit is forced to a logic 1 for the transmit and receive data LCR[5] = logic 1 and LCR[4] = logic 1: parity bit is forced to a logic 0 for the transmit and receive data
4	LCR[4]	Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format. logic 0 = odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition). logic 1 = even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format.
3	LCR[3]	Parity enable. Parity or no parity can be selected via this bit. logic 0 = no parity (normal default condition) logic 1 = a parity bit is generated during the transmission, receiver checks the data and parity for transmission errors
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 14). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bit 1, bit 0. These two bits specify the word length to be transmitted or received (see Table 15). logic 0 or cleared = default condition

Table 13. LCR[5] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
0	0	1	odd parity
0	1	1	even parity
1	0	1	force parity ‘1’
1	1	1	forced parity ‘0’

Table 14. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 15. LCR[1:0] word length

LCR[1]	LCR[0]	Word length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 16. Modem Control Register bits description

Bit	Symbol	Description
7	MCR[7]	reserved; set to 0
6	MCR[6]	reserved; set to 0
5	MCR[5]	AFE. This bit is the auto flow control enable. When this bit is set, the auto flow control is enabled.
4	MCR[4]	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output (TX) and the receiver input (RX), $\overline{CTS}$ are disconnected from the SC16C751B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 4). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3:2	MCR[3:2]	reserved
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTS}$ output to a logic 0
0	MCR[0]	reserved

The flow control can be configured by programming MCR[1] and MCR[5] as shown in Table 17.

Table 17. Flow control configuration

MCR[5] (AFE)	MCR[1] ($\overline{RTS}$)	Flow configuration
1	1	auto $\overline{RTS}$ and $\overline{CTS}$ enabled
1	0	auto $\overline{CTS}$ only enabled
0	X	auto $\overline{RTS}$ and $\overline{CTS}$ disabled

7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C751B and the CPU.

Table 18. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to logic 1 whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. logic 0 = no parity error (normal default condition) logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready. logic 0 = no data in receive holding register or FIFO (normal default condition) logic 1 = data has been received and is saved in the receive holding register or FIFO

7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C751B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 19. Modem Status Register bits description

Bit	Symbol	Description
7:5	MSR[7:5]	reserved
4	MSR[4]	Clear To Send. CTS. $\overline{CTS}$ functions as hardware flow control signal input if it is enabled via MCR[5]. Flow control (when enabled) allows starting and stopping the transmissions based on the external modem $\overline{CTS}$ signal. A logic 1 at the $\overline{CTS}$ pin will stop SC16C751B transmissions as soon as current character has finished transmission. Normally MSR[4] is the complement of the $\overline{CTS}$ input. However, in the Loopback mode, this bit is equivalent to the RTS bit in the MCR register.
3:1	MSR[3:1]	reserved
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no $\overline{CTS}$ change (normal default condition) logic 1 = the $\overline{CTS}$ input to the SC16C751B has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR[0] is set to logic 1, a Modem Status Interrupt will be generated if modem status interrupt is enabled.

7.9 Scratchpad Register (SPR)

The SC16C751B provides a temporary data register to store 8 bits of user information.

7.10 SC16C751B external reset conditions

Table 20. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
FCR	FCR[7:0] = 0

Table 21. Reset state for outputs

Output	Reset state
TX	HIGH
$\overline{RTS}$	HIGH
INT	LOW

8. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0 pins	V_{SS} – 0.3	V_{DD} + 0.3	V
		at any input only pin	V_{SS} – 0.3	5.3	V
T_{amb}	ambient temperature	operating	–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

9. Static characteristics

Table 23. Static characteristics

T_{amb} = –40 °C to +85 °C; tolerance of V_{DD} = ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage		–0.3	0.45	–0.3	0.6	–0.5	0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage		1.8	V_{DD}	2.4	V_{DD}	3.0	V_{DD}	V
V_{IL}	LOW-level input voltage		–0.3	0.65	–0.3	0.8	–0.5	0.8	V
V_{IH}	HIGH-level input voltage		1.6	-	2.0	-	2.2	V_{DD}	V
V_{OL}	LOW-level output voltage	on all outputs [1]							
		I_{OL} = 5 mA (data bus)	-	0.4	-	0.4	-	0.4	V
		I_{OL} = 4 mA (other outputs)	-	0.4	-	0.4	-	0.4	V
		I_{OL} = 2 mA (data bus)	-	0.4	-	0.4	-	0.4	V
		I_{OL} = 1.6 mA (other outputs)	-	0.4	-	0.4	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA (data bus)	1.85	-	2.0	-	2.0	-	V
		I_{OH} = –1 mA (other outputs)	1.85	-	2.0	-	2.0	-	V
		I_{OH} = –800 µA (data bus)	1.85	-	2.0	-	2.0	-	V
		I_{OH} = –400 µA (other outputs)	1.85	-	2.0	-	2.0	-	V
I_{LIL}	LOW-level input leakage current		-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current		-	±30	-	±30	-	±30	µA
$I_{DD(AV)}$	average supply current		-	3.5	-	4.5	-	4.5	mA
$I_{DD(sleep)}$	sleep mode supply current	[2]	-	50	-	50	-	50	µA
$I_{DD(lp)}$	low-power mode supply current		-	1.0	-	1.5	-	1.5	mA
C_i	input capacitance		-	5	-	5	-	5	pF
$R_{pu(int)}$	internal pull-up resistance		500	-	500	-	500	-	kΩ

[1] Except for XTAL2, V_{OL} = 1 V typically.

[2] Sleep current might be higher if there is activity on the UART data bus during Sleep mode.

10. Dynamic characteristics

Table 24. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{DD} = ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
t_{w2}	pulse width LOW			10	-	6	-	6	-	ns
t_{w1}	pulse width HIGH			10	-	6	-	6	-	ns
f_{XTAL1}	frequency on pin XTAL1		[1]	-	48	-	80	-	80	MHz
$t_{6s'}$	address set-up time			10	-	10	-	5	-	ns
t_{7d}	$\overline{IOR}$ delay from chip select			10	-	10	-	10	-	ns
t_{7w}	$\overline{IOR}$ strobe width	25 pF load		77	-	26	-	23	-	ns
t_{7h}	chip select hold time from $\overline{IOR}$			0	-	0	-	0	-	ns
$t_{7h'}$	address hold time			5	-	5	-	5	-	ns
t_{9d}	read cycle delay	25 pF load		20	-	20	-	20	-	ns
t_{12d}	delay from $\overline{IOR}$ to data	25 pF load		-	77	-	26	-	23	ns
t_{12h}	data disable time	25 pF load		-	15	-	15	-	15	ns
t_{13d}	$\overline{IOW}$ delay from chip select			10	-	10	-	10	-	ns
t_{13w}	$\overline{IOW}$ strobe width			20	-	20	-	15	-	ns
t_{13h}	chip select hold time from $\overline{IOW}$			0	-	0	-	0	-	ns
t_{14d}	$\overline{IOW}$ delay from address			10	-	10	-	10	-	ns
t_{15d}	write cycle delay			25	-	25	-	20	-	ns
t_{16s}	data set-up time			20	-	20	-	15	-	ns
t_{16h}	data hold time			15	-	5	-	5	-	ns
t_{17d}	delay from $\overline{IOW}$ to output	25 pF load		-	100	-	33	-	29	ns
t_{18d}	delay to set interrupt from modem input	25 pF load		-	100	-	24	-	23	ns
t_{19d}	delay to reset interrupt from $\overline{IOR}$	25 pF load; Figure 7		-	100	-	24	-	23	ns
t_{20d}	delay from stop to set interrupt		[2]	-	$1T_{RCLK}$	-	$1T_{RCLK}$	-	$1T_{RCLK}$	s
t_{21d}	delay time $\overline{IOR}$ to reset interrupt	25 pF load; Figure 9		-	100	-	29	-	28	ns
t_{22d}	delay from start to set interrupt			-	100	-	45	-	40	ns
t_{23d}	delay time from $\overline{IOW}$ to transmit start		[2]	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	$8T_{RCLK}$	$24T_{RCLK}$	s
t_{24d}	delay from $\overline{IOW}$ to reset interrupt			-	100	-	45	-	40	ns
t_{RESET}	RESET pulse width		[3]	100	-	40	-	40	-	ns
N	baud rate divisor			1	$2^{16} - 1$	1	$2^{16} - 1$	1	$2^{16} - 1$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[3] Reset pulse must happen when these signals are inactive: $\overline{CS}$, $\overline{IOR}$, $\overline{IOW}$.

10.1 Timing diagrams

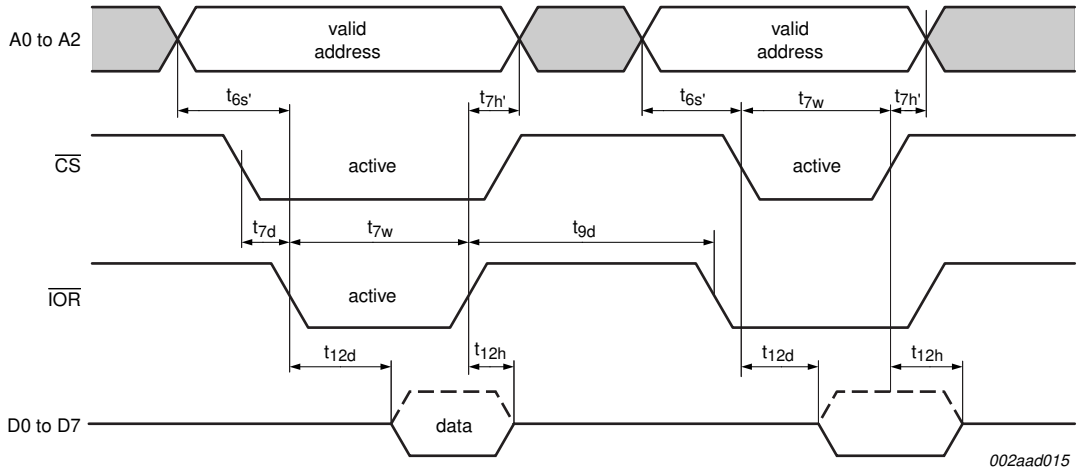


Fig 5. General read timing

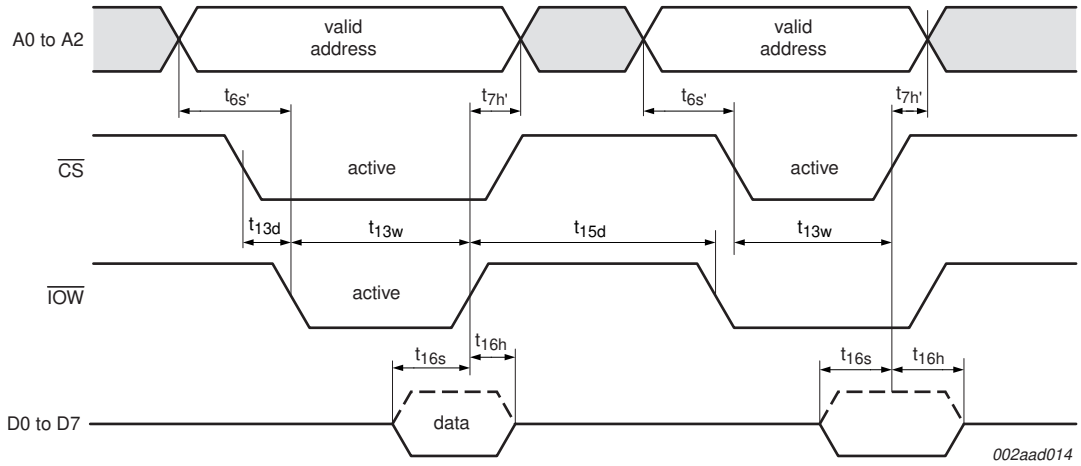


Fig 6. General write timing

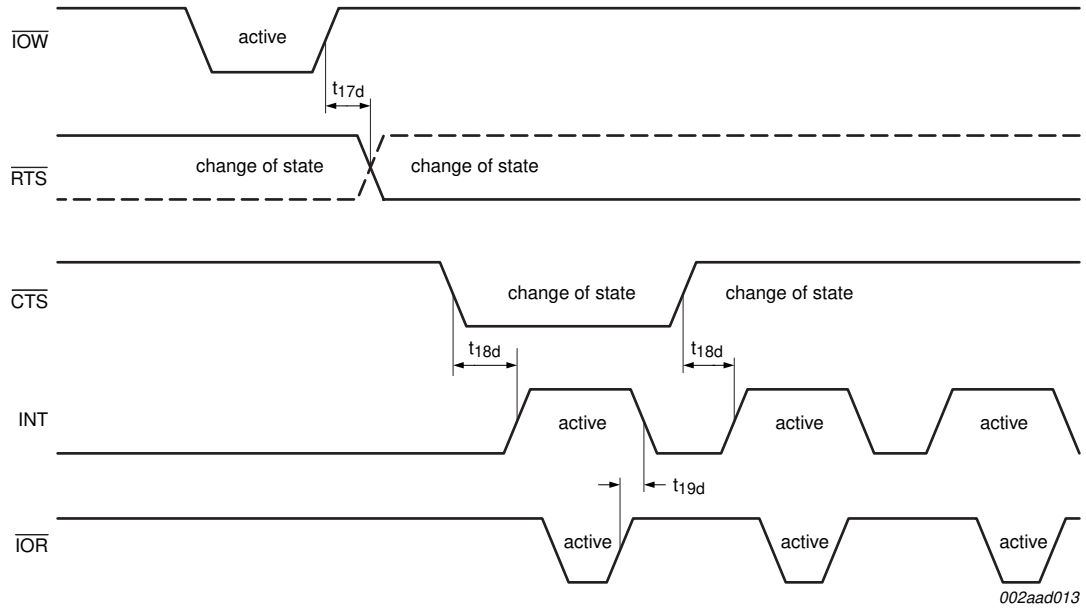
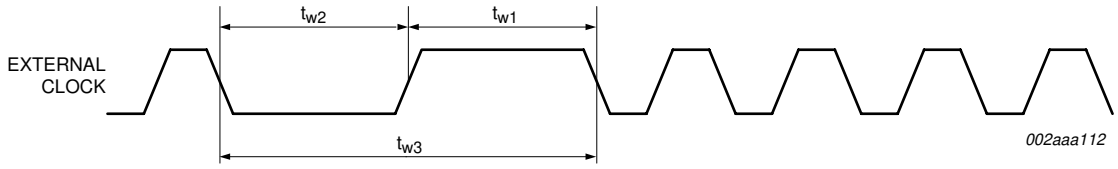


Fig 7. Modem input/output timing



$$f_{XTAL1} = \frac{1}{t_{w3}}$$

Fig 8. External clock timing

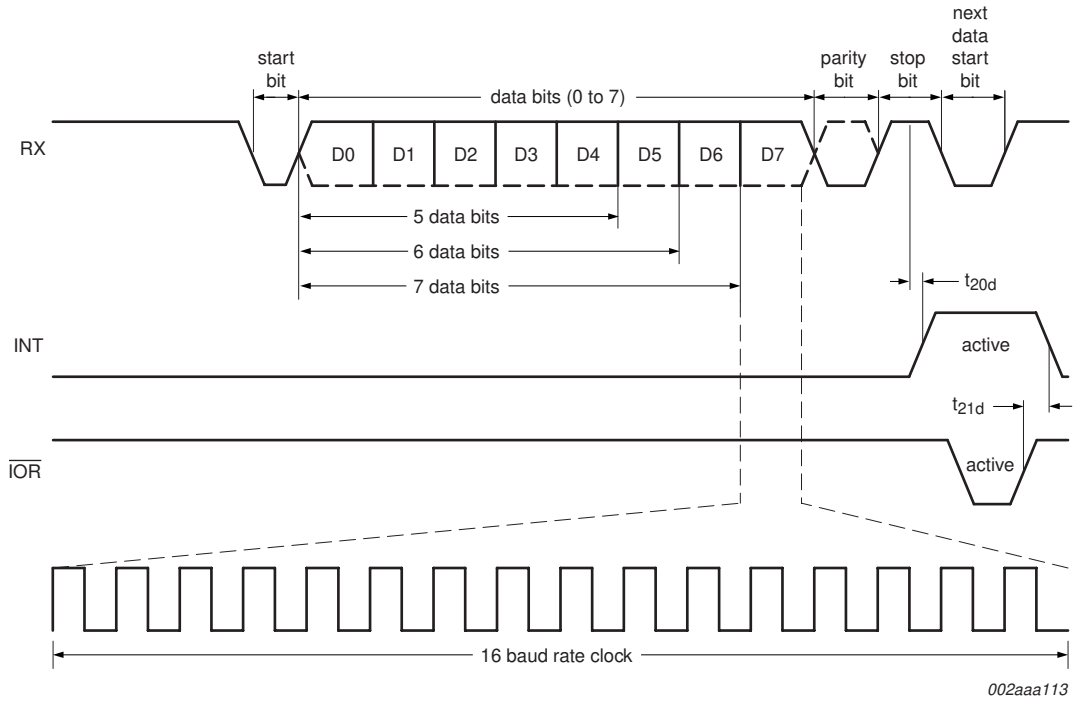


Fig 9. Receive timing

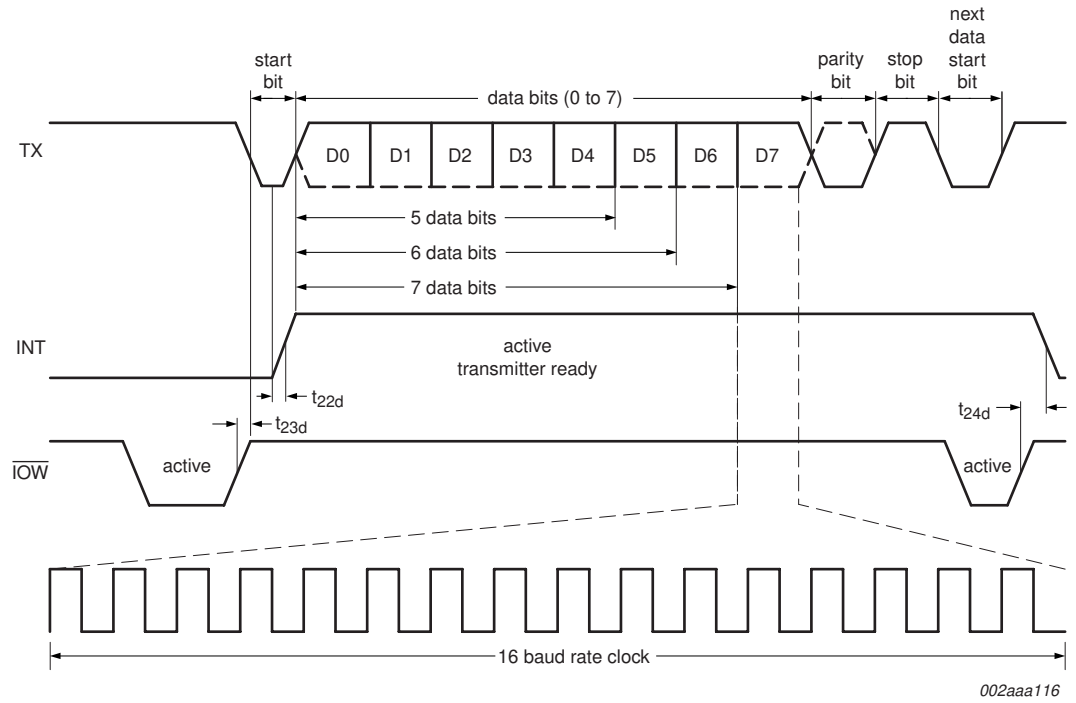


Fig 10. Transmit timing