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SC16C852SV

1.8 V dual UART, 20 Mbit/s (max.) with 128-byte FIFOs, infrared (IrDA), and XScale VLIO bus interface

Rev. 01 — 23 September 2008 Product data sheet

1. General description

The SC16C852SV is a 1.8 V, low power dual channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 20 Mbit/s (4× sampling rate). SC16C852SV can be programmed to operate in extended mode where additional advanced UART features are available (see Section 6.2). The SC16C852SV family UART provides enhanced UART functions with 128-byte FIFOs, modem control interface and IrDA encoder/decoder. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loopback capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC16C852SV with Intel XScale processor VLIO interface operates at 1.8 V and is available in the TFBGA36 package.

2. Features

- Dual channel high performance UART
- 1.8 V operation
- Advanced package: TFBGA36
- Up to 20 Mbit/s data rate (4× sampling) at 1.8 V
- Programmable sampling rate: 16×, 8×, 4×
- 128-byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 128-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- 128 programmable Receive and Transmit FIFO interrupt trigger levels
- 128 Receive and Transmit FIFO reporting levels (level counters)
- Automatic software (Xon/Xoff) and hardware ($\overline{RTS}$/$\overline{CTS}$ or $\overline{DTR}$/$\overline{DSR}$) flow control
- Programmable Xon/Xoff characters
- 128 programmable hardware and software trigger levels
- Automatic 9-bit mode (RS-485) address detection
- Automatic RS-485 driver turn-around with programmable delay
- Dual channel concurrent write
- UART software reset
- High resolution clock prescaler, from 0 to 15 with granularity of $^1/_{16}$ to allow non-standard UART clock to be used

- Industrial temperature range (−40 °C to +85 °C)
- Software compatible with industry standard SC16C652B
- Software selectable baud rate generator
- Supports IrDA version 1.0 (up to 115.2 kbit/s)
- Standard modem interface or infrared IrDA encoder/decoder interface
- Enhanced Sleep mode and low power feature
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{CD}$)
- Independent transmitter and receiver enable/disable
- Pb-free, RoHS compliant package offered

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16C852SVIET	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body $3.5 \times 3.5 \times 0.8$ mm	SOT912-1

4. Block diagram

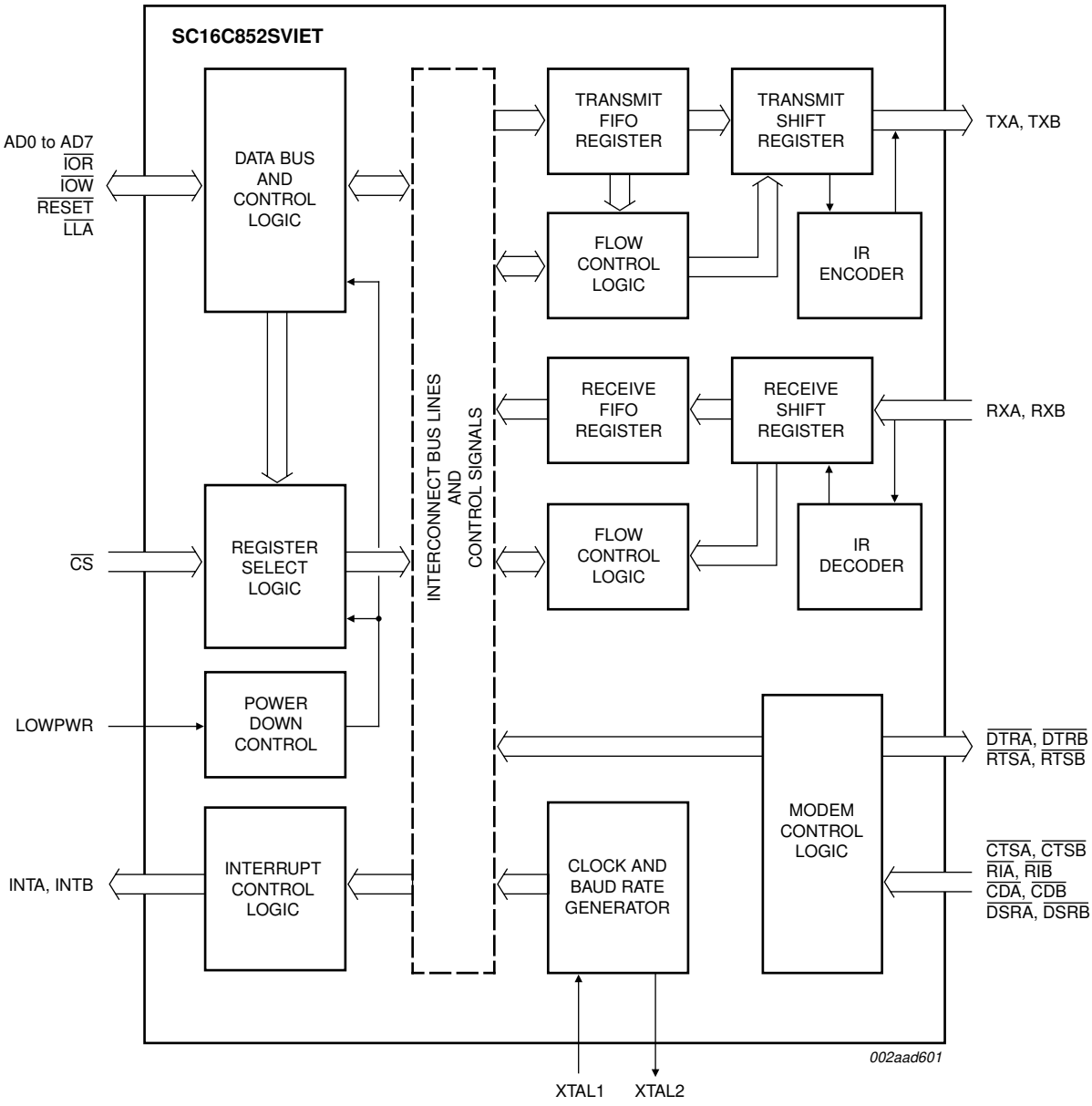


Fig 1. Block diagram of SC16C852SV

5. Pinning information

5.1 Pinning

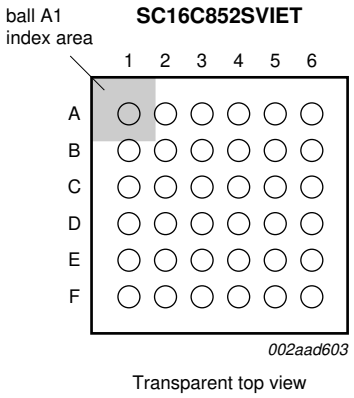


Fig 2. Pin configuration for TFBGA36

	1	2	3	4	5	6
A	AD4	AD2	AD0	$\overline{RIA}$	$\overline{DSRA}$	$\overline{CTSA}$
B	AD5	AD3	AD1	$\overline{CDA}$	$\overline{RESET}$	$\overline{DTRB}$
C	AD7	RXB	AD6	V_{DD}	$\overline{DTRA}$	$\overline{RTSA}$
D	RXA	TXA	XTAL1	V_{SS}	INTA	INTB
E	TXB	$\overline{CS}$	$\overline{IOW}$	$\overline{DSRB}$	$\overline{RTSB}$	$\overline{LLA}$
F	LOWPWR	XTAL2	$\overline{CDB}$	$\overline{IOR}$	$\overline{RIB}$	$\overline{CTSB}$

002aac352

Fig 3. TFBGA36 ball mapping (transparent top view)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
AD0	A3	I/O	**Address and Data bus (bidirectional).** These pins are the 8-bit multiplexed data bus and address bus for transferring information to or from the controlling CPU. AD0 is the least significant bit and is address A0 during the address cycle, and AD7 is the most significant bit and is address A7 during the address cycle.
AD1	B3		
AD2	A2		
AD3	B2		
AD4	A1		
AD5	B1		
AD6	C3		
AD7	C1		
$\overline{CDA}$	B4	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	F3		

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{CS}$	E2	I	**Chip Select (active LOW).** This pin enables the data transfers between the host and the SC16C852SV for the addressed channel. Individual channel selection is done with address A6. When A6 is 0 channel A is selected, and when A6 is 1 channel B is selected.
$\overline{CTSA}$	A6	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{CTS}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C852SV. Status can be tested by reading MSR[4].
$\overline{CTSB}$	F6		
$\overline{DSRA}$	A5	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. Status can be tested by reading MSR[5].
$\overline{DSRB}$	E4		
$\overline{DTRA}$	C5	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the SC16C852SV is powered-on and ready. This pin can be controlled via the Modem Control Register. Writing a logic 1 to MCR[0] will set the $\overline{DTR}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset.
$\overline{DTRB}$	B6		
INTA	D5	O	**Channel A interrupt output.** The output state is defined by the user through the software setting of MCR[3]. INTA is set to the active mode when MCR[3] is set to a logic 1. INTA is set to the 3-state mode when MCR[3] is set to a logic 0. See Table 19.
INTB	D6	O	**Channel B interrupt output.** The output state is defined by the user through the software setting of MCR[3]. INTB is set to the active mode when MCR[3] is set to a logic 1. INTB is set to the 3-state mode when MCR[3] is set to a logic 0. See Table 19.
$\overline{IOR}$	F4	I	**Read strobe (active LOW).** A HIGH to LOW transition on this signal starts the read cycle. The SC16C852SV reads a byte from the internal register and puts the byte on the data bus for the host to retrieve.
$\overline{IOW}$	E3	I	**Write strobe (active LOW).** A HIGH to LOW transition on this signal starts the write cycle, and a LOW to HIGH transition transfers the data on the data bus to the internal register.
$\overline{LLA}$	E6	I	**Latch Lower Address (active LOW).** A logic LOW on this pin puts the VLIO interface in the address phase of the transaction, where the lower 8 bits of the VLIO (specifying the UART register and the channel address) are loaded into the address latch of the device through the AD7 to AD0 bus. A logic HIGH puts the VLIO interface in the data phase where data can are transferred between the host and the UART.
LOWPWR	F1	I	**Low Power.** When asserted (active HIGH), the device immediately goes into low power mode. The oscillator is shut-off and some host interface pins are isolated from the host's bus to reduce power consumption. The device only returns to normal mode when the LOWPWR pin is de-asserted. On the negative edge of a de-asserting LOWPWR signal, the device is automatically reset and all registers return to their default reset states. This pin has an internal pull-down resistor, therefore, it can be left unconnected.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{\text{RESET}}$	B5	I	**Master reset (active LOW).** A reset pulse will reset the internal registers and all the outputs. The SC16C852SV transmitter outputs and receiver inputs will be disabled during reset time. (See Section 7.24 "SC16C852SV external reset condition and software reset" for initialization details.)
$\overline{\text{RIA}}$	A4	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
$\overline{\text{RIB}}$	F5		
$\overline{\text{RTSA}}$	C6	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{\text{RTS}}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1.
$\overline{\text{RTSB}}$	E5		
RXA	D1	I	**Receive data A, B.** These inputs are associated with individual serial channel data to the SC16C852SV receive input circuits, A through B. The RX signal will be a logic 1 during reset, idle (no data), or when not receiving data. During the local Loopback mode, the RX input pin is disabled and TX data is connected to the UART RX input, internally.
RXB	C2		
TXA	D2	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC16C852SV. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.
TXB	E1		
V_{DD}	C4	I	**Power supply input.**
V_{SS}	D4	I	**Signal and power ground.**
XTAL1	D3	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates (see Section 6.9 "Programmable baud rate generator"). See Figure 5.
XTAL2	F2	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1.

6. Functional description

The SC16C852SV provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C852SV represents such an integration with greatly enhanced features. The SC16C852SV is fabricated with an advanced CMOS process.

The SC16C852SV is an upward solution to the SC16C652B with a VLIO interface that provides a dual UART capability with 128 bytes of transmit and receive FIFO memory, instead of 32 bytes for the SC16C652B. The SC16C852SV is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C852SV by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable receive and transmit FIFO trigger interrupt levels are provided in normal mode, or 128 programmable levels are provided in extended mode for maximum data throughput performance especially when operating in a multi-channel environment (see Section 6.2 “Extended mode (128-byte FIFO)”). The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, and increases performance.

A low power pin (LOWPWR) is provided to further reduce power consumption by isolating the host interface bus.

The SC16C852SV is capable of operation up to 20 Mbit/s with an external 80 MHz clock. With a 24 MHz crystal it is capable of operation up to 6 Mbit/s.

The rich feature set of the SC16C852SV is available through internal registers. These features are: selectable and programmable receive and transmit FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls (all standard features). Following a power-on reset an external reset or a software reset, the SC16C852SV is software compatible with the previous generation SC16C652B.

6.1 UART A-B functions

The UART provides the user with the capability to bidirectionally transfer information between a CPU and an external serial device. The $\overline{CS}$ pin together with addresses A6 and A7 determine which channel of the UART is being accessed; see Table 3.

Table 3. Serial port selection

H = HIGH-level; L = LOW-level; X = Don’t care.

Chip Select	Function
$\overline{CS}$ = H, A7 = X, A6 = X	none
$\overline{CS}$ = L, A7 = L, A6 = L	UART channel A
$\overline{CS}$ = L, A7 = L, A6 = H	UART channel B
$\overline{CS}$ = L, A7 = L, A6 = X	device not selected

6.2 Extended mode (128-byte FIFO)

The device is in the extended mode when any of these four registers contains any value other than 0: FLWCNTH, FLWCNTL, TXINTLVL, RXINTLVL.

6.3 Internal registers

The SC16C852SV provides two sets of internal registers (A and B) consisting of 25 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4.

Table 4. Internal registers decoding

A3	A2	A1	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Extra Feature Control Register (EFCR)
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Second special register set (TXLVLCNT/RXLVLCNT)[3]				
0	1	1	Transmit FIFO Level Count	n/a
1	0	0	Receive FIFO Level Count	n/a
Enhanced register set (EFR, Xon1/Xon2, Xoff1/Xoff2)[4]				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon1 word	Xon1 word
1	0	1	Xon2 word	Xon2 word
1	1	0	Xoff1 word	Xoff1 word
1	1	1	Xoff2 word	Xoff2 word
First extra feature register set (TXINTLVL/RXINTLVL, FLWCNTH/FLWCNTL)[5]				
0	1	0	Transmit FIFO Interrupt Level	Transmit FIFO Interrupt Level
1	0	0	Receive FIFO Interrupt Level	Receive FIFO Interrupt Level
1	1	0	Flow Control Count High	Flow Control Count High
1	1	1	Flow Control Count Low	Flow Control Count Low
Second extra feature register set (CLKPRES, SAMPR, RS485TIME, AFCR2, AFCR1)[6]				
0	1	0	Clock Prescaler	Clock Prescaler
0	1	1	Sampling rate	Sampling rate
1	0	0	RS-485 turn-around Timer	RS-485 turn-around Timer
1	1	0	Additional Feature Control Register 2	Additional Feature Control Register 2
1	1	1	Additional Feature Control Register 1	Additional Feature Control Register 1

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Second special register are accessible only when EFCR[0] = 1.

[4] Enhanced feature registers are only accessible when LCR = 0xBF.

[5] First extra feature registers are only accessible when EFCR[2:1] = 01b.

[6] Second extra feature registers are only accessible when EFCR[2:1] = 10b.

6.4 FIFO operation

6.4.1 32-byte FIFO mode

When all four of these registers (TXINTLVL, RXINTLVL, FLWCNTH, FLWCNTL) in the First Extra Register Set are empty (0x00) the transmit and receive trigger levels are set by FCR[7:4]. In this mode the transmit and receive trigger levels are backward compatible to the SC16C652B (see Table 5), and the FIFO sizes are 32 entries. The transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). It should be noted that the user can set the transmit trigger levels by writing to the FCR, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU (see Section 6.8). Please refer to Table 10 and Table 11 for the setting of FCR[7:4].

Table 5. Interrupt trigger level and Flow control mechanism

(FCR[7:6, 5:4])	INTA/INTB pin activation		Negate $\overline{\text{RTSA}}$/$\overline{\text{RTSB}}$ or send Xoff	Assert $\overline{\text{RTSA}}$/$\overline{\text{RTSB}}$ or send Xon
	RX	TX		
[00, 00]	8	16	8	0
[01, 01]	16	8	16	7
[10, 10]	24	24	24	15
[11, 11]	28	30	28	23

6.4.2 128-byte FIFO mode

When either TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the First Extra Register Set contains any value other than 0x00, the transmit and receive trigger levels are set by TXINTLVL and RXINTLVL registers. TXINTLVL sets the trigger levels for the transmit FIFO, and the transmit trigger levels can be set to any value between 1 and 128 with granularity of 1. RXINTLVL sets the trigger levels for the receive FIFO, the receive trigger levels can be set to any value between 1 and 128 with granularity of 1.

When the effective FIFO size changes (that is, when FCR[0] toggles or when the combined content of TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL changes between equal and unequal to 0x00), both RX FIFO and TX FIFO will be reset (data in the FIFO will be lost).

6.5 Hardware flow control

When automatic hardware flow control is enabled, the SC16C852SV monitors the $\overline{\text{CTSx}}$ pin for a remote buffer overflow indication and controls the $\overline{\text{RTSx}}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If $\overline{\text{CTSx}}$ transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[7:6]), and the

SC16C852SV will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{\text{CTSx}}$ input returns to a logic 0, indicating more data may be sent.

When AFCR1[2] is set to 1, then the function of $\overline{\text{CTSx}}$ pin is mapped to the $\overline{\text{DSRx}}$ pin, and the function of $\overline{\text{RTS}}$ is mapped to $\overline{\text{DTRx}}$ pin. $\overline{\text{DSRx}}$ and $\overline{\text{DTRx}}$ pins will behave as described above for $\overline{\text{CTSx}}$ and $\overline{\text{RTSx}}$.

With the automatic hardware flow control function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{\text{RTSx}}$ (or $\overline{\text{DTRx}}$) pin will not be forced to a logic 1 (RTS off) until the receive FIFO reaches the next trigger level. However, the $\overline{\text{RTSx}}$ (or $\overline{\text{DTRx}}$) pin will return to a logic 0 after the receive buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. Under the above described conditions, the SC16C852SV will continue to accept data until the receive FIFO is full.

When TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL in the First Extra Register Set are all zeroes, the hardware and software flow control trigger levels are set by FCR[7:4]; see Table 5.

When either TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the First Extra Register Set contains any value other than 0x00, the hardware and software flow control trigger levels are set by FLWCNTH and FLWCNTL. The content in FLWCNTH determines how many bytes are in the receive FIFO before $\overline{\text{RTSx}}$ (or $\overline{\text{DTRx}}$) is de-asserted or XOFF is sent. The content of FLWCNTL determines how many bytes are in the receive FIFO before $\overline{\text{RTSx}}$ (or $\overline{\text{DTRx}}$) is asserted, or XON is sent.

In 128-byte FIFO mode, hardware and software flow control trigger levels can be set to any value between 1 and 128 in granularity of 1. The value of FLWCNTH should always be greater than FLWCNTL. The UART does not check for this condition automatically, and if this condition is not met spurious operation of the device might occur. When using FLWCNTH and FWLCNTL, these registers must be initialized to the proper values before hardware or software flow control is enabled via the EFR register.

6.6 Software flow control

When software flow control is enabled, the SC16C852SV compares one or two sequentially received data characters with the programmed Xon or Xoff character value(s). If the received character(s) match the programmed Xoff values, the SC16C852SV will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, ISR bit 4 will be set (if enabled via IER[5]) and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16C852SV will monitor the receive data stream for a match to the Xon1/Xon2 character value(s). If a match is found, the SC16C852SV will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions (see Table 24). When double 8-bit Xon/Xoff characters are selected, the SC16C852SV compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly.

Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the receive FIFO. When using software flow control, the Xon/Xoff characters cannot be used for data transfer.

In the event that the receive buffer is overfilling, the SC16C852SV automatically sends an Xoff character (when enabled) via the serial TX output to the remote UART. The SC16C852SV sends the Xoff1/Xoff2 characters as soon as the number of received data in the receive FIFO passes the programmed trigger level. To clear this condition, the SC16C852SV will transmit the programmed Xon1/Xon2 characters as soon as the number of characters in the receive FIFO drops below the programmed trigger level.

6.7 Special character detect

A special character detect feature is provided to detect an 8-bit character when EFR[5] is set. When an 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RXA/RXB data. This condition is selected in conjunction with EFR[3:0] (see Table 24). Note that software flow control should be turned off when using this special mode by setting EFR[3:0] to all zeroes.

The SC16C852SV compares each incoming receive character with Xoff2 data. If a match occurs, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although Table 7 “SC16C852SV internal registers” shows Xon-1, Xon-2, Xoff-1, Xoff-2 with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[1:0] define the number of character bits, that is, either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[1:0] also determine the number of bits that will be used for the special character comparison. Bit 0 in the Xon-1, Xon-2, Xoff-1, Xoff-2 registers corresponds with the LSB bit for the received character.

6.8 Interrupt priority and time-out interrupts

The interrupts are enabled by IER[7:0]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC16C852SV will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The ISR indicates the current singular highest priority interrupt only. A condition can exist where a higher priority interrupt masks the lower priority interrupt(s) (see Table 12). Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[0]), and it is important to serve these interrupts correctly. The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C852SV FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] to see if there are any additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

6.9 Programmable baud rate generator

The SC16C852SV UART contains a programmable rational baud rate generator that takes any clock input and divides it by a divisor in the range between 1 and ($2^{16} - 1$). The SC16C852SV offers the capability of dividing the input frequency by rational divisor. The fractional part of the divisor is controlled by the CLKPRES register in the First Extra Register Set.

$$baud\ rate = \frac{f_{XTAL1}}{MCR[7] \times \left[SAMPR \times \left(N + \frac{M}{SAMPR} \right) \right]}$$

where:

N is the integer part of the divisor in DLL and DLM registers;

M is the fractional part of the divisor in CLKPRES register;

f_{XTAL1} is the clock frequency at XTAL1 pin;

SAMPR is the sampling rate in SAMPR register (16×, 8×, 4×)

Prescaler = 1 when MCR[7] is set to 0.

Prescaler = 4 when MCR[7] is set to 1.

Remark: $\frac{M}{SAMPR}$ should always be less than 1.

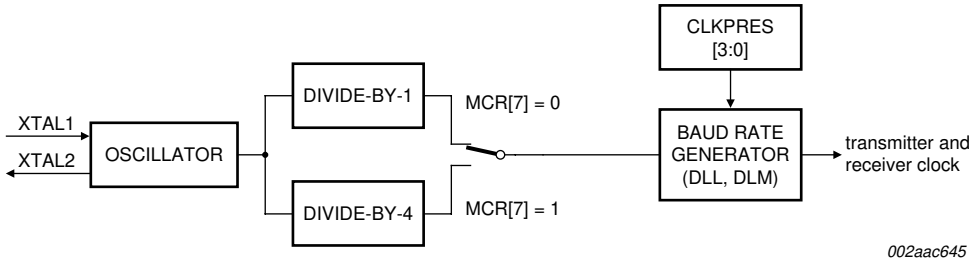


Fig 4. Prescalers and baud rate generator block diagram

A single baud rate generator is provided for the transmitter and receiver. The programmable baud rate generator is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC16C852SV can be configured for internal or external clock operation. For internal clock operation, an industry standard crystal is connected externally between the XTAL1 and XTAL2 pins (see Figure 5). Alternatively, an external clock can be connected to the XTAL1 pin (see Figure 6) to clock the internal baud rate generator for standard or custom rates (see Table 6).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C852SV divides the basic external clock by 16. The baud rate is configured via the CLKPRES, DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of the baud rate generator.

However, the user can also select 4×, 8× sampling rates (see Section 7.20 “Sampling Rate (SAMPR)”) to operate at four times or two times faster than 16× sampling rate.

Programming the baud rate generator registers CLKPRES, DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 6 shows the selectable baud rate table available when using a 1.8432 MHz external clock input with MCR[7] is 0, SAMPR[1:0] = 00b and CLKPRES = 0x00.

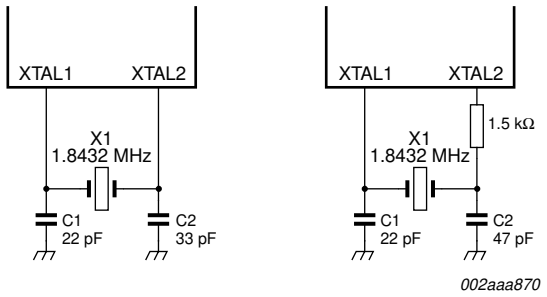
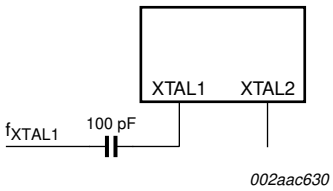


Fig 5. Crystal oscillator connection



If f_{XTAL1} frequency is greater than 50 MHz, then a DC blocking capacitor is required.

XTAL2 pin should be left unconnected when an external clock is used.

Fig 6. External clock connection

Table 6. Baud rate generator programming table using a 1.8432 MHz clock with MCR[7] = 0, SAMPR[1:0] = 00b and CLKPRE[3:0] = 0

Output baud rate (bit/s)	Output 16× clock divisor (decimal)	Output 16× clock divisor (hexadecimal)	DLM program value (hexadecimal)	DLL program value (hexadecimal)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
3600	32	20	00	20
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C

Table 6. Baud rate generator programming table using a 1.8432 MHz clock with MCR[7] = 0, SAMPR[1:0] = 00b and CLKPRE[3:0] = 0 *…continued*

Output baud rate (bit/s)	Output 16× clock divisor (decimal)	Output 16× clock divisor (hexadecimal)	DLM program value (hexadecimal)	DLL program value (hexadecimal)
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

6.10 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally (see Figure 7). MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, the transmitter output (TXA/TXB) and the receiver input (RXA/RXB) are disconnected from their associated interface pins, and instead are connected together internally. The $\overline{\text{CTSx}}$, $\overline{\text{DSRx}}$, $\overline{\text{CDx}}$, and $\overline{\text{RIx}}$ are disconnected from their normal modem control inputs pins, and instead are connected internally to $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, MCR[3] ($\overline{\text{OP2A}}$/$\overline{\text{OP2B}}$) and MCR[2] ($\overline{\text{OP1A}}$/$\overline{\text{OP1B}}$). Loopback test data is entered into the transmit holding register via the user data bus interface, D[7:0]. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D[7:0]. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode the interrupt pins are 3-stated, therefore the software must use polling method (see Section 7.2.2) to send and receive data.

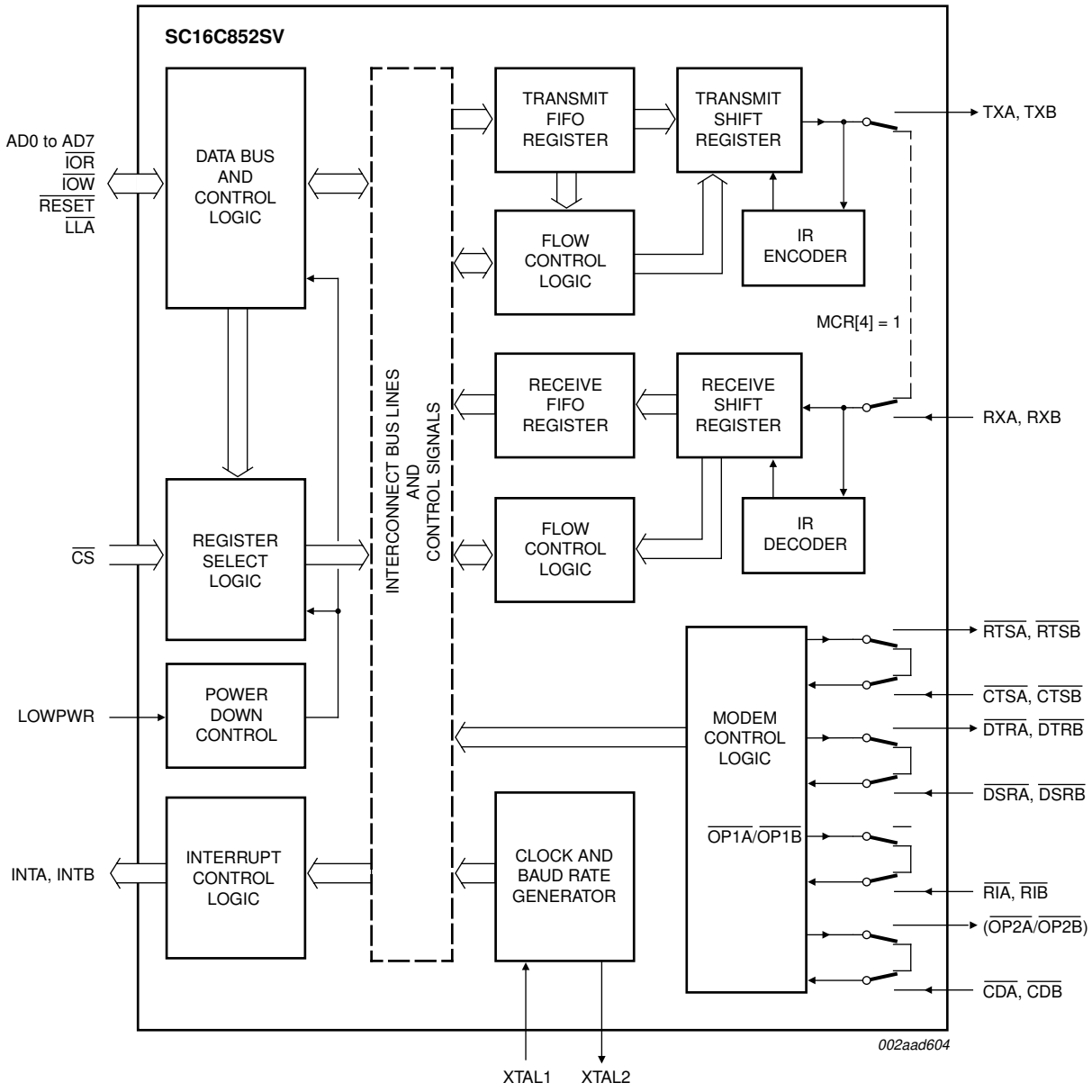


Fig 7. Internal Loopback mode diagram

6.11 Sleep mode

Sleep mode is an enhanced feature of the SC16C852SV UART. It is enabled when EFR[4], the enhanced functions bit, is set **and** when IER[4] of both channels are set.

6.11.1 Conditions to enter Sleep mode

Sleep mode is entered when:

- Modem input pins are not toggling.
- The serial data input line, RXA/RXB, is idle for 4 character time (logic HIGH) and AFCR1[4] is 0. When AFCR1[4] is 1, the device will go to sleep regardless of the state of the RXA/RXB pin (see Section 7.22 for the description of AFCR1 bit 4).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending.
- The RX FIFO is empty.

In Sleep mode, the UART clock and baud rate clock are stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced.

Remark: Writing to the divisor latches, DLL and DLM, to set the baud clock, must not be done during Sleep mode. Therefore, it is advisable to disable Sleep mode using IER[4] before writing to DLL or DLM.

6.11.2 Conditions to resume normal operation

SC16C852SV resumes normal operation by any of the following:

- Receives a start bit on RXA or RXB pin.
- Data is loaded into transmit FIFO.
- A change of state on any of the modem input pins.

If the device is awakened by one of the conditions described above, it will return to the Sleep mode automatically after all the conditions described in Section 6.11.1 are met. The device will stay in Sleep mode until it is disabled by setting any channel's IER bit 4 to a logic 0.

When the SC16C852SV is in Sleep mode and the host interface bus (AD7 to AD0, $\overline{IOW}$, $\overline{IOR}$, $\overline{CS}$) remains in steady state, either HIGH or LOW, the sleep current will be in the microampere range as specified in Table 37 "Static characteristics". If any of these signals is toggling or floating then the sleep current will be higher.

6.12 Low Power feature

A Low Power feature is provided by the SC16C852SV to prevent the switching of the host data bus from influencing the sleep current. When the pin LOWPWR is activated (logic HIGH), the device immediately and unconditionally goes into Low Power mode. All clocks are stopped and most host interface pins are isolated to reduce power consumption. The device only returns to normal mode when the LOWPWR pin is de-asserted. The pin can be left unconnected because it has an internal pull-down resistor.

6.13 RS-485 features

6.13.1 Auto RS-485 $\overline{\text{RTS}}$ control

Normally the $\overline{\text{RTSx}}$ pin is controlled by MCR bit 1, or if hardware flow control is enabled, the logic state of the $\overline{\text{RTSx}}$ pin is controlled by the hardware flow control circuitry. EFCR2 register bit 4 will take the precedence over the other two modes; once this bit is set, the transmitter will control the state of the $\overline{\text{RTSx}}$ pin. The transmitter automatically asserts the $\overline{\text{RTSx}}$ pin (logic 0) once the host writes data to the transmit FIFO, and de-asserts the $\overline{\text{RTSx}}$ pin (logic 1) once the last bit of the data has been transmitted.

To use the auto RS-485 $\overline{\text{RTS}}$ mode, the software would have to disable the hardware flow control function.

6.13.2 RS-485 $\overline{\text{RTS}}$ inversion

EFCR2 bit 5 reverses the polarity of the $\overline{\text{RTSx}}$ pin if the UART is in auto RS-485 $\overline{\text{RTS}}$ mode.

When the transmitter has data to be sent, it will de-assert the $\overline{\text{RTSx}}$ pin (logic 1), and when the last bit of the data has been sent out, the transmitter asserts the $\overline{\text{RTS}}$ pin (logic 0).

6.13.3 Auto 9-bit mode (RS-485)

EFCR2 bit 0 is used to enable the 9-bit mode (Multi-drop or RS-485 mode). In this mode of operation, a ‘master’ station transmits an address character followed by data characters for the addressed ‘slave’ stations. The slave stations examine the received data and interrupt the controller if the received character is an address character (parity bit = 1).

To use the auto 9-bit mode the software would have to disable the hardware and software flow control functions.

6.13.3.1 Normal Multi-drop mode

The 9-bit Mode in EFCR (bit 0) is enabled, but not Special Character Detect (EFR bit 5). The receiver is set to Force Parity 0 (LCR[5:3] = 111) in order to detect address bytes. With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate a line status interrupt (IER bit 2 must be set to ‘1’ at this time), and at the same time puts this address byte in the RX FIFO. After the controller examines the byte it must make a decision whether or not to enable the receiver; it should enable the receiver if the address byte addresses its ID address, and must not enable the receiver if the address byte does not address its ID address.

If the controller enables the receiver, the receiver will receive the subsequent data until being disabled by the controller after the controller has received a complete message from the ‘master’ station. If the controller does not disable the receiver after receiving a message from the ‘master’ station, the receiver will generate a parity error upon receiving another address byte. The controller then determines if the address byte addresses its ID address, if it is not, the controller then can disable the receiver. If the address byte addresses the ‘slave’ ID address, the controller take no further action, the receiver will receive the subsequent data.

6.13.3.2 Auto address detection

If Special Character Detect is enabled (EFR[5] is set and the XOFF2 register contains the address byte), the receiver will try to detect an address byte that matches the programmed character in the XOFF2 register. If the received byte is a data byte or an address byte that does not match the programmed character in the XOFF2 register, the receiver will discard these data. Upon receiving an address byte that matches the Xoff2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates a line status interrupt (IER[2] must be set to logic 1 at this time). The receiver will then receive the subsequent data from the 'master' station until being disabled by the controller after having received a message from the 'master' station.

If another address byte is received and this address byte does not match Xoff2 character, the receiver will be automatically disabled and the address byte is ignored. If the address byte matches Xoff2 character, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit (LSR bit 2).

7. Register descriptions

Table 7 details the assigned bit functions for the SC16C852SV internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.24.

Table 7. SC16C852SV internal registers

A3	A2	A1	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General register set[2]													
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	W
0	0	1	IER	00	CTS interrupt[3]	RTS interrupt[3]	Xoff interrupt[3]	Sleep mode[3]	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register	R/W
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB)[3]	TX trigger (LSB)[3]	reserved	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable	W
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	INT priority bit 4	INT priority bit 3	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status	R
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0	R/W
1	0	0	MCR	00	clock select[3]	IRDA enable	reserved	loopback	$\overline{OP2A}$, INT enable	($\overline{OP1A}$)	$\overline{RTS}$	$\overline{DTR}$	R/W
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready	R
1	0	1	EFCR	00	reserved	reserved	reserved	reserved	reserved	Enable extra feature bit-1	Enable extra feature bit-0	Enable TXLVLCNT/ RXLVLCNT	W
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$	R
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Special register set[4]													
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
Second special register set[5]													
0	1	1	TXLVLCNT	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
1	0	0	RXLVLCNT	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R

Table 7. SC16C852SV internal registers *…continued*

A3	A2	A1	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
Enhanced register set[6]													
0	1	0	EFR	00	Auto CTS	Auto RTS	special character select	Enable IER[7:4], ISR[5:4], FCR[5:4], MCR[7:5]	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control	R/W
1	0	0	Xon-1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	1	Xon-2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
1	1	0	Xoff-1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	Xoff-2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
First extra register set[7]													
0	1	0	TXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	0	RXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	FLWCNTH	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	FLWCNTL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Second extra register set[8]													
0	1	0	CLKPRES		reserved	reserved	reserved	reserved	bit 3	bit 2	bit 1	bit 0	R/W
0	1	1	SAMPR[9]	0x00	reserved	reserved	reserved	reserved	reserved	reserved	bit 1	bit 0	R/W
1	0	0	RS485TIME	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	AFCR2	0x00	reserved	reserved	RS485 RTS invert	Auto RS485 RTS	RS485 RTS/DTR	transmitter disable	receiver disable	9-bit enable	R/W
1	1	1	AFCR1	0x00	concurrent write	reserved	reserved	sleep RX LOW	reserved	RTS/CTS mapped to DTR/DSR	software reset	TSR interrupt	R/W

[1] The value shown in represents the register's initialized HEX value; X = not applicable.

[2] Accessible only when LCR[7] is logic 0, and EFCR[2:1] are logic 0.

[3] This bit is only accessible when EFR[4] is set.

[4] Baud rate registers accessible only when LCR[7] is logic 1.

[5] Second special registers are accessible only when EFCR[0] = 1, and EFCR[2:1] are logic 0.

[6] Enhanced Feature Register, Xon1/Xon2 and Xoff1/Xoff2 are accessible only when LCR is set to 0xBF, and EFCR[2:1] are logic 0.

[7] First extra register set is only accessible when EFCR[2:1] = 01b.

[8] Second extra register set is only accessible when EFCR[2:1] = 10b.

[9] The SAMPR must be programmed before the LCR register is programmed.

7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (AD7 to AD0) to the transmit FIFO. The THR empty flag in the LSR will be set to a logic 1 when the transmit FIFO is empty or when data is transferred to the TSR.

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16C852SV receive FIFO by reading the RHR. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the sampling rate. After $^{SAMPR}/_{2}{}^{1}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA, INTB output pins.

Table 8. Interrupt Enable Register bits description

Bit	Symbol	Description
7	IER[7]	CTS interrupt. logic 0 = disable the CTS interrupt (normal default condition) logic 1 = enable the CTS interrupt. The SC16C852SV issues an interrupt when the $\overline{CTS}$ pin transitions from a logic 0 to a logic 1.
6	IER[6]	RTS interrupt. logic 0 = disable the RTS interrupt (normal default condition) logic 1 = enable the RTS interrupt. The SC16C852SV issues an interrupt when the $\overline{RTS}$ pin transitions from a logic 0 to a logic 1.
5	IER[5]	Xoff interrupt. logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition) logic 1 = enable the receive Xoff interrupt
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt

1. SAMPR is the sampling rate of 16×, 8× or 4×.

Table 8. Interrupt Enable Register bits description *...continued*

Bit	Symbol	Description
1	IER[1]	Transmit Holding Register interrupt. In the non-FIFO mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register. In the non-FIFO mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO is enabled (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR, or by loading the THR with new data characters.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, setting IER[3:0] = zeroes puts the SC16C852SV in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs and set the receive FIFO trigger levels.

7.3.1 FIFO mode

Table 9. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	Receive trigger level in 32-byte FIFO mode.[1] These bits are used to set the trigger level for receive FIFO interrupt and flow control. The SC16C852SV will issue a receive ready interrupt when the number of characters in the receive FIFO reaches the selected trigger level. Refer to Table 10.
5:4	FCR[5:4]	Transmit trigger level in 32-byte FIFO mode.[2] These bits are used to set the trigger level for the transmit FIFO interrupt and flow control. The SC16C852SV will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level. Refer to Table 11.
3	FCR[3]	reserved
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO

[1] For 128-byte FIFO mode, refer to Section 7.16, Section 7.17, Section 7.18.

[2] For 128-byte FIFO mode, refer to Section 7.15, Section 7.17, Section 7.18.

Table 10. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level in 32-byte FIFO mode[1]
0	0	8 bytes
0	1	16 bytes
1	0	24 bytes
1	1	28 bytes

[1] When RXINTLVL or TXINTLVL or FLWCNTH or FLWCNTL contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL; see Section 6.4 “FIFO operation”.

Table 11. TX FIFO trigger levels

FCR[5]	FCR[4]	TX FIFO trigger level in 32-byte FIFO mode[1]
0	0	16 bytes
0	1	8 bytes
1	0	24 bytes
1	1	30 bytes

[1] When RXINTLVL or TXINTLVL or FLWCNTH or FLWCNTL contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL; see Section 6.4 “FIFO operation”.

7.4 Interrupt Status Register (ISR)

The SC16C852SV provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 12 “Interrupt source” shows the data values (bits 5:0) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 12. Interrupt source

Priority level	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS change of state

Table 13. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the non-FIFO mode. They are set to a logic 1 when the FIFOs are enabled in the SC16C852SV mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	INT priority bits 4:3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received. logic 0 or cleared = default condition
3:1	ISR[3:1]	INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 12). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)