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SC16IS850L

Single UART with I²C-bus/SPI interface, 128 bytes of transmit and receive FIFOs, IrDA SIR built-in support

Rev. 2 — 18 July 2012 Product data sheet

1. General description

The SC16IS850L is a slave I²C-bus/SPI interface to a single-channel high performance UART. It offers data rates up to 5 Mbit/s and guarantees low operating and sleeping current. The device comes in very small HVQFN24 and TSSOP24 packages, which makes it ideally suitable for handheld, battery operated applications. It also enables seamless protocol conversion from I²C-bus or SPI to and RS-232/RS-485 and are fully bidirectional.

The SC16IS850L supports SPI clock speeds up to 12 Mbit/s, and it supports IrDA SIR up to 115.2 kbit/s. Its internal register set is backward-compatible with the widely used and widely popular 16C850. This allows the software to be easily written or ported from another platform.

The SC16IS850L also provides additional advanced features such as auto hardware and software flow control, automatic RS-485 support, and software reset. This allows the software to reset the UART at any moment, independent of the hardware reset signal.

2. Features and benefits

2.1 General features

- Single full-duplex UART
- Selectable I²C-bus or SPI interface
- 1.8 V operation
- Industrial temperature range: −40 °C to +85 °C
- 128 bytes FIFO (transmitter and receiver)
- Fully compatible with industrial standard 16C450 and equivalent
- Baud rates up to 5 Mbit/s in 16× clock mode
- Auto hardware flow control using RTS/CTS
- Auto software flow control with programmable Xon/Xoff characters
- Single or double Xon/Xoff characters
- Automatic RS-485 support (automatic slave address detection)
- RS-485 driver direction control via $\overline{\text{RTS}}$ signal
- RS-485 driver direction control inversion
- Built-in IrDA encoder and decoder interface
- Supports IrDA SIR with speeds up to 115.2 kbit/s
- Software reset
- Transmitter and receiver can be enabled/disabled independent of each other

- Receive and Transmit FIFO levels
- Programmable special character detection
- Fully programmable character formatting
  - 5-bit, 6-bit, 7-bit or 8-bit character
  - Even, odd, or no parity
  - 1, 1 ½, or 2 stop bits
- Line break generation and detection
- Internal Loopback mode
- Sleep current less than 5 μA at 1.8 V
- Industrial and commercial temperature ranges
- Available in HVQFN24 and TSSOP24 packages

2.2 I²C-bus features

- 400 kbit/s maximum speed
- Compliant with I²C-bus Fast-mode (Fm) speed
- Slave mode only

2.3 SPI features

- Supports 12 Mbit/s maximum SPI clock speed
- Slave mode only
- SPI Mode 0

3. Applications

- Factory automation and process control
- Portable and battery operated devices
- Cellular data devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16IS850LIBS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3
SC16IS850LIPW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Block diagram

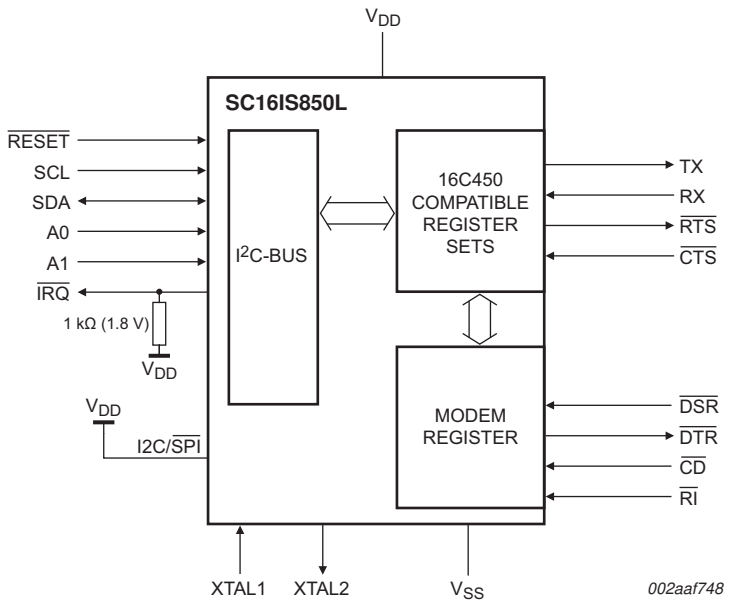


Fig 1. Block diagram of SC16IS850L I²C-bus interface

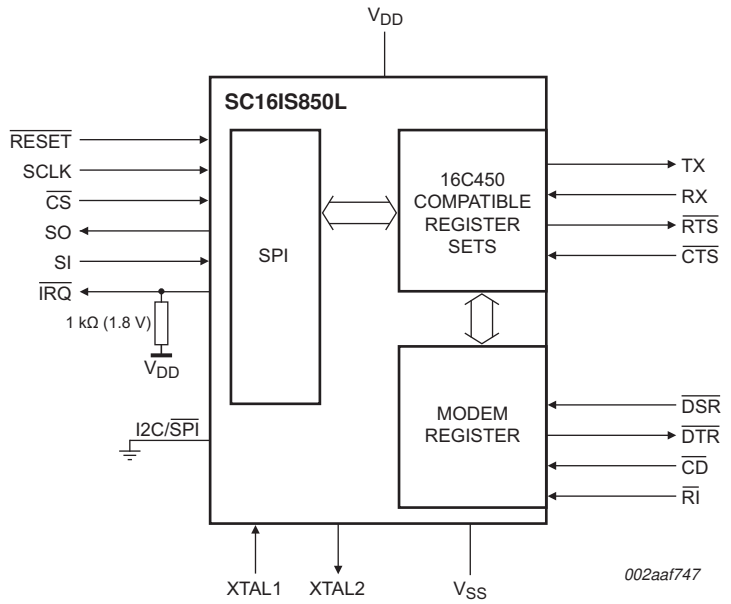


Fig 2. Block diagram of SC16IS850L SPI interface

6. Pinning information

6.1 Pinning

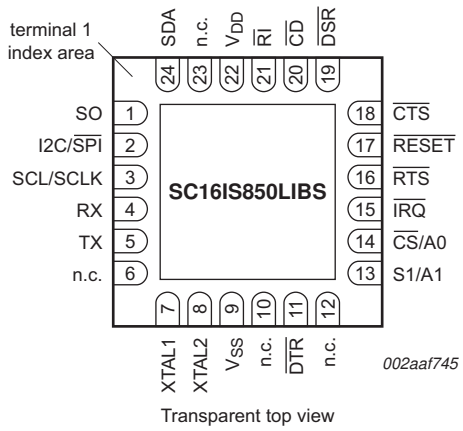


Fig 3. Pin configuration for HVQFN24

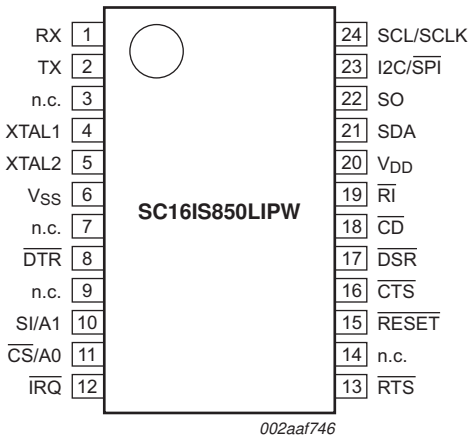


Fig 4. Pin configuration for TSSOP24

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	HVQFN24	TSSOP24		
$\overline{CTS}$	18	16	I	UART clear to send (active LOW). A logic 0 (LOW) on the $\overline{CTS}$ pin indicates the modem or data set is ready to accept transmit data from the SC16IS850L. Status can be tested by reading MSR[4]. This pin only affect the transmit and receive operations when Auto-$\overline{CTS}$ function is enabled via the Enhanced Feature Register EFR[7] for hardware flow control operation.
TX	5	2	O	UART transmitter output. During the local Loopback mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.
RX	4	1	I	UART receiver input. During the local Loopback mode, the RX input pin is disabled and TX data is connected to the UART RX input internally.
$\overline{RESET}$	17	15	I	Device hardware reset (active LOW).
XTAL1	7	4	I	Crystal input or external clock input. Functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 6). Alternatively, an external clock can be connected to this pin.
XTAL2	8	5	O	Crystal output or clock output. (See also XTAL1.) XTAL2 is used as a crystal oscillator output.
V_{DD}	22	20	-	Power supply.

Table 2. Pin description *...continued*

Symbol	Pin		Type	Description
	HVQFN24	TSSOP24		
V_{SS}	9[1]	6	-	Power ground.
I2C/$\overline{SPI}$	2	23	I	I²C-bus or SPI interface select. I²C-bus interface is selected if this pin is at logic HIGH. SPI interface is selected if this pin is at logic LOW. This pin has an internal pull-up resistor, and can be left unconnected if I²C-bus mode is selected.
$\overline{CS}$/A0	14	11	I	SPI chip select or I²C-bus device address select A0. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this pin is the SPI chip select pin (Schmitt-trigger, active LOW). If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin along with A1 pin allows user to change the device's base address. For I²C-bus slave address configuration, please refer to Table 33.
SI/A1	13	10	I	SPI data input pin or I²C-bus device address select A1. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this is the SPI data input pin. If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin along with A0 pin allows user to change the device's base address. For I²C-bus slave address configuration, please refer to Table 33
SO	1	22	O	SPI data output pin. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this is a 3-stateable output pin. If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin function is undefined and must be left as n.c. (not connected).
SCL/SCLK	3	24	I	I²C-bus or SPI input clock.
SDA	24	21	I/O	I²C-bus data input/output, open-drain if I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin. If SPI configuration is selected then this pin is an undefined pin and must be connected to V_{SS}.
$\overline{IRQ}$	15	12	O	Interrupt (open-drain, active LOW). Interrupt is enabled when interrupt sources are enabled in the Interrupt Enable Register (IER). Interrupt conditions include: change of state of the input pins, receiver errors, available receiver buffer data, available transmit buffer space, or when a modem status flag is detected. An external 10 kΩ resistor must be connected between this pin and V_{DD}.

Table 2. Pin description *...continued*

Symbol	Pin		Type	Description
	HVQFN24	TSSOP24		
$\overline{RTS}$	16	13	O	UART request to send (active LOW). A logic 0 on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the Modem Control Register MCR[1] will set this pin to a logic 0, indicating data is available. After reset, this pin is set to a logic 1. This pin only affect the transmit and receive operations when Auto-$\overline{RTS}$ function is enabled via the Enhanced Feature Register (EFR[6]) for hardware flow control operation.
$\overline{DSR}$	19	17	I	Data set ready. DSR is a modem status signal. Its condition can be checked by reading MSR[5]. MSR[1] indicates DSR has changed levels since the last read from the modem status register. If the modem status interrupt is enabled when DSR changes levels, an interrupt is generated.
$\overline{CD}$	20	18	I	Data carrier detect. $\overline{CD}$ is a modem status signal. Its condition can be checked by MSR[7]. MSR[3] indicates that $\overline{CD}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CD}$ changes levels, an interrupt is generated.
$\overline{RI}$	21	19	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading MSR[6]. MSR[2] indicates that $\overline{RI}$ has transitioned from a LOW to a HIGH level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{DTR}$	11	8	O	Data terminal ready. When active (LOW), $\overline{DTR}$ informs a modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the DTR bit of the modem control register. $\overline{DTR}$ is placed in the inactive level either as a result of a Master Reset, during Loopback mode operation, or clearing the DTR bit.
n.c.	6, 10, 12, 23	3, 7, 9, 14	-	Not connected; these pins should be left open.

[1] HVQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Please refer to Figure 1 “Block diagram of SC16IS850L I²C-bus interface”.

The SC16IS850L provides serial asynchronous receive data synchronization, serial-to-serial data conversions for both the transmitter and receiver sections. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The status of the UART can be read at any time during functional operation by the host through either I²C-bus or SPI interface.

The SC16IS850L represents such an integration with greatly enhanced features. The SC16IS850L is fabricated with an advanced CMOS process. The SC16IS850L provides a single UART capability with 128 bytes of transmit and receive FIFO memory, instead of 64 bytes for the SC16IS750. The SC16IS850L is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16IS850L by transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable receive and transmit FIFO trigger interrupt levels are provided in 16C650 mode, or 128 programmable levels are provided in the extended mode for maximum data throughput performance especially when operating in a multi-channel environment (see ”Section 7.1 “Extended mode (128-byte FIFO)”). The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU and increases performance. Sleep mode function in the SC16IS850L allows the UART to be placed under low power mode when the serial data input line, RX, is idle, TX FIFO and Transmit Shift Registers are empty, and there is no interrupt pending except THR. The UART is capable of operation up to 5 Mbit/s with an external 80 MHz clock. With a crystal, the SC16IS850L is capable of operation up to 1.5 Mbit/s.

The rich feature set of the SC16IS850L is available through internal registers. These features are: selectable and programmable receive and transmit FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls, and are all standard features. Following a power-on reset, an external reset, or a software reset, the SC16IS850L is software compatible with the previous generation, SC16C550B, and SC16C650B.

The SC16IS850L has selectable hardware flow control and software flow control. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the $\overline{RTS}$ output and $\overline{CTS}$ input signals. Software flow control automatically controls data flow by using programmable Xon/Xoff characters. The UART includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and $(2^{16} - 1)$.

7.1 Extended mode (128-byte FIFO)

The device is in the extended mode when any of these four registers contains any value other than 0: FLWCNTH, FLWCNTL, TXINTLVL, RXINTLVL.

7.2 Internal registers

The SC16IS850L provides a set of 25 internal registers for monitoring and controlling the functions of the UART. These registers are shown in Table 3.

Table 3. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, EFCR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Extra Feature Control Register (EFCR)
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Second special register set (TXLVLCNT/RXLVLCNT)[3]				
0	1	1	Transmit FIFO Level Count	n/a
1	0	0	Receive FIFO Level Count	n/a
Enhanced feature register set (EFR, Xon1/Xon2, Xoff1/Xoff2)[4]				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon1 word	Xon1 word
1	0	1	Xon2 word	Xon2 word
1	1	0	Xoff1 word	Xoff1 word
1	1	1	Xoff2 word	Xoff2 word
First extra feature register set (TXINTLVL/RXINTLVL, FLWCNTH/FLWCNTL)[5]				
0	1	0	Transmit FIFO Interrupt Level	Transmit FIFO Interrupt Level
1	0	0	Receive FIFO Interrupt Level	Receive FIFO Interrupt Level
1	1	0	Flow Control Count High	Flow Control Count High
1	1	1	Flow Control Count Low	Flow Control Count Low
Second extra feature register set (CLKPRES, RS485TIME, AFCR2, AFCR1)[6]				
0	1	0	Clock Prescaler	Clock Prescaler
1	0	0	RS-485 turn-around Timer	RS-485 turn-around Timer
1	1	0	Additional Feature Control Register 2	Additional Feature Control Register 2
1	1	1	Additional Feature Control Register 1	Additional Feature Control Register 1

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Second Special registers are accessible only when EFCR[0] = 1.

[4] Enhanced Feature Registers are only accessible when LCR = 0xBF.

[5] First Extra Feature Registers are only accessible when EFCR[2:1] = 01b.

[6] Second Extra Feature Registers are only accessible when EFCR[2:1] = 10b.

7.3 FIFO operation

7.3.1 32-byte FIFO mode

When all four of these registers (TXINTLVL, RXINTLVL, FLWCNTH, FLWCNTL) in the 'first extra feature register set' are empty (0x00) the transmit and receive trigger levels are set by FCR[7:4]. In this mode the transmit and receive trigger levels are backward compatible to the SC16C650B (see Table 4), and the FIFO sizes are 32 entries. The transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). It should be noted that the user can set the transmit trigger levels by writing to the FCR, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU (see Section 7.7). Please refer to Table 9 and Table 10 for the setting of FCR[7:4].

Table 4. Interrupt trigger level and flow control mechanism

FCR[7:6]	FCR[5:4]	INT pin activation		Negate $\overline{RTS}$ or send Xoff	Assert $\overline{RTS}$ or send Xon
		RX	TX		
00	00	8	16	8	0
01	01	16	8	16	7
10	10	24	24	24	15
11	11	28	30	28	23

7.3.2 128-byte FIFO mode

When either TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the 'first extra feature register set' contains any value other than 0x00, the transmit and receive trigger levels are set by TXINTLVL and RXINTLVL registers. TXINTLVL sets the trigger levels for the transmit FIFO, and the transmit trigger levels can be set to any value between 1 and 128 with granularity of 1. RXINTLVL sets the trigger levels for the receive FIFO, the receive trigger levels can be set to any value between 1 and 128 with granularity of 1.

When the effective FIFO size changes (that is, when FCR[0] toggles or when the combined content of TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL changes between equal and unequal to 0x00), both RX FIFO and TX FIFO will be reset (data in the FIFO will be lost).

7.4 Hardware flow control

When automatic hardware flow control is enabled, the SC16IS850L monitors the $\overline{CTS}$ pin for a remote buffer overflow indication and controls the $\overline{RTS}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If $\overline{CTS}$ transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[7:6]), and the SC16IS850L will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTS}$ input returns to a logic 0, indicating more data may be sent.

When AFCR1[2] is set to logic 1 then the function of $\overline{CTS}$ pin is mapped to the $\overline{DSR}$ pin, and the function of $\overline{RTS}$ is mapped to $\overline{DTR}$ pin. $\overline{DSR}$ and $\overline{DTR}$ pins will behave as described above for $\overline{CTS}$ and $\overline{RTS}$.

With the automatic hardware flow control function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$) pin will not be forced to a logic 1 ($\overline{\text{RTS}}$ off), until the receive FIFO reaches the next trigger level. However, the $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$) pin will return to a logic 0 after the receive buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. Under the above described conditions, the SC16IS850L will continue to accept data until the receive FIFO is full.

When the TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL in the 'first extra feature register set' are all zeroes, the hardware and software flow control trigger levels are set by FCR[7:4]; see Table 4.

When the TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the 'first extra feature register set' contain any value other than 0x00, the hardware and software flow control trigger levels are set by FLWCNTH and FLWCNTL. The content in FLWCNTH determines how many bytes are in the receive FIFO before $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$) is de-asserted or Xoff is sent. The content in FLWCNTL determines how many bytes are in the receive FIFO before $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$) is asserted, or Xon is sent.

In 128-byte FIFO mode, hardware and software flow control trigger levels can be set to any value between 1 and 128 in granularity of 1. The value of FLWCNTH should always be greater than FLWCNTL. The UART does not check for this condition automatically, and if this condition is not met, spurious operation of the device might occur. When using FLWCNTH and FLWCNTL, these registers must be initialized to proper values before hardware or software flow control is enabled via the EFR register.

7.5 Software flow control

When software flow control is enabled, the SC16IS850L compares one or two sequentially received data characters with the programmed Xon or Xoff character value(s). If the received character(s) match the programmed Xoff values, the SC16IS850L will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, ISR bit 4 will be set (if enabled via IER[5]) and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16IS850L will monitor the receive data stream for a match to the Xon1/Xon2 character value(s). If a match is found, the SC16IS850L will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions (see Table 22). When double 8-bit Xon/Xoff characters are selected, the SC16IS850L compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the receive FIFO. When using software flow control, the Xon/Xoff characters cannot be used for data transfer.

In the event that the receive buffer is overfilling, the SC16IS850L automatically sends an Xoff character (when enabled) via the serial TX output to the remote UART. The SC16IS850L sends the Xoff1/Xoff2 characters as soon as the number of received data in

the receive FIFO passes the programmed trigger level. To clear this condition, the SC16IS850L will transmit the programmed Xon1/Xon2 characters as soon as the number of characters in the receive FIFO drops below the programmed trigger level.

7.6 Special character detect

A special character detect feature is provided to detect an 8-bit character when EFR[5] is set. When an 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[3:0] (see Table 22). Note that software flow control should be turned off when using this special mode by setting EFR[3:0] to all zeroes.

The SC16IS850L compares each incoming receive character with Xoff2 data. If a match occurs, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although Table 6 “SC16IS850L internal registers” shows Xon1, Xon2, Xoff1, Xoff2 with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[1:0] define the number of character bits, that is, either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[1:0] also determines the number of bits that will be used for the special character comparison. Bit 0 in Xon1, Xon2, Xoff1, Xoff2 corresponds with the LSB bit for the received character.

7.7 Interrupt priority and time-out interrupts

The interrupts are enabled by IER[7:0]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC16IS850L will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The ISR indicates the current singular highest priority interrupt only. A condition can exist where a higher priority interrupt masks the lower priority interrupt(s) (see Table 11). Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]), and it is important to serve these interrupts correctly. The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16IS850L FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] to see if there are any additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

7.8 Programmable baud rate generator

The SC16IS850L UART contains a programmable rational baud rate generator that takes any clock input and divides it by a divisor in the range between 1 and ($2^{16} - 1$). The SC16IS850L offers the capability of dividing the input frequency by rational divisor. The fractional part of the divisor is controlled by the CLKPRES register in the 'first extra feature register set'.

$$baud\ rate = \frac{f_{XTAL1}}{MCR[7] \times \left[16 \times \left(N + \frac{M}{16}\right)\right]} \quad (1)$$

where:

N is the integer part of the divisor in DLL and DLM registers;

M is the fractional part of the divisor in CLKPRES register;

f_{XTAL1} is the clock frequency at XTAL1 pin.

Prescaler = 1 when MCR[7] is set to 0.

Prescaler = 4 when MCR[7] is set to 1.

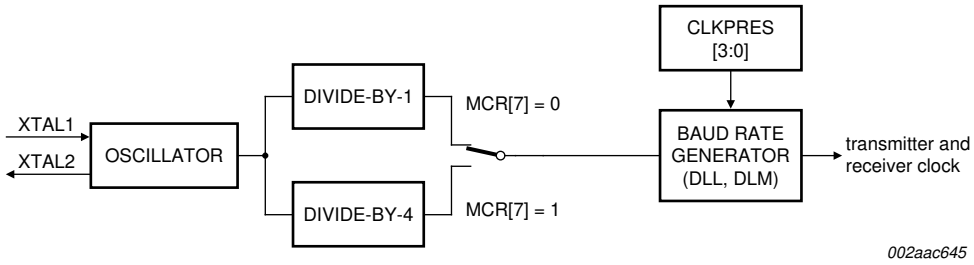


Fig 5. Prescalers and baud rate generator block diagram

A single baud rate generator is provided for the transmitter and receiver. The programmable Baud Rate Generator is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC16IS850L can be configured for internal or external clock operation. For internal clock operation, an industry standard crystal is connected externally between the XTAL1 and XTAL2 pins (see Figure 6). Alternatively, an external clock can be connected to the XTAL1 pin (see Figure 7) to clock the internal baud rate generator for standard or custom rates (see Table 5).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16IS850L divides the basic external clock by 16. The baud rate is configured via the CLKPRES, DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of the baud rate generator.

Programming the baud rate generator registers CLKPRES, DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows the selectable baud rate table available when using a 1.8432 MHz external clock input when MCR[7] = 0, and CLKPRES = 0x00.

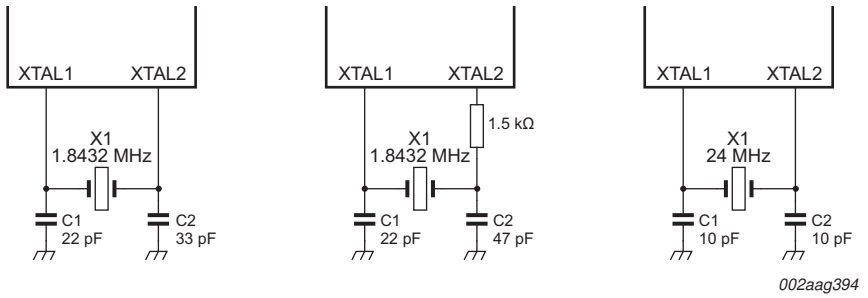
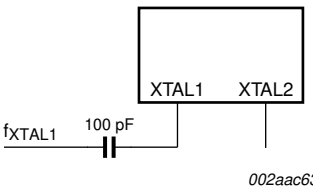


Fig 6. Crystal oscillator connection



If f_{XTAL1} frequency is greater than 50 MHz, then a DC blocking capacitor is required.

XTAL2 pin should be left unconnected when an external clock is used.

Fig 7. External clock connection

Table 5. Baud rate generator programming table using a 1.8432 MHz clock when MCR[7] = 0 and CLKPRES[3:0] = 0

Output baud rate (bit/s)	Output 16× clock divisor (decimal)	Output 16× clock divisor (hexadecimal)	DLM program value (hexadecimal)	DLL program value (hexadecimal)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1.2 k	96	60	00	60
2.4 k	48	30	00	30
3.6 k	32	20	00	20
4.8 k	24	18	00	18
7.2 k	16	10	00	10
9.6 k	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

7.9 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally (see Figure 8). MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, the transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally. The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, MCR[3] ($\overline{OP2}$) and MCR[2] ($\overline{OP1}$). Loopback test data is entered into the transmit holding register via the user data bus interface, D[7:0]. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D[7:0]. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the interrupt pin is 3-stated, therefore, the software must use the polling method (see Section 8.2.2) to send and receive data.

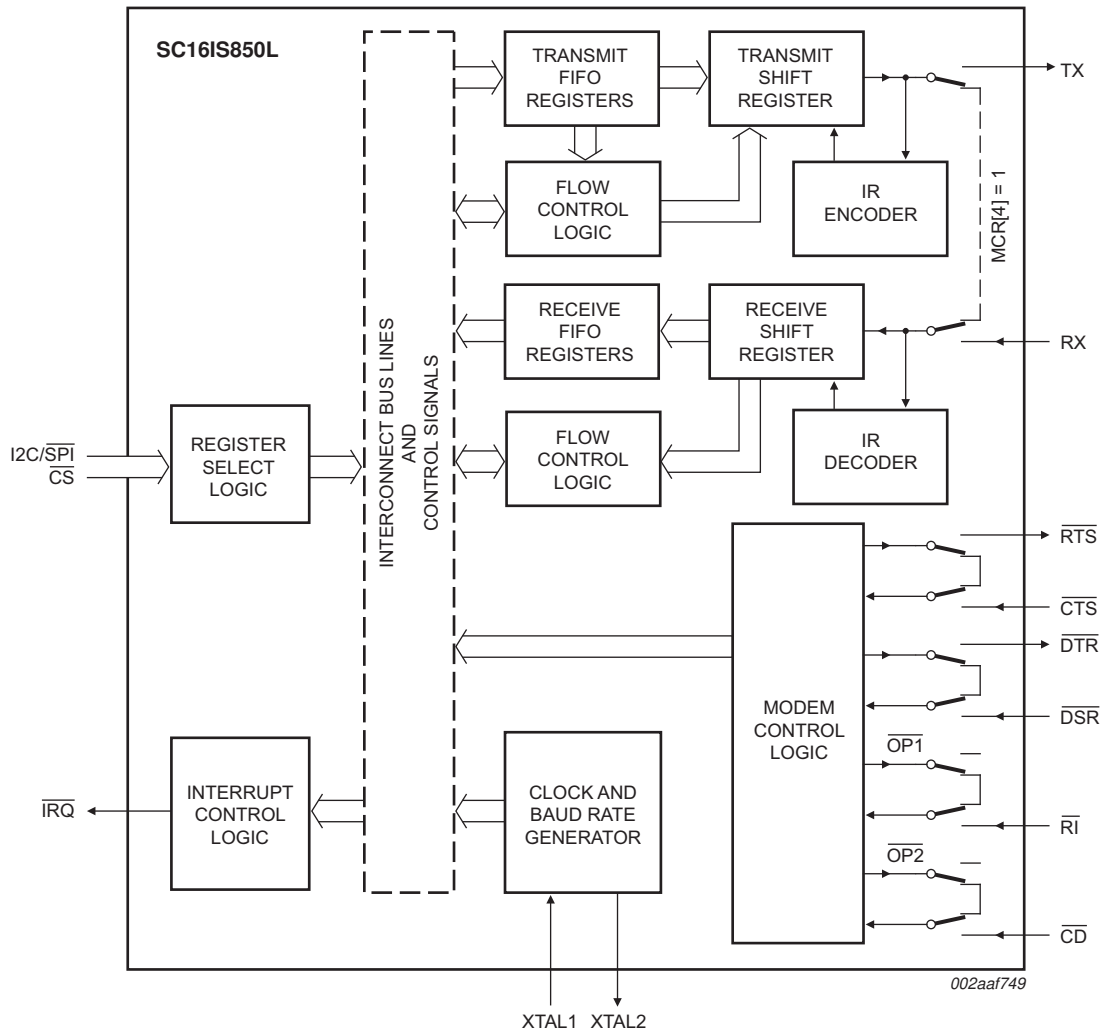


Fig 8. Internal Loopback mode diagram

7.10 Sleep mode

Sleep mode is an enhanced feature of the SC16IS850L UART. It is enabled when EFR[4], the enhanced functions bit, is set **and** when IER[4] bit is set.

7.10.1 Conditions to enter Sleep mode

Sleep mode is entered when:

- Modem input pins are not toggling.
- The serial data input line, RX, is idle for 4 character time (logic HIGH) and AFCR1[4] is logic 0. When AFCR1[4] is logic 1 the device will go to sleep regardless of the state of the RX pin (see Section 8.21 for the description of AFCR1 bit 4).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending.
- The RX FIFO is empty.

In Sleep mode, the UART clock and baud rate clock are stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced.

Remark: Writing to the divisor latches, DLL and DLM, to set the baud clock, must not be done during Sleep mode. Therefore, it is advisable to disable Sleep mode using IER[4] before writing to DLL or DLM.

7.10.2 Conditions to resume normal operation

SC16IS850L resumes normal operation by any of the following:

- Receives a start bit on RX pin.
- Data is loaded into transmit FIFO.
- A change of state on any of the modem input pins

If the device is awakened by one of the conditions described above, it will return to the Sleep mode automatically after all the conditions described in Section 7.10.1 are met. The device will stay in Sleep mode until it is disabled by setting any channel's IER bit 4 to a logic 0.

Wake-up by serial data on RX input pin is supported in UART mode but not in IrDA mode. Refer to application note *AN19064, "How to wake up SC16IS740/750/760 in IrDA mode"* for a software procedure to wake up the device by receiving data in IrDA mode.

When the SC16IS850L is in Sleep mode and the host data bus (D[7:0], A[2:0], $\overline{IOW}$, $\overline{IOR}$, $\overline{CS}$) remains in steady state, either HIGH or LOW, the Sleep mode supply current will be in the μA range as specified in Table 37 "Static characteristics". If any of these signals is toggling or floating then the sleep current will be higher.

7.11 RS-485 features

7.11.1 Auto RS-485 $\overline{\text{RTS}}$ control

Normally the $\overline{\text{RTS}}$ pin is controlled by MCR[1], or if hardware flow control is enabled, the logic state of the $\overline{\text{RTS}}$ pin is controlled by the hardware flow control circuitry. AFCR2[4] will take the precedence over the other two modes; once this bit is set, the transmitter will control the state of the $\overline{\text{RTS}}$ pin. The transmitter automatically asserts the $\overline{\text{RTS}}$ pin (logic 0) once the host writes data to the transmit FIFO, and de-asserts $\overline{\text{RTS}}$ pin (logic 1) once the last bit of the data has been transmitted.

To use the auto RS-485 $\overline{\text{RTS}}$ mode the software would have to disable the hardware flow control function.

7.11.2 RS-485 $\overline{\text{RTS}}$ inversion

AFCR2[5] reverses the polarity of the $\overline{\text{RTS}}$ pin if the UART is in auto RS-485 $\overline{\text{RTS}}$ mode.

When the transmitter has data to be sent it will de-asserts the $\overline{\text{RTS}}$ pin (logic 1), and when the last bit of the data has been sent out the transmitter asserts the $\overline{\text{RTS}}$ pin (logic 0).

7.11.3 Auto 9-bit mode (RS-485)

AFCR2[0] is used to enable the 9-bit mode (Multi-drop or RS-485 mode). In this mode of operation, a ‘master’ station transmits an address character followed by data characters for the addressed ‘slave’ stations. The slave stations examine the received data and interrupt the controller if the received character is an address character (parity bit = 1).

To use the automatic 9-bit mode, the software would have to disable the hardware and software flow control functions.

7.11.3.1 Normal Multi-drop mode

The 9-bit Mode in AFCR2[0] is enabled, but not Special Character Detect (EFR[5]). The receiver is set to Force Parity 0 (LCR[5:3] = 111) in order to detect address bytes.

With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate a line status interrupt (IER[2] must be set to ‘1’ at this time), and at the same time puts this address byte in the RX FIFO. After the controller examines the byte it must make a decision whether or not to enable the receiver; it should enable the receiver if the address byte addresses its ID address, and must not enable the receiver if the address byte does not address its ID address.

If the controller enables the receiver, the receiver will receive the subsequent data until being disabled by the controller after the controller has received a complete message from the ‘master’ station. If the controller does not disable the receiver after receiving a message from the ‘master’ station, the receiver will generate a parity error upon receiving another address byte. The controller then determines if the address byte addresses its ID address, if it is not, the controller then can disable the receiver. If the address byte addresses the ‘slave’ ID address, the controller takes no further action, and the receiver will receive the subsequent data.

7.11.3.2 Auto address detection

If Special Character Detect is enabled (EFR[5] is set and the Xoff2 register contains the address byte) the receiver will try to detect an address byte that matches the programmed character in the Xoff2 register. If the received byte is a data byte or an address byte that does not match the programmed character in the Xoff2 register, the receiver will discard these data. Upon receiving an address byte that matches the Xoff2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates a line status interrupt (IER[2] must be set to '1' at this time). The receiver will then receive the subsequent data from the 'master' station until being disabled by the controller after having received a message from the 'master' station.

If another address byte is received and this address byte does not match the Xoff2 character, the receiver will be automatically disabled and the address byte is ignored. If the address byte matches the Xoff2 character, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit (LSR bit 2).

8. Register descriptions

Table 6 details the assigned bit functions for the SC16IS850L internal registers. The assigned bit functions are more fully defined in Section 8.1 through Section 8.23.

Table 6. SC16IS850L internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General register set[2]													
0	0	0	RHR	0xXX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0	0	0	THR	0xXX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	W
0	0	1	IER	0x00	CTS interrupt[3]	RTS interrupt[3]	Xoff interrupt[3]	Sleep mode[3]	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register interrupt	R/W
0	1	0	FCR	0x00	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB)[3]	TX trigger (LSB)[3]	reserved	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable	W
0	1	0	ISR	0x01	FIFOs enabled	FIFOs enabled	INT priority bit 4	INT priority bit 3	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status	R
0	1	1	LCR	0x00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0	R/W
1	0	0	MCR	0x00	clock select[3]	IrDA enable	reserved	loopback	$\overline{OP2}$	$\overline{OP1}$	$\overline{RTS}$	$\overline{DTR}$	R/W
1	0	1	LSR	0x60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready	R
1	0	1	EFCR	0x00	reserved	reserved	reserved	reserved	reserved	Enable extra feature bit 1	Enable extra feature bit 0	Enable TXLVLCNT/ RXLVLCNT	W
1	1	0	MSR	0xX0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$	R
1	1	1	SPR	0xFF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Special register set[4]													
0	0	0	DLL	0xXX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0	0	1	DLM	0xXX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
Second special register set[6]													
0	1	1	TXLVLCNT	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
1	0	0	RXLVLCNT	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R

Table 6. SC16IS850L internal registers *…continued*

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
Enhanced feature register set[5]													
0	1	0	EFR	0x00	Auto CTS	Auto RTS	special character select	Enable IER[7:4], ISR[5:4], FCR[5:4], MCR[7:5]	Cont-3 TX, RX Control	Cont-2 TX, RX Control	Cont-1 TX, RX Control	Cont-0 TX, RX Control	R/W
1	0	0	Xon1	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	1	Xon2	0x00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
1	1	0	Xoff1	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	Xoff2	0x00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
First extra feature register set[7]													
0	1	0	TXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	0	RXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	FLWCNTH	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	FLWCNTL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Second extra feature register set[8]													
0	1	0	CLKPRES	0x00	reserved	reserved	reserved	reserved	bit 3	bit 2	bit 1	bit 0	R/W
1	0	0	RS485TIME	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	AFCR2	0x00	reserved	reserved	RS485 RTS Invert	Auto RS485 RTS	RS485 RTS/DTR	Transmitter Disable	Receiver Disable	9-bit Enable	R/W
1	1	1	AFCR1	0x00	reserved	reserved	reserved	Sleep RXLow	reserved	RTS/CTS mapped to DTR/DSR	Software Reset	TSR Interrupt	R/W

[1] The value shown represents the register's initialized HEX value; X = not applicable.

[2] Accessible only when LCR[7] is logic 0, and EFCR[2:1] are logic 0.

[3] This bit is only accessible when EFR[4] is set.

[4] Baud rate registers accessible only when LCR[7] is logic 1.

[5] Enhanced Feature Register, Xon1/Xon2 and Xoff1/Xoff2 are accessible only when LCR is set to 0xBF, and EFCR[2:1] are logic 0.

[6] Second Special registers are accessible only when EFCR[0] = 1, and EFCR[2:1] are logic 0.

[7] First extra feature register set is only accessible when EFCR[2:0] = 010b.

[8] Second extra feature register set is only accessible when EFCR[2:0] = 100b.

8.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data byte [D7:D0] to the transmit FIFO. The THR empty flag in the LSR will be set to a logic 1 when the transmit FIFO is empty or when data is transferred to the TSR.

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16IS850L receive FIFO by reading the RHR. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

8.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT output pin.

Table 7. Interrupt Enable Register bits description

Bit	Symbol	Description
7	IER[7]	CTS interrupt. logic 0 = disable the CTS interrupt (normal default condition) logic 1 = enable the CTS interrupt. The SC16IS850L issues an interrupt when the $\overline{\text{CTS}}$ pin transitions from a logic 0 to a logic 1.
6	IER[6]	RTS interrupt. logic 0 = disable the RTS interrupt (normal default condition) logic 1 = enable the RTS interrupt. The SC16IS850L issues an interrupt when the $\overline{\text{RTS}}$ pin transitions from a logic 0 to a logic 1.
5	IER[5]	Xoff interrupt. logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition) logic 1 = enable the receive Xoff interrupt
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt

Table 7. Interrupt Enable Register bits description *…continued*

Bit	Symbol	Description
1	IER[1]	Transmit Holding Register interrupt. In the non-FIFO mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register interrupt. In the non-FIFO mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

8.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO is enabled (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR, or by loading the THR with new data characters.

8.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, setting IER[3:0] puts the SC16IS850L in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

8.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, and set the receive FIFO trigger levels.

8.3.1 FIFO mode

Table 8. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	Receive trigger level in 32-byte FIFO mode[1]. These bits are used to set the trigger levels for receive FIFO interrupt and flow control. The SC16IS850L will issue a receive ready interrupt when the number of characters in the receive FIFO reaches the selected trigger level. Refer to Table 9.
5:4	FCR[5:4]	Transmit trigger level in 32-byte FIFO mode[2]. These bits are used to set the trigger level for the transmit FIFO interrupt and flow control. The SC16IS850L will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level. Refer to Table 10.
3	FCR[3]	reserved
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO

[1] For 128-byte FIFO mode, refer to Section 8.16, Section 8.17, Section 8.18.

[2] For 128-byte FIFO mode, refer to Section 8.15, Section 8.17, Section 8.18.

Table 9. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level (bytes) in 32-byte FIFO mode[1]
0	0	8
0	1	16
1	0	24
1	1	28

[1] When RXINTLVL, TXINTLVL, FLWCNTL or FLWCNTH contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL registers (see Section 7.3 “FIFO operation”).

Table 10. TX FIFO trigger levels

FCR[5]	FCR[4]	TX FIFO trigger level (bytes) in 32-byte FIFO mode[1]
0	0	16
0	1	8
1	0	24
1	1	30

[1] When RXINTLVL, TXINTLVL, FLWCNTL or FLWCNTH contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL registers (see Section 7.3 “FIFO operation”).

8.4 Interrupt Status Register (ISR)

The SC16IS850L provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 11 “Interrupt source” shows the data values (bits 5:0) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 11. Interrupt source

Priority level	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS change of state

Table 12. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the non-FIFO mode. They are set to a logic 1 when the FIFOs are enabled in the SC16IS850L mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	INT priority bits 4:3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received. logic 0 or cleared = default condition
3:1	ISR[3:1]	INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 11). logic 0 or cleared = default condition

Table 12. Interrupt Status Register bits description *…continued*

Bit	Symbol	Description
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

8.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 13. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5:3	LCR[5:3]	Programs the parity conditions (see Table 14).
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 15). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 16). logic 0 or cleared = default condition

Table 14. LCR[5:3] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
0	0	1	odd parity
0	1	1	even parity
1	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 15. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	1½
1	6, 7, 8	2