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SC196
1.5A Synchronous Buck Converter with Integrated Power Devices

POWER MANAGEMENT

Description

The SC196 is a synchronous step-down converter with integrated power devices designed for use in applications using a single-cell Li-ion battery. Its wide input voltage range also makes it suitable for use in systems with fixed 3.3V or 5V supply rails available. The switching frequency is nominally set to 1MHz, allowing the use of small inductors and capacitors. The current rating of the internal MOSFET switches allows a DC output current of 1.5A.

The output voltage is set by connecting a resistor divider from the filter inductor to the feedback pin. See the SC196A for pin-programmable output voltages.

The SC196 has a flexible clocking methodology that allows it to be synchronized to an external oscillator or controlled by the internal oscillator. The device operates in either forced PWM mode or in PSAVE mode. If PSAVE mode is enabled, the part will automatically enter PFM at light loads to maintain maximum efficiency across the full load range.

For noise sensitive applications, PSAVE mode can be disabled by synchronizing to an external oscillator or pulling the SYNC/PWM pin high. Shutdown turns off all the control circuitry to achieve a typical shutdown current of 0.1µA.

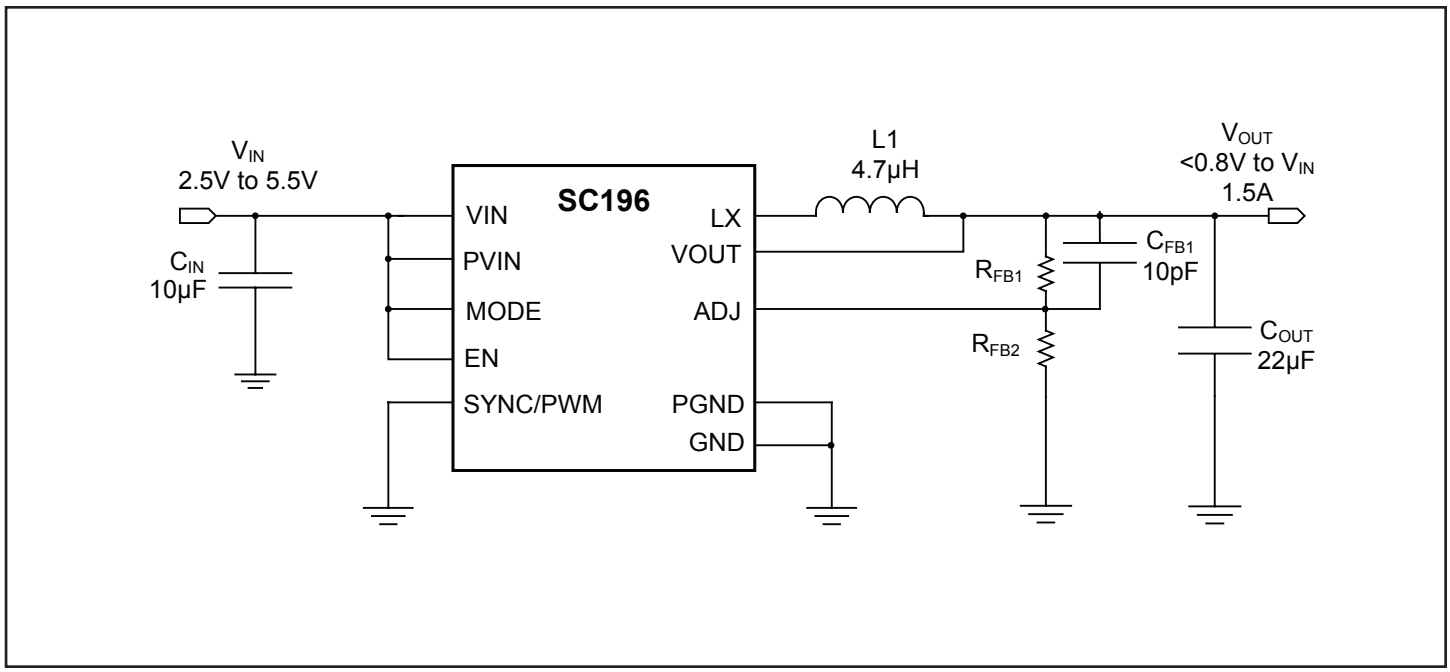
Features

- Up to 95% efficiency
- V_{OUT} adjustable from less than 0.8V to V_{IN}
- Output current — 1.5A
- Input range — 2.5V to 5.5V
- Quiescent current — 17µA
- Fixed 1MHz frequency or 750kHz to 1.25MHz synchronized operation
- PSAVE operation to maximize efficiency at light loads
- Shutdown current <1µA
- Fast transient response
- 100% duty cycle in dropout
- Soft-start
- Over-temperature and short-circuit protection
- Lead-free package — MLPD10-UT, 3 x 3 x 0.6 mm

Applications

- Cell phones
- Wireless communication chipset power
- Personal media players
- Microprocessor/DSP core/IO power
- PDAs and handheld computers
- WLAN peripherals
- USB powered modems
- 1 Li-Ion or 3 NiMH/NiCd powered devices

Typical Application Circuit



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-0.3 to 7	V
Logic Inputs (N=SYNC/PWM, EN, MODE)	V_N	-0.3 to V_{IN}+0.3, 7V Max	V
Output Voltage	V_{OUT}	-0.3 to V_{IN}+0.3, 7V Max	V
ADJ Input	V_{ADJ}	-0.3 to V_{IN}+0.3, 7V Max	V
LX Voltage	V_{LX}	-1 to V_{IN} +1, 7V Max	V
Thermal Impedance Junction to Ambient(1)	θ_{JA}	40	°C/W
VOUT Short-Circuit to GND	t_{SC}	Continuous	s
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature	T_S	-65 to +150	°C
Junction Temperature	T_J	-40 to +150	°C
Peak IR Reflow Temperature	T_{PKG}	260	°C
ESD Protection Level (2)	V_{ESD}	2	kV

Notes:
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless otherwise noted: V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = V_{IN}, SYNC/PWM = V_{IN}, MODE = V_{IN}, T_A = -40 to 85°C. Typical values are at T_A = 25°C.

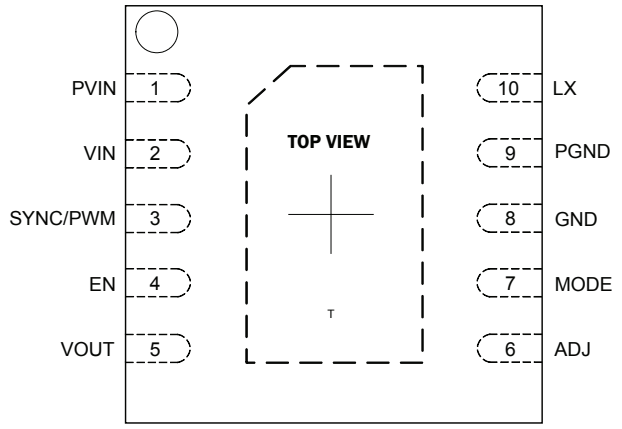
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.5		5.5	V
UVLO Threshold (upper)	V_{UVL}		2.18	2.3	2.45	V
UVLO Hysteresis	V_{UVLHYS}			150		mV
Output Voltage Range	V_{OUT}		0.8		V_{IN}	V
FB Voltage Tolerance	V_{FB}	V_{IN} = 2.5V to 5.5V, I_{OUT} = 0mA to 1.5A	0.485	0.5	0.515	V
Load Regulation (PWM)	$V_{OUT\ LOAD}$	I_{OUT} = 0mA to 1.5A		±0.5	±1	%
PSAVE Regulation	$V_{OUT\ PSAVE}$	SYNC/PWM=GND,C_{OUT} = 22µF, V_{IN} = 2.5V to 5.5V, I_{OUT} = 0mA to 1.5A		±2	±3	%
P-Channel Current Limit	$I_{LIM(P)}$	V_{IN}=2.5V to 5.5V	1.96	2.8	3.57	A
Quiescent Current	I_Q	SYNC/PWM = GND, I_{OUT} = 0A, V_{OUT} = 1.04 x $V_{OUT(Programmed)}$		17	28	µA
Shutdown Current	I_{SD}	EN = GND, LX = OPEN		0.1	1	µA

Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
P-Channel On Resistance	R_{DSP}	I_{LX} = 100mA		0.275		Ω
N-Channel On Resistance	R_{DSN}	I_{LX} = 100mA		0.165		Ω
LX Leakage Current PMOS	I_{LXP}	LX = GND, EN = GND		0.1	2	µA
LX Leakage Current NMOS	I_{LXN}	LX = 3.6V, EN = GND	-2	0.1		µA
Oscillator Frequency	f_{OSC}		0.85	1.0	1.15	MHz
SYNC Frequency (upper)	f_{SYNCU}		1.25			MHz
SYNC Frequency (lower)	f_{SYNCL}				750	kHz
Start-Up Time	t_{START}				5	ms
Thermal Shutdown	T_{SD}			145		°C
Thermal Shutdown Hysteresis	T_{SD-HYS}			10		°C
Logic Input High(1)	V_{IH}		1.2			V
Logic Input Low(1)	V_{IL}				0.4	V
Logic Input Current High(1)	I_{IH}		-2	0.1	2	µA
Logic Input Current Low(1)	I_{IL}		-2	0.1	2	µA

Note:
(1) For EN, SYNC/PWM, MODE

Pin Configuration



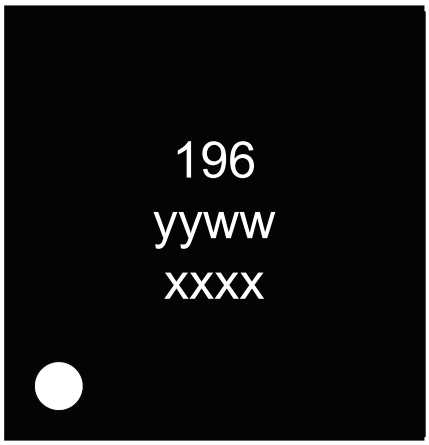
MLPD-UT: 3X3X0.6, 10 LEAD

Ordering Information

DEVICE	PACKAGE
SC196ULTRT(1)(2)	MLPD-UT10 3x3x0.6
SC196EVB	Evaluation Board

Notes:
1) Lead-free packaging only. This product is fully WEEE and RoHS compliant.
2) Available in tape and reel only. A reel contains 3000 devices.

Marking Information

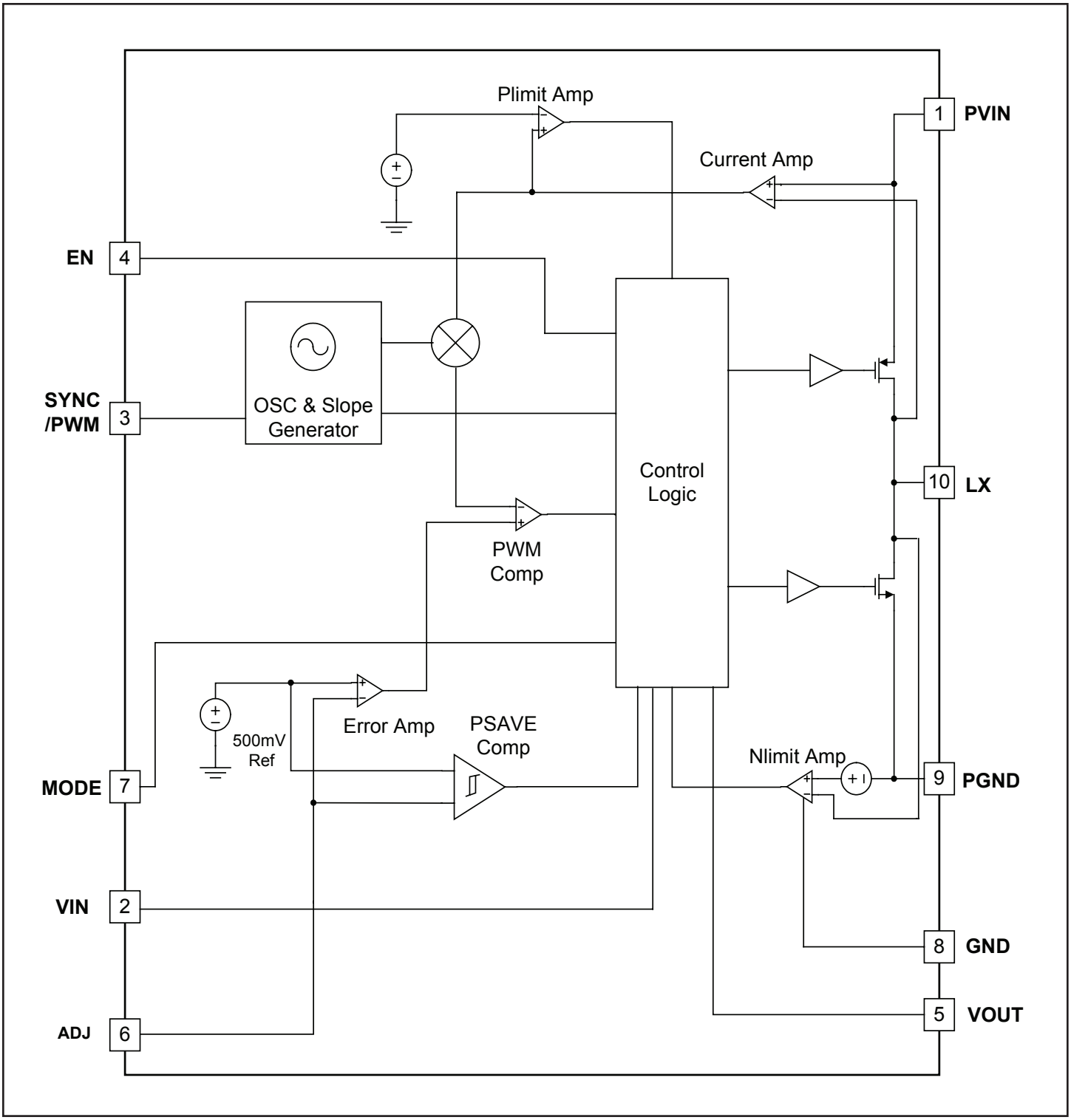


yy = two digit year of manufacture
ww = two digit week of manufacture
xxxx = lot number

Pin Descriptions

Pin #	Pin Name	Pin Function
1	PVIN	Input supply voltage connection to switching FETs — connect the input capacitor between this pin and PGND directly.
2	VIN	Input supply voltage for control circuits
3	SYNC/PWM	Oscillator synchronization input. Tie to V_{IN} for forced PWM mode or GND to allow the part to enter PSAVE mode at light loads. Apply an external clock signal for frequency synchronization.
4	EN	Enable digital input; a high input enables the SC196, a low disables and reduces quiescent current to less than 1µA. In shutdown, LX becomes high impedance.
5	VOUT	Regulated output voltage sense pin — connect to the output capacitor allowing sensing of the output voltage.
6	ADJ	Output Voltage Adjust and feedback compensation pin - connect resistor divider between this pin and GND to set the desired output voltage level.
7	MODE	MODE select pin — MODE = V_{IN} to select 100% duty cycle function, MODE = GND to disable this function.
8	GND	Ground
9	PGND	Power Ground
10	LX	Inductor connection to the switching FETs
T	THERMAL PAD	Pad for heatsinking purposes — not connected internally. Connects to ground plane using multiple vias.

Block Diagram



Applications Information

SC196 Detailed Description

The SC196 is a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter utilizing a 1MHz fixed-frequency current mode architecture. The device is designed to operate in a fixed-frequency PWM mode across the full load range and can enter Power Save Mode (PSAVE), utilizing Pulse Frequency Modulation (PFM) at light loads to maximize efficiency.

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. Current feedback for the switching regulator uses the PMOS current path, and it is amplified and summed with the internal slope compensation network. The voltage feedback loop uses an external feedback divider. The on-time is determined by comparing the summed current feedback and the output of the error amplifier. The period is set by the onboard oscillator or by an external clock attached to the SYNC/PWM pin.

The SC196 has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin.

Output Voltage Selection

The output voltage can be programmed using a resistor network connected from VOUT to ADJ to GND. The combined resistance of the divider chain should be greater than 10KΩ and less than 1MΩ. Table 1 lists appropriate resistors which limit the bias current required of the external feedback resistor chain and ensuring good noise immunity.

The output voltage can be adjusted between less than 0.8V and V_{IN}. The output voltage formula is:

$$V_{OUT} = 0.5 \times \left(\frac{R_{FB1}}{R_{FB2}} + 1 \right)$$

V_{OUT} = output voltage (V)
R_{FB1} = feedback resistor from VOUT to ADJ (Ω)
R_{FB2} = feedback resistor from ADJ to GND (Ω)

Resistors with 1% or better tolerance are recommended to ensure voltage accuracy.

Table 1 — Recommended ADJ Resistor Combinations

V_{OUT}(V)	R_{FB2}(kΩ)	R_{FB1}(kΩ)
1	200	200
1.1	200	240
1.2	200	280
1.3	200	320
1.5	178	357
1.6	200	442
1.7	178	432
1.8	178	464
1.875	178	487
2.5	200	806
2.8	178	820
3	178	887
3.3	100	560
3.6	100	620
3.8	100	665

Continuous Conduction & Oscillator Synchronization

The SC196 is designed to operate in continuous conduction, fixed-frequency mode. When the SYNC/PWM pin is tied high the part runs in PWM mode using the internal oscillator. The part can be synchronized to an external clock by driving a clock signal into the SYNC/PWM pin. The part synchronizes to the rising edge of the clock.

Protection Features

The SC196 provides the following protection features:

- Thermal Shutdown
- Current Limit
- Over-Voltage Protection
- Soft-Start

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC196 if the junction temperature exceeds 145°C. In thermal shutdown, the on-chip power devices are disabled, effectively tri-stating the LX output. Switching will resume when the temperature drops by 10°C. During this time,

Applications Information (Cont.)

if the output voltage decreases by more than 60% of its programmed value, a soft-start will be invoked.

Current Limit

The PMOS and NMOS power devices of the buck switcher stage are protected by current limit functions. In the case of a short to ground on the output, the part enters frequency foldback mode, which causes the switching frequency to divide by a factor determined by the output voltage. This prevents the inductor current from "stair-casing".

Over-Voltage Protection

Over-voltage protection is provided on the SC196. In the event of an over-voltage on the output, the PWM drive is disabled, effectively tri-stating the LX output. The part will not resume switching until the output voltage has fallen 2% below the regulation voltage.

Soft-Start

The soft-start mode is enabled after every shutdown cycle to limit in-rush current. In conjunction with the frequency foldback, this controls the maximum current during start-up. The PMOS current limit is stepped up through seven soft-start levels to the full value by a timer driven from the internal oscillator. During soft-start, the switching frequency is stepped through 1/8, 1/4, 1/2 and full internal oscillator frequency. The time at which these steps are made is controlled by the output voltage reaching predefined threshold levels. When the output voltage is within 2% of the regulation voltage, soft-start mode is disabled.

Power Save Mode Operation

The PSAVE mode may be selected by tying the SYNC/PWM pin to GND. Selecting PSAVE mode will enable the SC196 to automatically activate/deactivate operation at light loads, maximizing efficiency across the full load range. The SC196 automatically detects the load current at which it should enter PSAVE mode. The SC196 is optimized to track maximum efficiency with respect to V_{IN}.

In PSAVE mode, V_{OUT} is driven from a lower level to an upper level by a switching burst. Once the upper level has been reached, the switching is stopped and the quiescent current is reduced. V_{OUT} falls from the upper to lower levels in this low current state as the load current discharges the output capacitor. The burst-to-off period in PSAVE will decrease as the load current reduces.

The PSAVE switching burst frequency is controlled so that the inductor current ripple is similar to that in PWM mode. The minimum switching frequency during this period is limited to 650kHz.

The SC196 automatically detects when to exit PSAVE mode by monitoring V_{OUT}. For the SC196 to exit PSAVE mode, the load must be increased, causing V_{OUT} to decrease until the power save exit threshold is reached. PSAVE levels are set high to minimize the undershoot when exiting PSAVE. The lower PSAVE comparator level is set +0.7% above V_{OUT}, and the upper comparator level at +1.5% above V_{OUT}, with the exit threshold at -2% below V_{OUT}.

If PSAVE operation is required, then a 22µF output capacitor must be used.

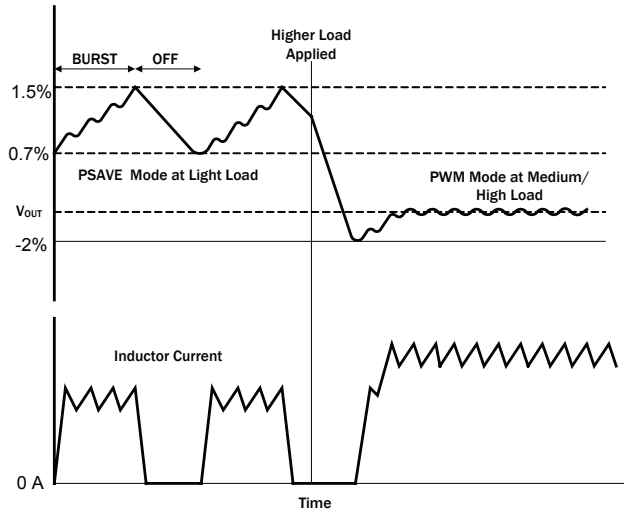


Figure 1 — Power Save Operation

100% Duty Cycle Operation

The 100% duty cycle mode may be selected by connecting the MODE pin high. This will allow the SC196 to maintain output regulation under conditions of low input voltage/ high output voltage conditions.

In 100% duty cycle operation, as the input supply drops toward the output voltage, the PMOS on-time increases linearly above the maximum value in fixed-frequency operation until the PMOS is active continuously. Once

Applications Information (Cont.)

the PMOS is switched on continuously, the output voltage tracks the input voltage minus the voltage drop across the PMOS power device and inductor according to the following relationship:

$$V_{OUT} = V_{IN} - I_{OUT} \times (R_{DSP} + R_{IND})$$

where
V_{OUT} = Output voltage
V_{IN} = Input voltage
I_{OUT} = Output current
R_{DSP} = PMOS switch ON resistance
R_{IND} = Series resistance of the inductor

Inductor Selection

The SC196 is designed for use with a 4.7µH inductor. Where V_{OUT} > 3.8V is required, a 10µH inductor is recommended. The magnitude of the inductor current ripple depends on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{osc}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

This equation demonstrates the relationship between input voltage, output voltage, and inductor ripple current.

The inductor should have a low DCR to minimize the conduction losses and maximize efficiency. As a minimum requirement, the DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Final inductor selection will depend on various design considerations such as efficiency, EMI, size and cost. Table 2 lists the manufacturers of practical inductor options.

C_{IN} Selection

The source input current to a buck converter is non-continuous. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 10µF should be used for input voltage filtering, while a 22µF capacitor is recommended for improved input voltage filtering.

Table 1 — Recommended Inductors

Manufacturer/Part #	Value (µH)	DCR (Ω)	Rated Current (A)	Tolerance (%)	Dimensions LxWxH (mm)
BI Technologies HM66404R1	4.1	0.057	1.95	20	5.7 × 5.7 ×2.0
Coilcraft D01608C-472ML	4.7	0.09	1.5	20	6.6 × 4.5 × 3.0
TDK VLCF4020T- 4R7N1R2	4.7	0.098	1.24	30	4.0 × 4.0 × 2.0
Taiyo Yuden LMNP04SB4R7N	4.7	0.050	1.2	30	5.0 × 5.0 × 2.0
TOKO D52LC	4.7	0.087	1.14	20	5.0 × 5.0 × 2.0
Sumida CDRH3D16	4.7	0.050	1.2	30	3.8 × 3.8 × 1.8
Coilcraft LPS3015	4.7	0.2	1.1	20	3.0 × 3.0 × 1.5

Note: recommended Inductors do not necessarily guarantee rated performance of the part.

C_{OUT} Selection

The internal compensation is designed to work with a certain output filter corner frequency defined by the equation:

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

This filter has a single pole and is designed to operate with a minimum output capacitor value of 10µF. Larger output capacitor values will improve transient performance. If PSAVE operation is required, the minimum capacitor value is 22µF.

Output voltage ripple is a combination of the voltage ripple from the inductor current charging and discharging the output capacitor and the voltage created from the inductor current ripple through the output capacitor ESR. Selecting an output capacitor with a low ESR will reduce the output voltage ripple component, as can be seen in the following equation:

$$\Delta V_{OUT(ESR)} = \Delta I_{L(RIPPLE)} \times ESR_{COUNT}$$

Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature

Applications Information (Cont.)

and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application. Attention should be paid to the DC voltage characteristics of the ceramic capacitors to be used for both input and output. Parts with different case sizes can vary significantly. For example a 22µF X5R 0805 capacitor with 3.6V DC applied could have a capacitance as low as 12µF. When a 1206 size part is used, the capacitance is approximately 20µF. Table 3 lists the manufacturers of recommended capacitor options.

Table 3 — Recommended Capacitors

Manufacturer/Part #	Value (µF)	Rated Voltage (VDC)	Temperature Characteristic	Case Size
Murata GRM21BR60J226ME39L	22	6.3	X5R	0805
Murata GRM422X5R226 K16H533	22	16	X5R	1210
Murata GRM188R60J106 MKE19	10	6.3	X5R	0603
TDK C2012X5R0J106K	10	6.3	X5R	0603

Note: Where PSAVE operation is required, 22µF must be used for C_{OUT}.

Feed-Forward Compensation Capacitor

A small 10pf compensation capacitor, C_{FB1} is required to ensure correct operation. This capacitor should be connected directly across feedback resistor R_{FB1}. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their superior temperature characteristics.

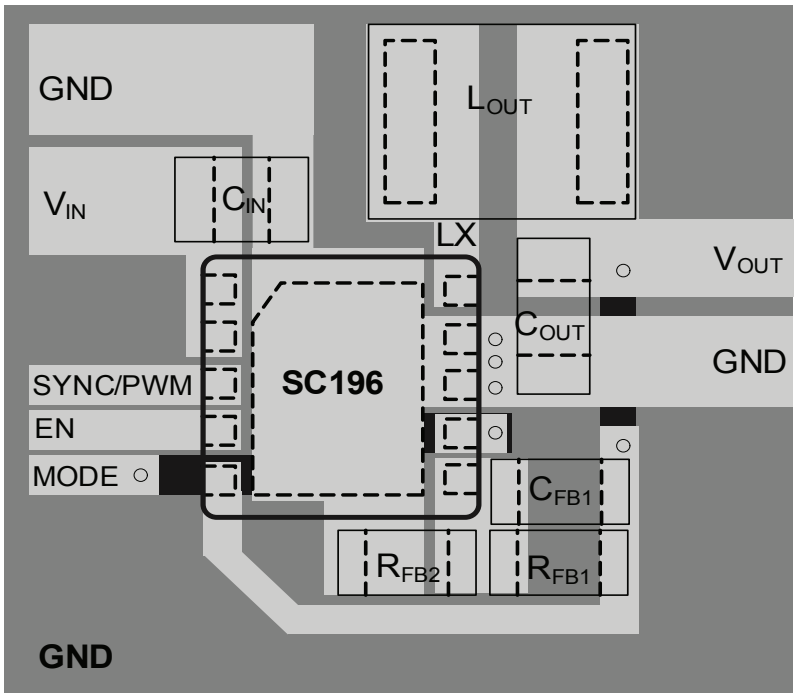
Applications Information (Cont.)

PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce and resistive voltage losses. Poor regulation and instability can result.

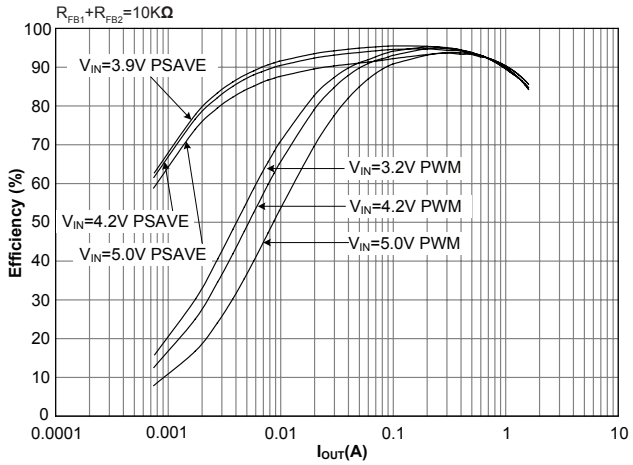
A few simple design rules can be implemented to ensure good layout:

1. Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
2. Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference. Keep R_{FB1} and R_{FB2} close to the ADJ pin to avoid noise pickup.
3. Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling of switching noise to the ground plane.
4. Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

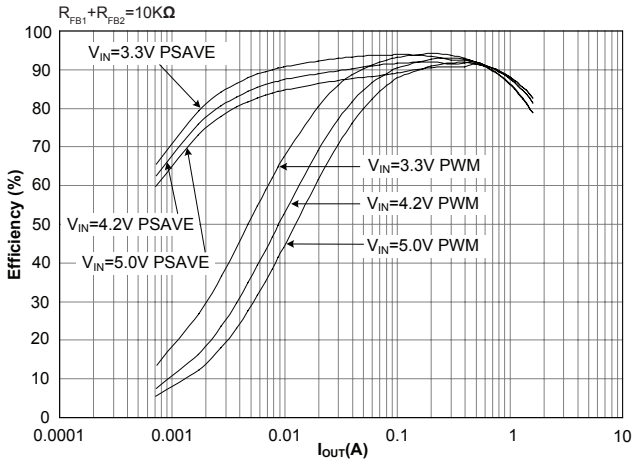


Typical Characteristics

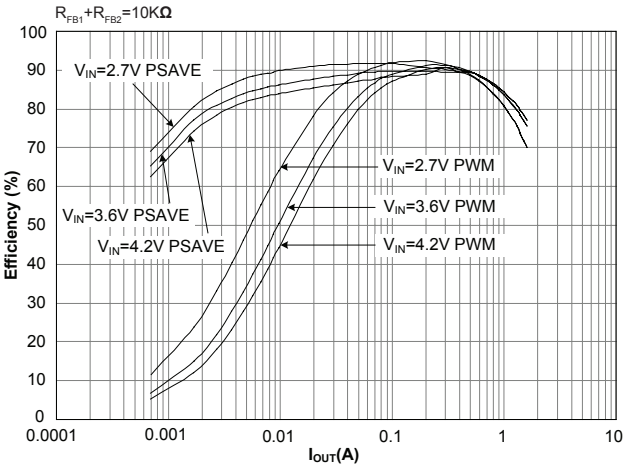
Efficiency vs. Load Current V_{OUT} = 3.3V



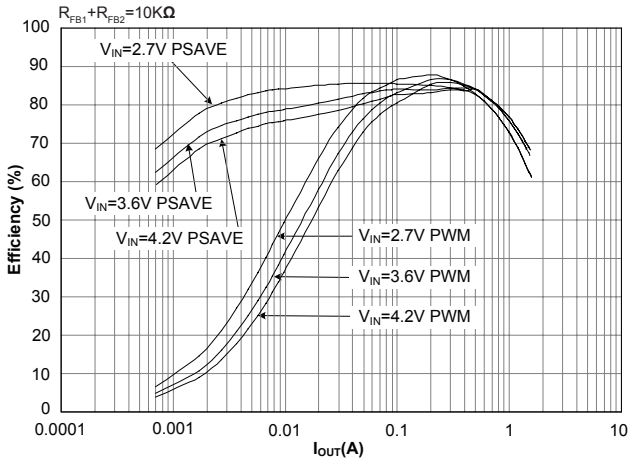
Efficiency vs. Load Current V_{OUT} = 2.5V



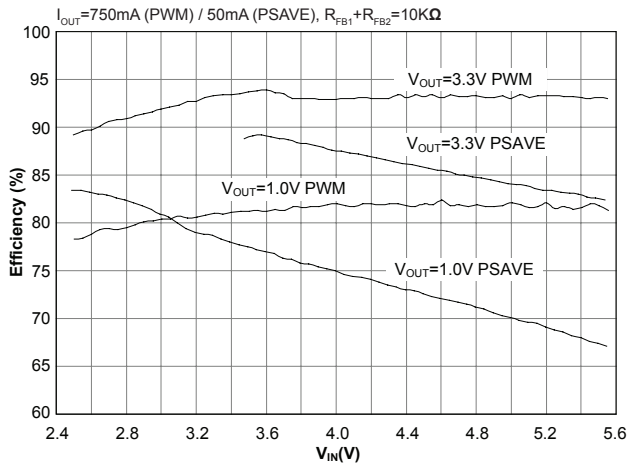
Efficiency vs. Load Current V_{OUT} = 1.8V



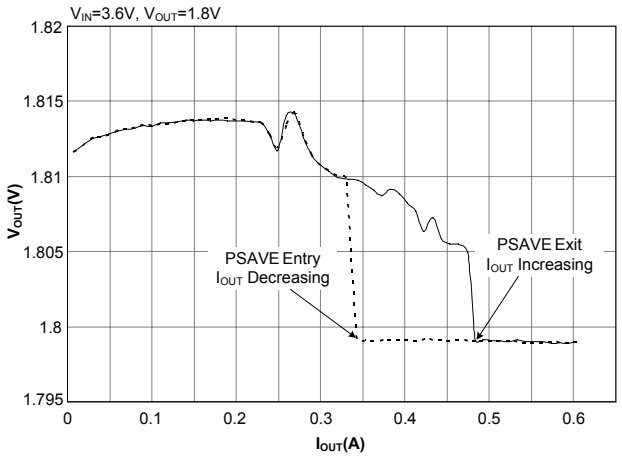
Efficiency vs. Load Current V_{OUT} = 1.0V



Efficiency vs. Input Voltage

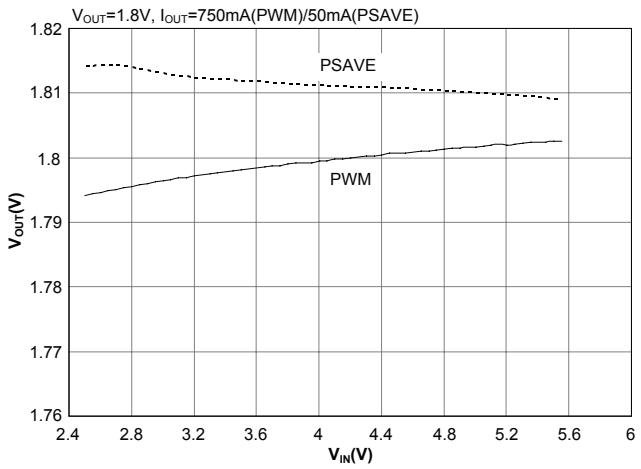


PWM to PSAVE Hysteresis

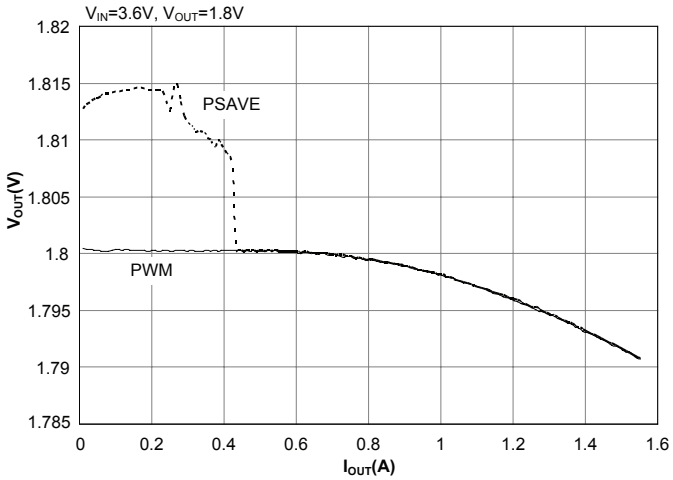


Typical Characteristics (Cont.)

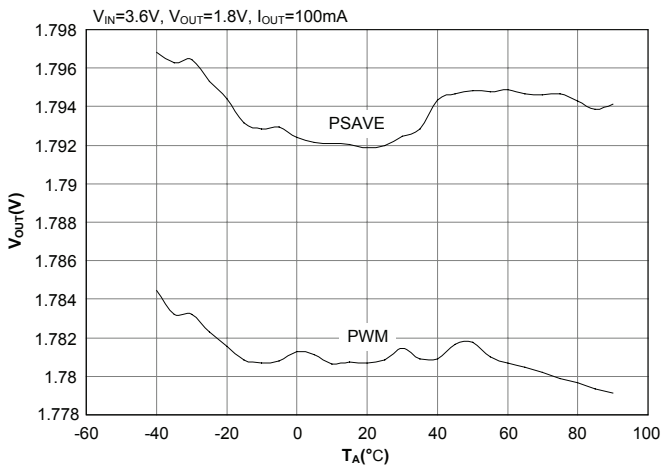
V_{OUT} vs. V_{IN}



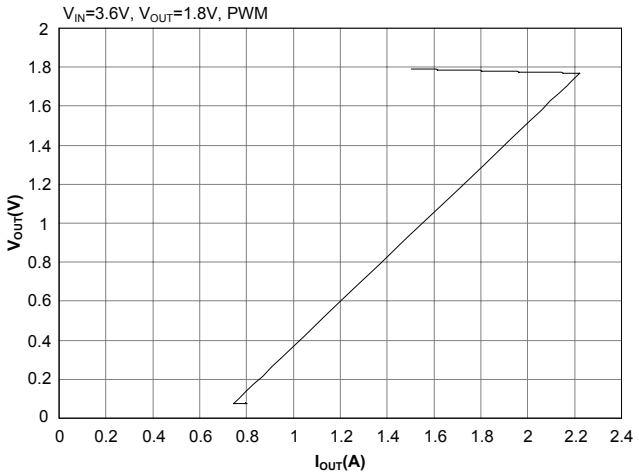
Load Regulation



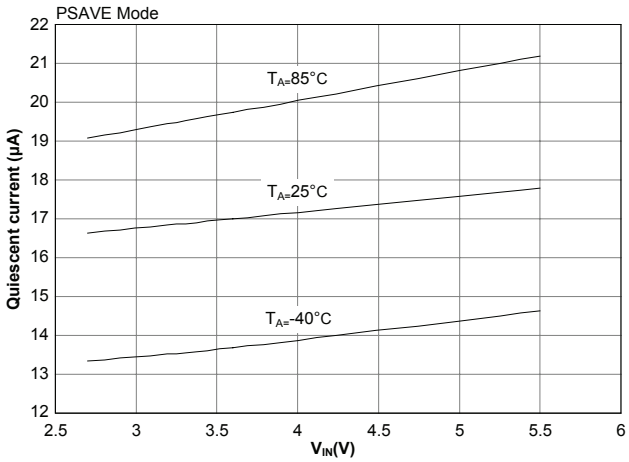
V_{OUT} vs. Temperature V_{OUT}=1.8V



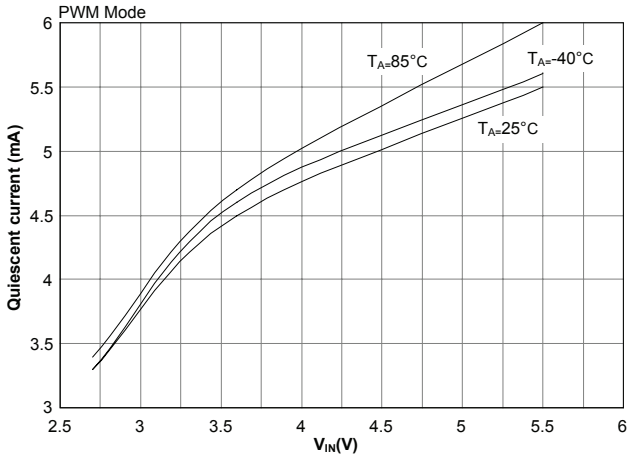
Current Limit



Quiescent Current vs. Input Voltage, PSAVE Mode

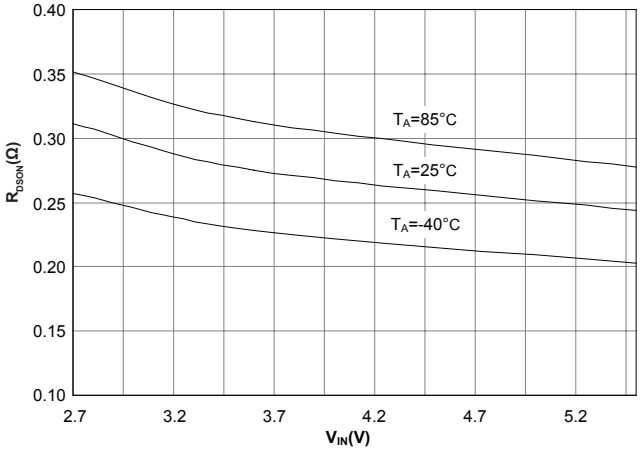


Quiescent Current vs. Input Voltage, PWM Mode

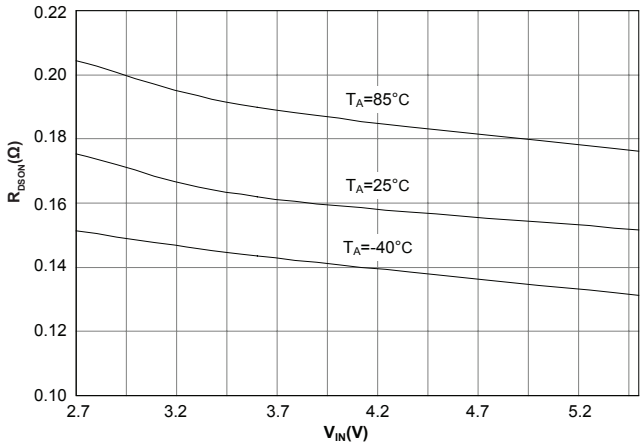


Typical Characteristics (Cont.)

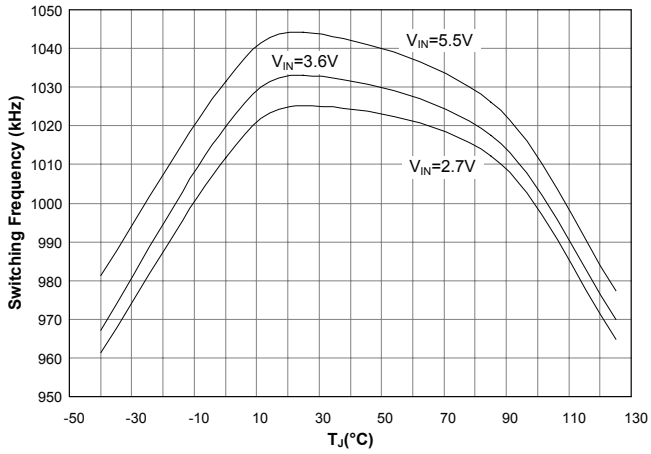
P-Channel R_{DSON} vs. Input Voltage



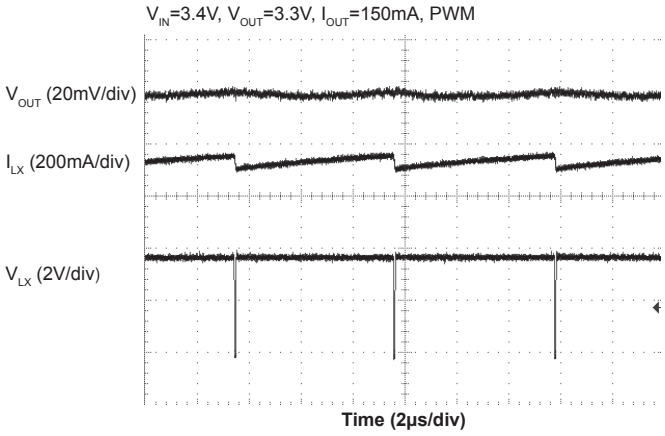
N-Channel R_{DSON} vs. Input Voltage



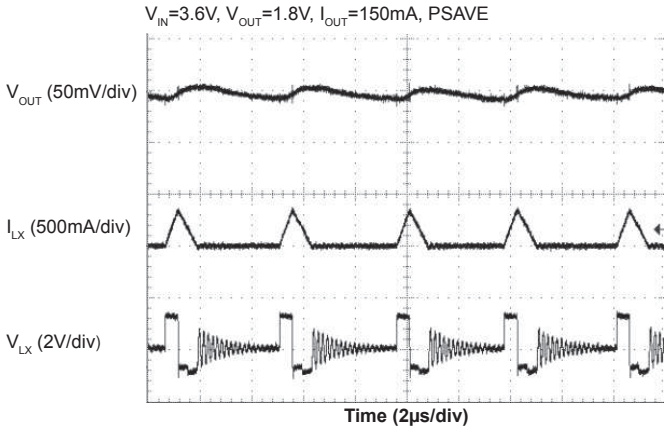
Switching Frequency vs. Temperature



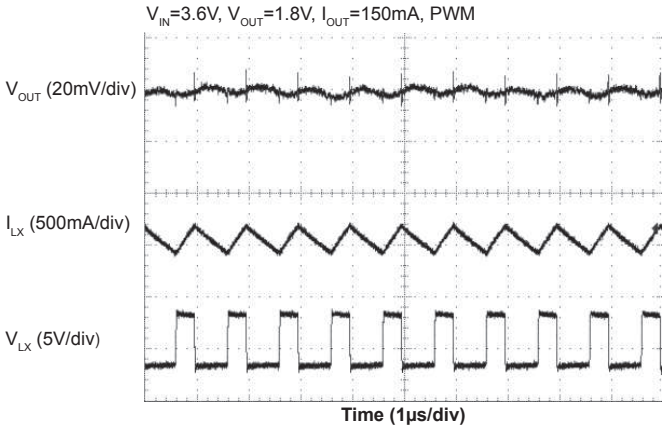
100% Duty Cycle Mode



PSAVE Operation

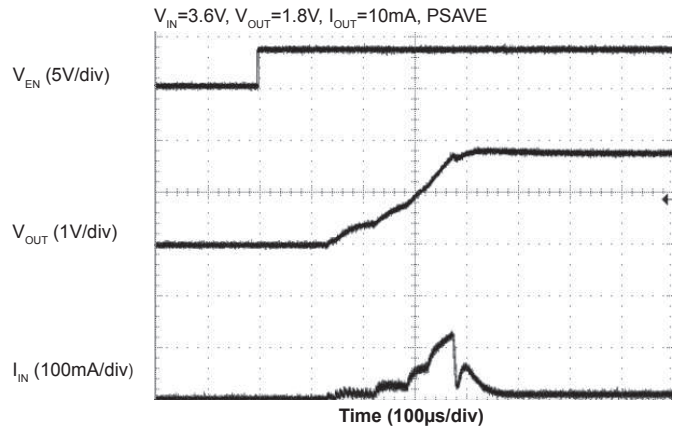


PWM Operation

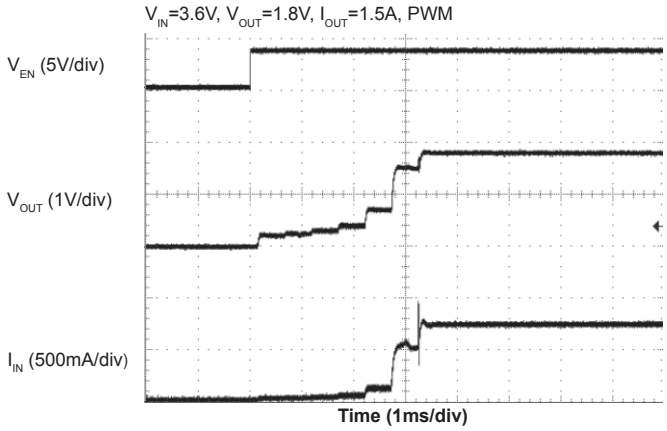


Typical Characteristics (Cont.)

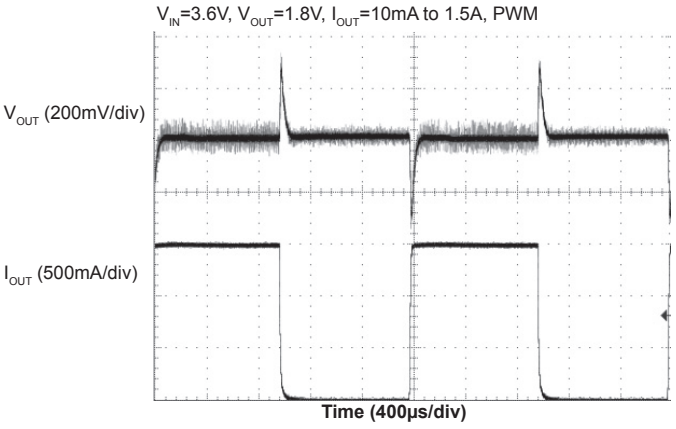
PSAVE Start-up



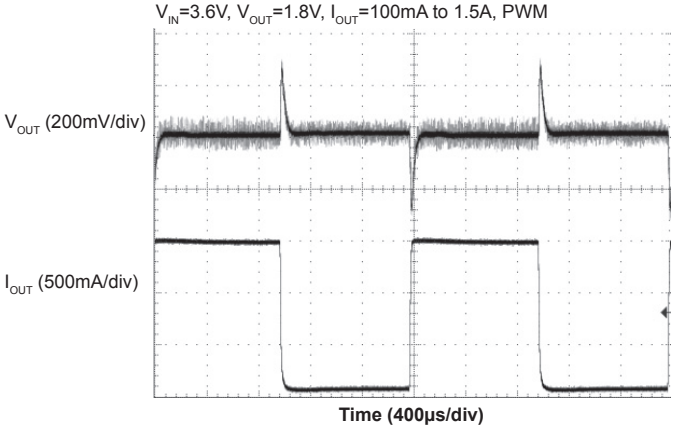
PWM Start-up



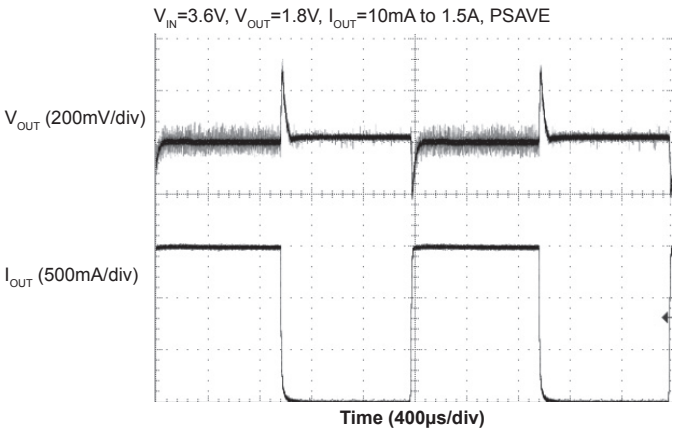
Load Transient Response-1



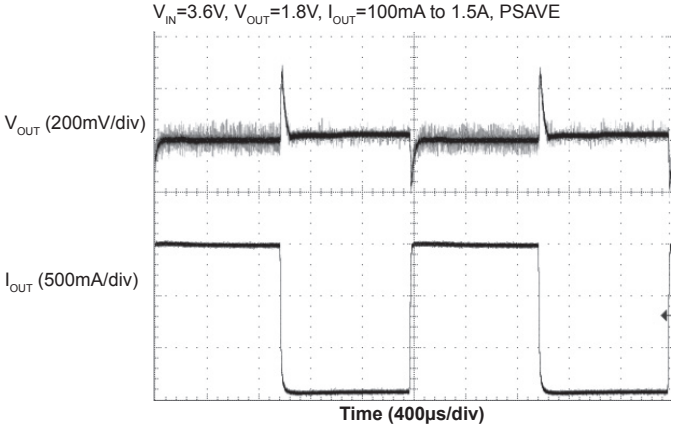
Load Transient Response-2



Load Transient Response-3

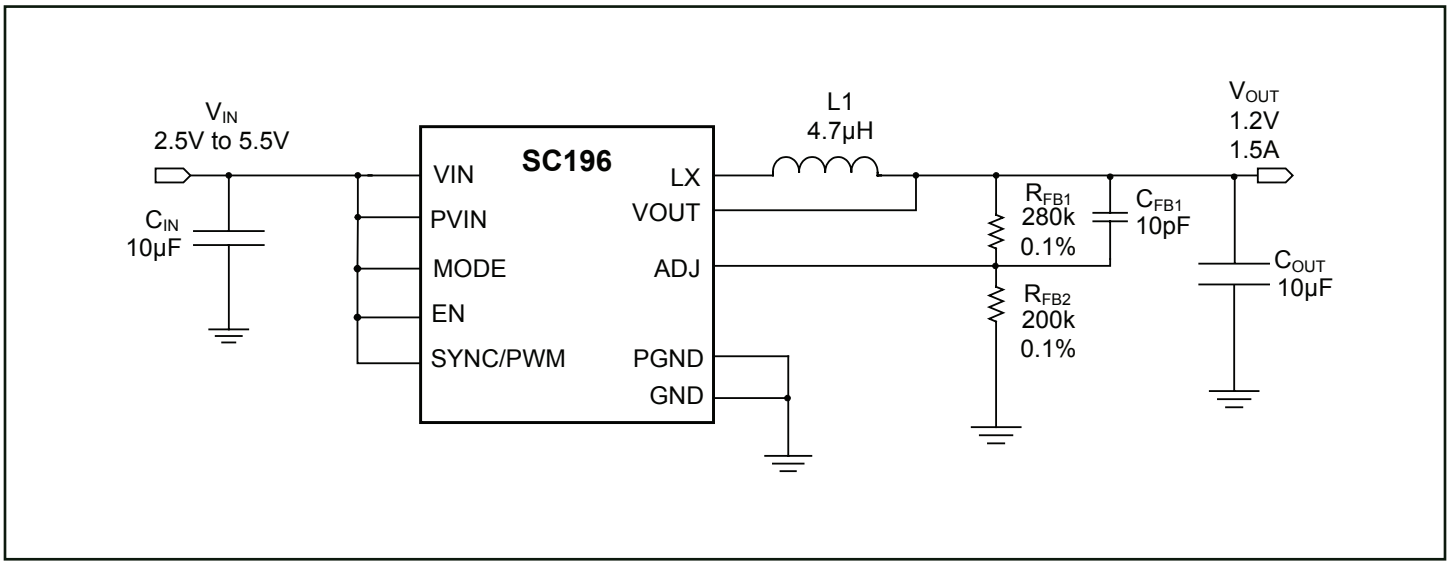


Load Transient Response-4



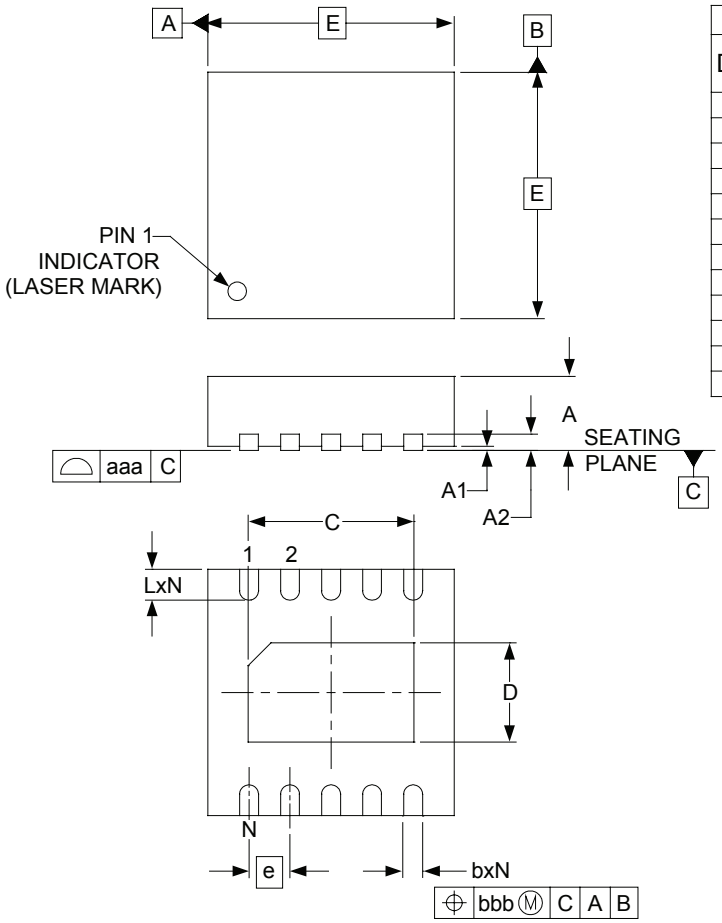
Applications Circuits

V_{OUT} Programmed to 1.2V, no PSAVE



The output voltage is set at 1.2V by the selection of the two resistors R_{FB1} and R_{FB2}, using resistor values from Table 1. PWM-only mode operation is selected by connecting the SYNC/PWM pin to the VIN pin. The 100% duty cycle capability is selected by connecting the MODE pin to the VIN pin. A 10µF capacitor is selected for the output, as PSAVE operation is not required in this application.

Outline Drawing — MLPD-UT10 3x3x0.6

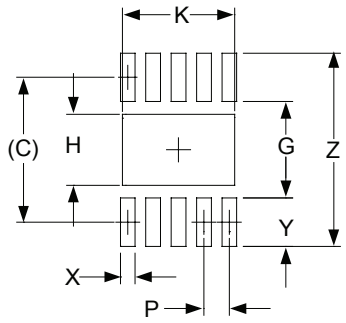


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.018	-	.024	0.45	-	.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.007	.009	.011	0.18	0.23	0.30
C	.074	.079	.083	1.87	2.02	2.12
D	.042	.048	.052	1.06	1.21	1.31
E	.114	.118	.122	2.90	3.00	3.10
e		.020 BSC			0.50 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		10			10	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-UT10 3x3x0.6



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.020	0.50
X	.012	0.30
Y	.037	0.95
Z	.150	3.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE

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