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SC2446
Dual-Phase Single or Two Output Synchronous Step-Down Controllers

Description

The SC2446 is a high-frequency dual synchronous step-down switching power supply controller. It provides out-of-phase high-current output gate drives to all N-channel MOSFET power stages. The SC2446 operates in synchronous continuous-conduction mode. Both phases are capable of maintaining regulation with sourcing or sinking load currents, making the SC2446 suitable for generating both V_{DDQ} and the tracking V_{TT} for DDR applications.

The SC2446 employs fixed frequency peak current-mode control for the ease of frequency compensation and fast transient response.

The dual-phase step-down controllers of the SC2446 can be configured to provide two individually controlled and regulated outputs or a single output with shared current in each phase. The Step-down controllers operate from an input of at least 4.7V and are capable of regulating outputs as low as 0.5V

The step-down controllers in the SC2446 have the provision to sense a synthesized MOSFET $R_{DS(ON)}$ for current-mode control. This sensing scheme (U.S. patent 6,441,597) eliminates the need of the current-sense resistor and is more noise-immune than direct sensing of the high-side or the low-side MOSFET voltage. Precise current-sensing with sense resistor is optional.

Individual soft-start and overload shutdown timer is included in each step-down controller. The SC2446 implements hiccup overload protection. In two-phase single-output configuration, the master timer controls the soft-start and overload shutdown functions of both controllers.

Features

- 2-Phase synchronous continuous conduction mode for high efficiency step-down converters
- Out of phase operation for low input current ripples
- Output source and sink currents
- Fixed frequency peak current-mode control
- 75mV/-110mV maximum current sense voltage
- Synthesized MOSFET $R_{DS(ON)}$ current-sensing for low-cost applications
- Optional resistor current-sensing for precise current-limit
- Dual outputs or 2-phase single output operation
- Excellent current sharing between individual phases
- Wide input voltage range: 4.7V to 16V
- Individual soft-start, overload shutdown and enable
- Duty cycle up to 88%
- 0.5V feedback voltage for low-voltage outputs
- External reference input for DDR applications
- Buffered $V_{DDQ}/2$ output
- Programmable frequency up to 1 MHz per phase
- External synchronization
- Industrial temperature range
- 28-lead TSSOP - EDP package

Applications

- Telecommunication power supplies
- DDR memory power supplies
- Graphic power supplies
- Servers and base stations

Typical Application Circuit

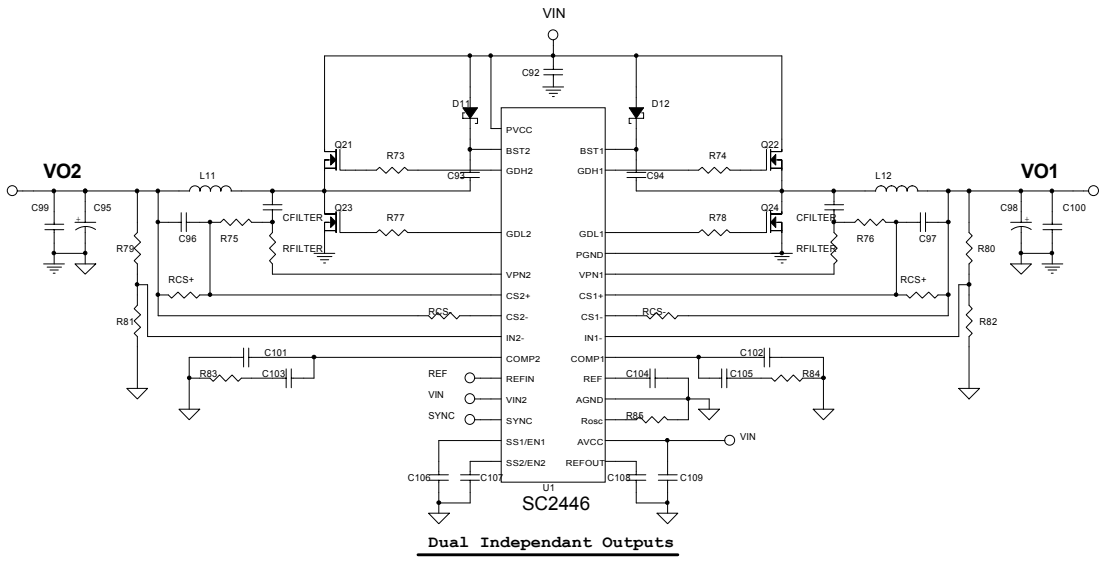


Figure 1

Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum Ratings	Units
Supply Voltage For Step-Down Controllers	AVCC, PVCC	-0.3 to 20	V
Input Voltage For the Second Converter	V_{IN2}	-0.3 to 20	V
High-Side Driver Supply Voltages	V_{BST1}, V_{BST2}	-0.3 to 32 (steady state)	V
		-0.3 to 40 (for <10ns @ freq. < 500kHz)	
VPN	V_{VPN}	-0.3 to 20 (steady state)	V
		-0.3 to 26 (for <10ns @ freq. < 500kHz)	
IN1-, IN2- Voltages	V_{IN1-}, V_{IN2-}	-0.3 to AVCC+0.3	V
REF, REF_{OUT} Voltages	V_{REF}, V_{REFOUT}	-0.3 to 6	V
REF_{IN} Voltage	V_{REFIN}	-0.3 to AVCC+0.3	V
COMP1, COMP2 Voltages	V_{COMP1}, V_{COMP2}	-0.3 to AVCC+0.3	V
CS1+, CS1-, CS2+ and CS2- Voltages	V_{CS1+}, V_{CS1-}, V_{CS2+}, V_{CS2-}	-0.3 to AVCC+0.3	V
SYNC Voltage	V_{SYNC}	-0.3 to AVCC+0.3	V
SS1/EN1 AND SS2/EN2 Voltages	V_{SS1}, V_{SS2}	-0.3 to 6	V
Peak Gate Drive Currents	I_{GDH1}, I_{GDH2}, I_{GDL1}, I_{GDL2}	3	A
Peak VPN1 and VPN2 Output Currents	I_{VPN1}, I_{VPN2}	100	mA
Ambient Temperature Range	T_A	-40 to 85	°C
Thermal Resistance Junction to Case (TSSOP-28)	θ_{JC}	13	°C/W
Thermal Resistance Junction to Ambient (TSSOP-28)	θ_{JA}	84	°C/W
Storage Temperature Range	T_{STG}	-60 to 150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	260	°C
Maximum Junction Temperature	T_J	150	°C

Electrical Characteristics

Unless specified: AVCC = PVCC = V_{IN2} =12V, V_{BST1} = V_{BST2} = 12V, SYNC= 0, R_{OSC} = 51.1kΩ, -40 °C < T_A = T_J < 85 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Undervoltage Lockout						
AVCC Start Threshold	$AVCC_{TH}$	AVCC Increasing		4.5	4.7	V
AVCC Start Hysteresis	$AVCC_{HYST}$			0.17		V
AVCC Operating Current	I_{CC}	AVCC= 12V		12	16	mA
AVCC Quiescent Current in UVLO		AVCC = $AVCC_{TH}$ - 0.2V		1.7		mA
Channel 1 Error Amplifier						
Non-inverting Input Voltage	V_{IN1+}		0.490	0.500	0.510	V
Non-inverting Input Line Regulation		$AVCC_{TH}$ < AVCC< 15V			0.02	%/V
Input Offset Voltage				1	±3	mV
Inverting Input Bias Current	I_{IN1-}			-100	-250	nA
Amplifier Transconductance	G_{M1}			260		$\mu\Omega^{-1}$
Amplifier Open-Loop Gain	a_{OL1}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
Minimum COMP1 Switching Threshold		V_{CS1+} = V_{CS1-} = 0 V_{SS1} Increasing		2.2		V

Electrical Characteristics (Cont.)

Unless specified: AVCC = PVCC = V_{IN2} =12V, V_{BST1} = V_{BST2} = 12V, SYNC= 0, R_{OSC} = 51.1kΩ, -40°C < T_A = T_J < 85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Amplifier Output Sink Current		V_{IN1-} = 1V, V_{COMP1} = 2.5V		16		µA
Amplifier Output Source Current		V_{IN1-} = 0, V_{COMP1} = 2.5V		12		µA
Channel 2 Error Amplifier						
Input Common-mode Voltage Range		(Note 1)	0		3	V
Inverting Input Voltage Range		(Note 1)	0		AVCC	V
Input Offset Voltage				1.5	±3	mV
Non-inverting Input Bias Current	I_{IN2+}			-150	-380	nA
Inverting Input Bias Current	I_{IN2-}			-100	-250	nA
Inverting Input Voltage for 2-Phase Single Output Operation			2.5			V
Amplifier Transconductance	G_{M2}			260		$\mu\Omega^{-1}$
Amplifier Open-Loop Gain	a_{OL2}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
Minimum COMP2 Switching Threshold		V_{CS2+} = V_{CS2-} = 0 V_{SS2} Increasing		2.2		V
Amplifier Output Sink Current		V_{COMP2} = 2.5V		16		µA
Amplifier Output Source Current		V_{COMP2} = 2.5V		12		µA
Oscillator						
Channel Frequency	f_{CH1}, f_{CH2}		450	500	550	KHz
Synchronizing Frequency		(Note 1)	2.1f_{CH}			KHz
SYNC Input High Voltage			1.5			V
SYNC Input Low Voltage					0.5	V
SYNC Input Current	I_{SYNC}	V_{SYNC} = 0.2V V_{SYNC} = 2V			1 100	µA
Channel Maximum Duty Cycle	D_{MAX1}, D_{MAX2}			88		%
Channel Minimum Duty Cycle	D_{MIN1}, D_{MIN2}				0	%
Current-limit Comparators						
Input Common-Mode Range			0		AVCC - 1	V
Cycle-by-cycle Peak Current Limit	V_{ILIM1+}, V_{ILIM2+}	V_{CS1-} = V_{CS2-} = 0.5V, Sourcing Mode	60	75	90	mV
Valley Current Overload Shutdown Threshold	V_{ILIM1-}, V_{ILIM2-}	V_{CS1-} = V_{CS2-} = 0.5V, Sinking Mode	-85	-110	-130	mV
Positive Current-Sense Input Bias Current	I_{CS1+}, I_{CS2+}	V_{CS1+} = V_{CS1-} = 0 V_{CS2-} = V_{CS2-} = 0		-0.7	-2	µA
Negative Current-Sense Input Bias Current	I_{CS1-}, I_{CS2-}	V_{CS1+} = V_{CS1-} = 0 V_{CS2+} = V_{CS2-} = 0		-0.7	-2	µA
Gate Drivers						
High-side Gate Drive Peak Source Current		V_{BST1} ,V_{BST2} = 12V		1.5		A
High-side Gate Drive Peak Sink Current		V_{BST1} ,V_{BST2} = 12V		1		A

Electrical Characteristics (Cont.)

Unless specified: AVCC = PVCC = V_{IN2} =12V, V_{BST1} = V_{BST2} = 12V, SYNC= 0, R_{OSC} = 51.1kΩ, -40°C < T_A = T_J < 85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-side Gate Drive Peak Source Current		AVCC = PVCC =12V		1.5		A
Low-side Gate Drive Peak Sink Current		AVCC = PVCC =12V		1		A
Gate Drive Rise Time		C_L = 2200pF		20		ns
Gate Drive Fall Time		C_L = 2200pF		20		ns
Low-side Gate Drive to High-side Gate Drive Non-overlapping Delay		C_L = 0		90		ns
High-side Gate Drive to Low-side Gate Drive Non-overlapping Delay		C_L = 0		90		ns
Minimum On-Time		TA = 25°C		150		ns
Soft-Start, Overload Latchoff and Enable						
Soft-Start Charging Current	I_{SS1}, I_{SS2}	V_{SS1} = V_{SS2} = 1.5V		2		µA
Overload Latchoff Enabling Soft-Start Voltage		V_{SS1} and V_{SS2} Increasing		3.2		V
Overload Latchoff IN1- Threshold		V_{SS1} = 3.8V, V_{IN1-}Decreasing		0.75V_{REF}		V
Overload Latchoff IN2- Threshold		V_{SS2} = 3.8V, V_{IN2-}Decreasing		0.72 X V_{REFIN}		V
Soft-Start Discharge Current	$I_{SS1(DIS)}$, $I_{SS2(DIS)}$	V_{IN1-} = 0.5V_{REF}, V_{IN2-} = 0.5V_{REFIN}, V_{SS1} = V_{SS2} = 3.8V		1.4		µA
Overload Latchoff Recovery Soft-Start Voltage	V_{SSRCV1}, V_{SSRCV2}	V_{SS1} and V_{SS2} Decreasing	0.3	0.5	0.7	V
Gate Drive Disable SS/EN Voltage			0.7	0.9		V
Gate Drive Enable SS/EN Voltage				1.2	1.5	V
Channel 1 Virtual Phase Node Voltage						
Output High Voltage	V_{VPN1H}	I_{VPN1}= -100µA, V_{BST1}= 24V	V_{PVCC}-0.05			V
Output Low Voltage	V_{VPN1L}	I_{VPN1}= 100µA, V_{BST1}= 24V			20	mV
Output Sourcing Current		V_{BST1}= 24V, V_{VPN1}= V_{PVCC} - 0.2V		7		mA
Output Sinking Current		V_{BST1}= 24V, V_{VPN1}= 0.2V		7		mA
Channel 2 Virtual Phase Node Voltage						
Output High Voltage	V_{VPN2H}	I_{VPN2}= -100µA, V_{BST2}= 24V	V_{IN2} - 0.05			V
Output Low Voltage	V_{VPN2L}	I_{VPN2}= 100µA, V_{BST2}= 24V			20	mV
Output Sourcing Current		V_{BST2}= 24V, V_{VPN2}= V_{IN2} - 0.2V		7		mA
Output Sinking Current		V_{BST2}= 24V, V_{VPN2}= 0.2V		7		mA
External Reference Buffer						
External Reference Input Voltage Range	V_{REFIN}		0		4	V
Buffered Output Voltage	V_{REFOUT}	V_{REFIN}=1.25V, I_{REFOUT}= -1mA	V_{REFIN}-0.01	V_{REFIN}	V_{REFIN}+0.01	V

Electrical Characteristics (Cont.)

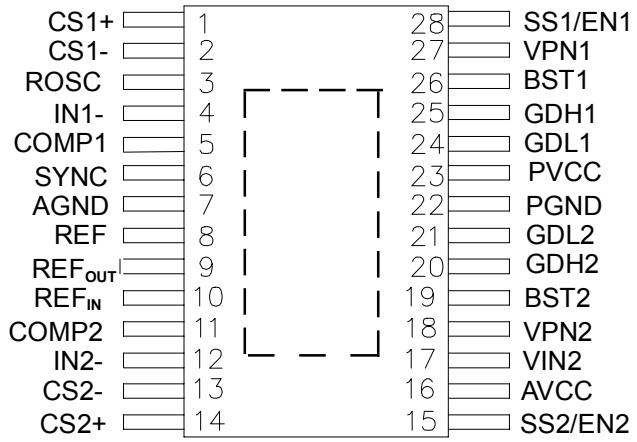
Unless specified: AVCC = PVCC = V_{IN2} =12V, V_{BST1} = V_{BST2} = 12V, SYNC= 0, R_{OSC} = 51.1kΩ, -40°C < T_A = T_J < 85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Load Regulation		0 < I_{REFOUT} < -5mA		0.02		%/mA
Internal 0.5V Reference Buffer						
Output Voltage	V_{REF}	I_{REF}= -1mA	490	500	510	mV
Load Regulation		0 < I_{REF} < -5mA		0.05		%/mA

Notes:
(1) Guaranteed by design not tested in production.
(2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configurations

(TOP VIEW)



(28-Pin TSSOP)

Figure 2

Ordering Information

Device	Package(1)	Temp. Range(T_A)
SC2446ITETRT(2)	TSSOP-28-EDP	-40 to 85°C
SC2446EVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices for TSSOP package.
(2) Lead free product.

Pin Descriptions

TSSOP Package

Pin	Pin Name	Pin Function
1	CS1+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 1.
2	CS1-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 1. Normally tied to the output of the converter.
3	ROSC	An external resistor connected from this pin to GND sets the oscillator frequency.
4	IN1-	Inverting Input of the Error Amplifier for the Step-down Controller 1. Tie an external resistive divider between OUTPUT1 and the ground for output voltage sensing.
5	COMP1	The Error Amplifier Output for Step-down Controller 1. This pin is used for loop compensation.
6	SYNC	Edge-triggered Synchronization Input. When not synchronized, tie this pin to a voltage above 1.5V or the ground. An external clock (frequency > frequency set with ROSC) at this pin synchronizes the controllers.
7	AGND	Analog Signal Ground.
8	REF	Buffered Output of the Internal 0.5V Reference. The non-inverting input of the error amplifier for the step-down converter 1 is internally connected to this pin .
9	REF_{OUT}	Buffered output of the external voltage applied to Pin 10.
10	REF_{IN}	An external Reference voltage is applied to this pin.The non-inverting input of the error amplifier for the step-down converter 2 is internally connected to this pin.
11	COMP2	The Error Amplifier Output for Step-down Controller 2. This pin is used for loop compensation.
12	IN2-	Inverting Input of the Error Amplifier for the Step-down Controller 2. Tie an external resistive divider between output2 and the ground for output voltage sensing. Tie to AVCC for two-phase single output applications
13	CS2-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 2. Normally tied to the output of the converter.
14	CS2+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 2
15	SS2/EN2	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for step-down converter 2. Pulling this pin below 0.7V shuts off the gate drivers for the second controller. Leave open for two-phase single output applications.
16	AVCC	Power Supply Voltage for the Analog Portion of the Controllers.
17	VIN2	This pin is tied to the voltage supplying the drain of the high side power MOSFET of converter 2. This pin is used only in "Combi" current sense.
18	VPN2	The Second Step-down Converter Virtual Phase Node (Unloaded). Used for "Combi" current sense only. This pin is left open when sensing current with a sense resistor at the converter output.
19	BST2	Bootstrapped Supply for the High-side Gate Drive 2. Connect to a bootstrap capacitor and an external diode as described in application information.
20	GDH2	Gate Drive Output for the High-side N-channel MOSFET of Output 2. Gate drive voltage swings from ground to VBST2.

Pin Descriptions

Pin	Pin Name	Pin Function
21	GDL2	Gate Drive Output for the Low-side N-channel MOSFET of Output 2. Gate drive voltage swings from ground to PVCC.
22	PGND	Ground Supply for All the Gate drivers.
23	PVCC	Power Supply Voltage for Low-side MOSFET Drivers.
24	GDL1	Gate Drive Output for the Low-side N-channel MOSFET of Output 1. Gate drive voltage swings from ground to PVCC.
25	GDH1	Gate Drive Output for the High-side N-channel MOSFET of Output 1. Gate drive voltage swings from ground to VBST1.
26	BST1	Bootstrapped Supply for the High-side Gate Drive 1. Connect to a bootstrap capacitor and an external diode as described in application information.
27	VPN1	The First Step-down Converter Virtual Phase Node (Unloaded). Used for "Combi" current sense only. This pin is left open when sensing current with a sense resistor at the converter output.
28	SS1/EN1	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for buck converter 1. Pulling this pin below 0.7V shuts off the gate drivers for the first controller.

Block Diagram

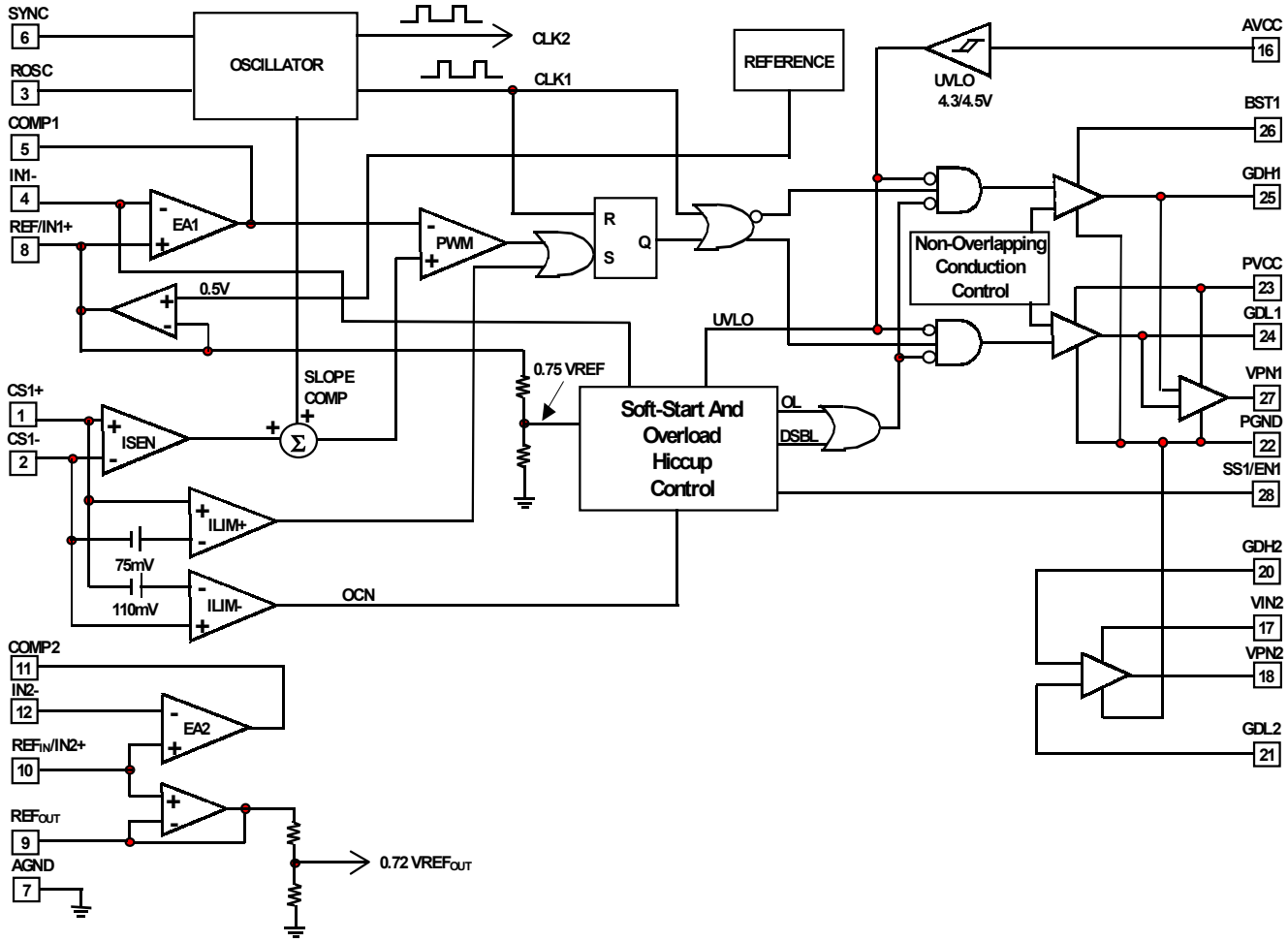


Figure 3. SC2446 Block Diagram (Channel 1 PWM Control Only)

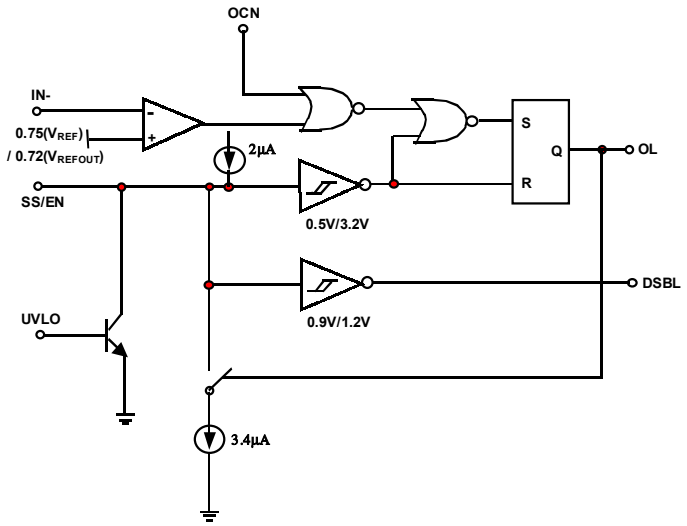


Figure 4. Soft-Start and Overload Hiccup Control Circuit

Operation

Overview

The SC2446 is a constant frequency 2–phase current-mode step-down PWM switching controller driving all N-channel MOSFET's. The two channels of the controller operate at 180 degrees out of phase from each other. Since input currents are interleaved in a two-phase converter, input ripple current is lower and smaller input capacitor can be used for filtering. Also, with lower inductor current and smaller inductor ripple current per phase, overall I^2R losses are reduced.

The SC2446 operates in synchronous continuous-conduction mode. It can be configured either as two independent step-down controllers producing two separate outputs or as a dual-phase single-output controller by tying the IN2- pin to V_{CC}. In single output operation, the channel one error amplifier controls both channels and the channel two error amplifier is disabled. Soft-start and overload hiccup of both channels is synchronized to channel one.

Frequency Setting and Synchronization

The internal oscillator of the SC2446 runs at twice the phase frequency. The free-running frequency of the oscillator can be programmed with an external resistor from the ROSC pin to the ground. The step-down controllers are capable of operating up to 1 MHz. It is necessary to consider the operating duty-ratio before deciding the switching frequency. See Applications Information section for more details.

When synchronized externally, the applied clock frequency should be twice the desired phase frequency. The synchronizing clock frequency should also be between 1-1.33 times the set free-running frequency.

Control Loop

The SC2446 uses peak current-mode control for fast transient response, ease of compensation and current sharing in single output operation. The low-side MOSFET of each channel is turned off at the falling-edge of the phase timing clock. After a brief non-overlapping time interval of 90ns, the high-side MOSFET is turned on. The phase inductor current ramps up. When the sensed inductor current reaches the threshold determined by the error amplifier output and ramp compensation, the high-side MOSFET is turned off. After a non-overlapping conduction time of 90ns, the low-side MOSFET is turned on.

The supply voltages for the high-side gate drivers are obtained from two diode-capacitor bootstrap circuits. If the bootstrap capacitor is charged from V_{CC}, the high-side gate drive voltage swing will be from approximately $2V_{CC}$ to the ground. The power dissipated in the high-side gate driver is not higher with higher voltage swing because the gate-source voltage of the high-side MOSFET still swing from zero to V_{CC}.The outputs of the low-side gate drivers swing from V_C to the ground.

The SC2446 has internal ramp-compensation to prevent sub-harmonic oscillation when operating above 50% duty cycle. There is enough ramp internally for a sensed voltage ripple between ¼ to 1/3 of the full-scale sensed voltage limit of 75mV. The maximum sensed voltage limit is unaffected by the compensation ramp.

Current-Sensing

There are two ways to sense the inductor current for current-mode control with the SC2446. Since the peak inductor current corresponds to 75mV of sensed voltage (CS+ - CS-), resistor current sensing can be used at the output without resulting in excessive power dissipation. Although accurate and far easier to lay out than high-side resistor sensing, a pair of precision sense resistors adds cost to the converter. The SC2446 has provision to reconstruct a differential voltage proportional to the inductor current at the output of the converter (U.S. patent 6,441,597). The voltage to current ratio or the equivalent sense resistance R_{eq} is a combination of high-side and low-side MOSFET $R_{DS(ON)}$'s and the inductor series resistance (hence the name "Combi-Sense"). The SC2446 provides the virtual phase voltages VPN1 and VPN2 (these are

Operation (Cont.)

unloaded versions of their respective power phase voltages) for current sensing. This method does not require any precision sense resistor. It is cheaper to implement but is less accurate than resistor current sensing. Since the sensed voltage is developed at the output of the step-down converter, it is less prone to switching transient spikes. This method will be described in more details in the Applications Information section.

Error Amplifiers

In closed loop operation, the error amplifier output ranges from 1.1V to 3.5V. The upper output operating range of either error amplifier is reserved for positive current-sense voltage (CS+ - CS-) and corresponds to positive (sourcing) output current. If the amplifier swings to its lower operating range, the amplifier will still modulate the high-side gate drive duty-ratio. However the peak current-sense voltage (hence the peak inductor current) will be limited to a negative value. The error amplifier output is about 2.2V when the peak sense-voltage is zero. The built-in offset in the current sense amplifier together with synchronous continuous-conduction mode of operation allows the SC2446 to regulate the output irrespective of the direction of the load current.

The non-inverting input of the first feedback amplifier is tied to the internal 0.5V voltage reference. Both the non-inverting and the inverting inputs of the second error amplifier are brought out as device pins so that the output of the second converter can be made to track the output of the first channel. For example in DDR applications, Channel 1 can be used to generate V_{DDQ} (2.5V) from the input (5V or 12V) and channel 2 is used to produce a tracking V_{TT} (1.25V) with V_{DDQ} being its input.

Current-Limit

The maximum current sense voltage of +75mV is the cycle-by-cycle peak current limit when the load is drawing current from the converter. There is no cycle-by-cycle current limiting when the inductor current flows in the negative direction. However once the valley of the current sense voltage exceeds –110mV, the corresponding channel will undergo shutdown and restart (hiccup).

Soft-Start and Overload Protection

The undervoltage lockout circuit discharges the SS/EN capacitors. After V_{CC} rises above 4.5V, the SS/EN capacitors are slowly charged by internal 2µA current source. With internal PNP transistors, the SS/EN voltages clamp the error amplifier outputs. When the error amplifier output rises to 2.2V, the high-side MOSFET starts to switch. As the SS/EN capacitor continues to be charged, the COMP voltage follows. The converter gradually delivers increasing power to the output. The inductor current follows the COMP voltage envelope until the output goes into regulation. The SS/EN clamp on COMP is then released.

After the SS/EN capacitor is charged above 3.2V (high enough for the error amplifier to provide full load current), the overload detection circuit is activated. If the output voltage falls below 70% of its set value or the valley current-sense voltage exceeds –110mV, an overload latch will be set and both the top and the bottom MOSFETs will be turned off. The SS/EN capacitor is slowly discharged with an internal 1.4µA current sink. The overload latch is reset when the SS/EN capacitor is discharged below 0.5V. The SS/EN capacitor is then recharged with the 2µA current source and the converter undergoes soft-start. If overload persists, the SC2446 will undergo repetitive shutdown and restart (Figure 3).

If the output is short-circuited, the inductor current will not increase indefinitely between the time the inductor current reaching its current limit and the instant the converter shuts down. This is due to cycle skipping reduces the actual operating frequency.

The SS/EN pin can also be used as the enable input for that channel. Both the high-side and the low-side MOSFETs will be turned off if the SS/EN pin is pulled below 0.7V.

Application Information

SC2446 consists of two current-mode synchronous buck controllers with many integrated functions. By proper application circuitry configuration, SC2446 can be used to generate
1) two independent outputs from a common input or two different inputs or
2) dual phase output with current sharing,
3) current sourcing/sinking from common or separate inputs as in DDR (I and II) memory application.
The application information related to the converter design using SC2446 is described in the following.

Step-down Converter

Starting from the following step-down converter specifications,

Input voltage range: $V_{in} \in [V_{in,min}, V_{in,max}]$
Input voltage ripple (peak-to-peak): ΔV_{in}
Output voltage: V_o
Output voltage accuracy: ε
Output voltage ripple (peak-to-peak): ΔV_o
Nominal output (load) current: I_o
Maximum output current limit: $I_{o,max}$
Output (load) current transient slew rate: dI_o (A/s)
Circuit efficiency: η
Selection criteria and design procedures for the following are described.
1) output inductor (L) type and value,
2) output capacitor (C_o) type and value,
3) input capacitor (C_{in}) type and value,
4) power MOSFET's,
5) current sensing and limiting circuit,
6) voltage sensing circuit,
7) loop compensation network.

Operating Frequency (f_s)

The switching frequency in the SC2446 is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.
1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time and
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET's/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

Minimum Switch On Time Consideration

In the SC2446 the falling edge of the clock turns on the top MOSFET. The inductor current and the sensed voltage ramp up. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2446 has a minimum on time of about 150ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 150ns.
For a synchronous step-down converter, the operating duty cycle is V_O/V_{IN}. So the required on time for the top MOSFET is $V_O/(V_{IN}fs)$. If the frequency is set such that the required pulse width is less than 150ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio V_O/V_{IN} and hence the required duty cycle is higher, the switching frequency can be increased to reduce the sizes of passive components.
There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2446. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

Application Information (Cont.)

Setting the Switching Frequency

The switching frequency is set with an external resistor connected from Pin 3 to the ground. The set frequency is inversely proportional to the resistor value (Figure 5).

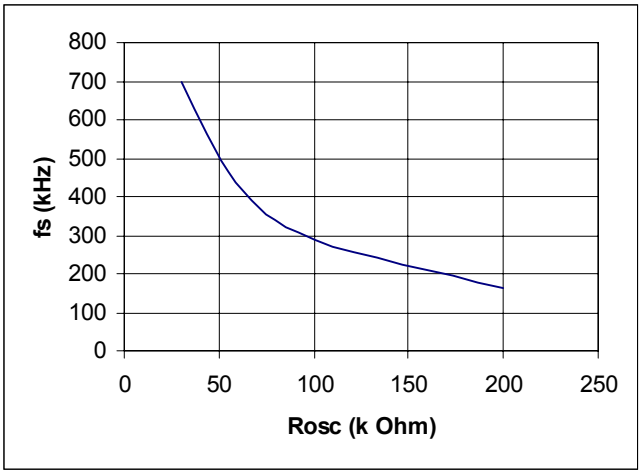


Figure 5. Free running frequency vs. R_{osc}.

Inductor (L) and Ripple Current

Both step-down controllers in the SC2446 operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.
Assuming that the inductor current ripple (peak-to-peak) value is $\delta * I_o$, the inductance value will then be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}.$$

The peak current in the inductor becomes (1+δ/2)*Io and the RMS current is

$$I_{L,rms} = I_o\sqrt{1+\frac{\delta^2}{12}}.$$

The followings are to be considered when choosing inductors.
a) Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.
b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.
c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR (R_{esr}) and ESL (L_{esl}) (Figure 6).

Figure 6. An equivalent circuit of C_o.

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t).$$

This basic equation illustrates the effect of ESR, ESL and C_o on the output voltage.

The first term is the DC voltage across C_o at time *t=0*. The second term is the voltage variation caused by the charge balance between the load and the converter output. The

Application Information (Cont.)

third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is

$$\Delta v_C \approx \frac{\delta I_o}{8 C_o f_s},$$

the ripple-voltage due to ESL is

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D},$$

and the ESR ripple-voltage is

$$\Delta v_{ESR} = R_{esr} \delta I_o.$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR. When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage $< \Delta V_o$, the ESR should satisfy

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}.$$

To limit the dynamic output voltage overshoot/undershoot within α (say 3%) of the steady state output voltage) from no load to full load, the ESR value should satisfy

$$R_{esr2} < \frac{\alpha V_o}{I_o}.$$

Then, the required ESR value of the output capacitors should be

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}.$$

The voltage rating of aluminum capacitors should be at least $1.5V_o$. The RMS current ripple rating should also be greater than

$$\frac{\delta I_o}{2\sqrt{3}}.$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{esr}}.$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant. For example, if a 10µF, 4mΩ ceramic capacitor is connected in parallel with 2x1500µF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100µF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100µF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formulae.

$$C_{eq}(\omega) := \frac{(R_{1a}+R_{1b})^2 \omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}{}^2 C_{1a} + R_{1b}{}^2 C_{1b})\omega^2 C_{1a} C_{1b} + (C_{1a}+C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (R_{1b}C_{1b}{}^2 + R_{1a}C_{1a}{}^2)}{(R_{1a}+R_{1b})^2 \omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors respectively. (Figure 7)

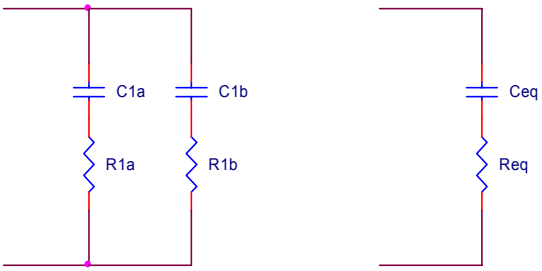


Figure 7. Equivalent RC branch.

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b} = R_1$ and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1.$$

Input Capacitor (C_{in})

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 8.

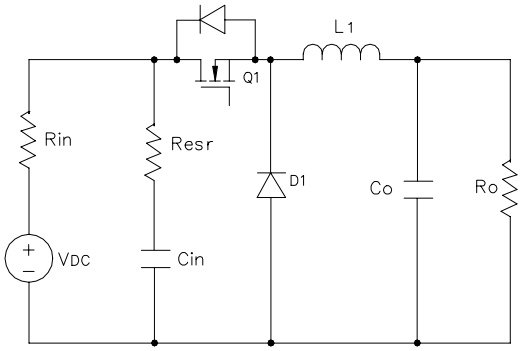


Figure 8. A simple model for the converter input

In Figure 8 the DC input voltage source has an internal impedance R_{in} and the input capacitor C_{in} has an ESR of R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 9.

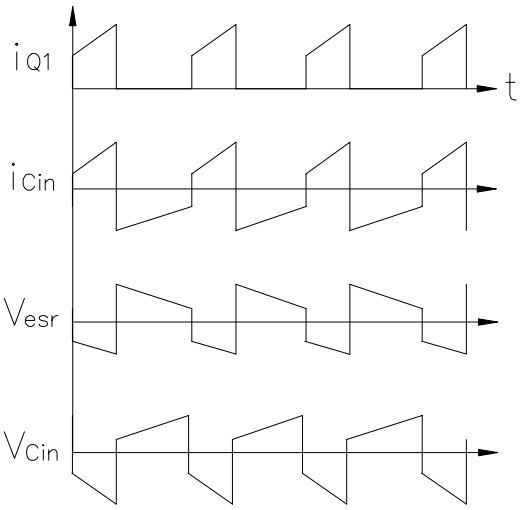


Figure 9. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFET's on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o \sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + \frac{D}{\eta^2}(1-D)]}.$$

The power dissipated in the input capacitors is then

$$P_{Cin} = I_{Cin}{}^2 R_{esr}.$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Application Information (Cont.)

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_o.$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_C \approx \frac{DI_o}{C_{in}f_s},$$

From these two expressions, C_{IN} can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2446 operate at 180 degrees from each other. If both step-down channels in the SC2446 are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, smaller inductors and capacitors can be used for each channel. The total output ripple-voltage remains unchanged. Smaller inductors speeds up output load transient.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the *RMS* value of the ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be D_1, D_2 and I_{o1}, I_{o2}, respectively.

If $D_1<0.5$ and $D_2<0.5$, then

$$I_{Cin} \approx \sqrt{D_1 I_{o1}^2 + D_2 I_{o2}^2}.$$

If $D_1>0.5$ and $(D_1-0.5) < D_2<0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + (D_1-0.5)(I_{o1}+I_{o2})^2 + (D_2-D_1+0.5) I_{o2}^2}.$$

If $D_1>0.5$ and $D_2 < (D_1-0.5) < 0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + D_2(I_{o1}+I_{o2})^2 + (D_1-D_2-0.5) I_{o2}^2}.$$

If $D_1>0.5$ and $D_2 > 0.5$, then

$$I_{Cin} \approx \sqrt{(D_1+D_2-1)(I_{o1}+I_{o2})^2 + (1-D_2) I_{o1}^2 + (1-D_1) I_{o2}^2}.$$

Choosing Power MOSFET's

Main considerations in selecting the MOSFET's are power dissipation, cost and packaging. Switching losses and conduction losses of the MOSFET's are directly related to the total gate charge (C_g) and channel on-resistance ($R_{ds(on)}$). In order to judge the performance of MOSFET's, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 10.

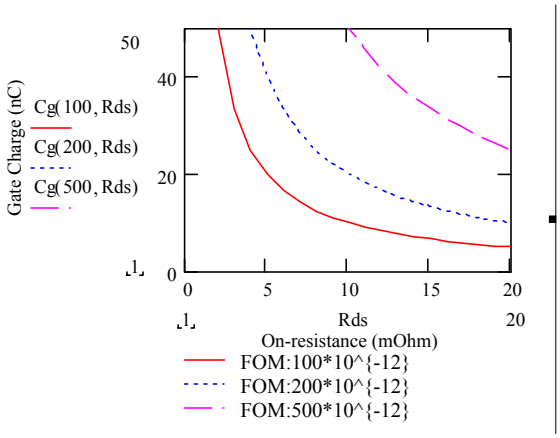


Figure 10. Figure of Merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFET's with both low C_g and low $R_{ds(on)}$. Usually a trade-off between $R_{ds(on)}$ and C_g has to be made.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET's with low C_g are used for the top switch and

Application Information (Cont.)

MOSFET's with low $R_{ds(on)}$ are used for the bottom switch.

MOSFET power dissipation consists of
a) conduction loss due to the channel resistance $R_{ds(on)}$,
b) switching loss due to the switch rise time t_r and fall time t_f, and
c) the gate loss due to the gate resistance R_G.

Top Switch:

The *RMS* value of the top switch current is calculated as

$$I_{Q1,rms} = I_o\sqrt{D(1+\tfrac{\delta^2}{12})}.$$

The conduction losses are then

$$P_{tc} = I_{Q1,rms}{}^2 R_{ds(on)}.$$

$R_{ds(on)}$ varies with temperature and gate-source voltage. Curves showing $R_{ds(on)}$ variations can be found in manufacturers' data sheet. From the Si4860 datasheet, $R_{ds(on)}$ is less than 8mΩ when V_{gs} is greater than 10V. However $R_{ds(on)}$ increases by 50% as the junction temperature increases from 25°C to 110°C.

The switching losses can be estimated using the simple formula

$$P_{ts} = \tfrac{1}{2}(t_r + t_f)(1+\tfrac{\delta}{2})I_o V_{in} f_s.$$

where t_r is the rise time and t_f is the fall time of the switching process. Different manufactures have different definitions and test conditions for t_r and t_f. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 11.

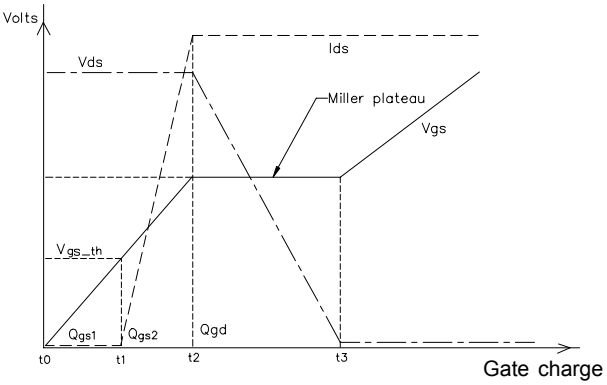


Figure 11. MOSFET switching characteristics

In Figure 11,
Q_{gs1} is the gate charge needed to bring the gate-to-source voltage V_{gs} to the threshold voltage V_{gs_th},
Q_{gs2} is the additional gate charge required for the switch current to reach its full-scale value I_{ds} and
Q_{gd} is the charge needed to charge gate-to-drain (Miller) capacitance when V_{ds} is falling.
Switching losses occur during the time interval [t_1, t_3]. Defining $t_r = t_3 - t_1$ and t_r can be approximated as

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}.$$

where R_{gt} is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance R_{gi}, external resistance R_{ge} and the gate resistance R_g within the MOSFET i.e.

$$R_{gt} = R_{gi} + R_{ge} + R_g.$$

V_{gsp} is the Miller plateau voltage shown in Figure 11. Similarly an approximate expression for t_f is

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}.$$

Only a portion of the total losses $P_g = Q_g V_{cc} f_s$ is dissipated in the MOSFET package. Here Q_g is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total power loss of the top switch is then

$$P_t = P_{tc} + P_{ts} + P_{tg}.$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction losses are inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Bottom Switch:

The *RMS* current in bottom switch can be shown to be

$$I_{Q2,rms} = I_o\sqrt{(1-D)(1+\tfrac{\delta^2}{12})}.$$

Application Information (Cont.)

The conduction losses are then

$$P_{bc}=I_{Q2,rms}{}^2 R_{ds(on)}.$$

where $R_{ds(on)}$ is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g. V_{in}=12V, V_o=1.5V), the duty ratio D will be small. Since the bottom switch conducts with duty ratio (1-D), the corresponding conduction losses can be quite high.

Due to non-overlapping conduction between the top and the bottom MOSFET's, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss

$$P_{bs} = \tfrac{1}{2}(t_r + t_f)(1+\tfrac{\delta}{2})I_o V_d f_s$$

is negligible due to near zero-voltage switching.

The gate losses are estimated as

$$P_{bg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total bottom switch losses are then

$$P_b=P_{bc}+P_{bs}+P_{bg}.$$

Once the power losses P_{loss} for the top (P_t) and bottom (P_b) MOSFET's are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ($T_{j,max}$, usually 125°C) is not exceeded under the worst-case condition. The equivalent thermal impedance from junction to ambient (θ_{ja}) should satisfy

$$\theta_{ja} \le \frac{T_{j,max} - T_{a,max}}{P_{loss}}.$$

θ_{ja} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area and the air flow condition (free or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

Integrated Power MOSFET Drivers

In SC2446 there are four internally integrated gate drivers to drive all the MOSFETs in dual channels. With the device bipolar process, emitter-follower based Darlington bipolar transistors are used for the output stage. The key advantage of the Darlington configuration is that the total current gain is greatly improved which leads to larger driving current I_{gs}. This in turn will help reduce the MOSFETs switching losses. In order to estimate the losses associated with the gate driver, we first measured the gate driver waveform (typical waveforms of V_{ce} and I_{gs}) as shown in Figure12.

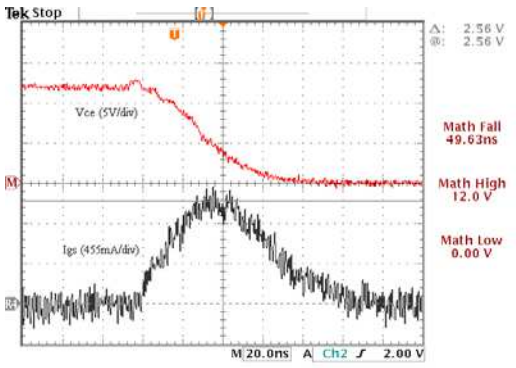


Figure 12. Measured gate driver output waveforms with 2.2Ω current limit resistor.

It is clear that the saturation voltage is not a constant. It changes with the driving current in a nonlinear fashion. A simple formula to calculate the losses with a reasonable accuracy is not available. But, we use a curve fitting technique to estimate the power losses in gate driver. First, the saturation voltage $v_{ce}(t)$ is approximated as

$$v_{ce}(t) = V_{cc}\, 2^{-\frac{1}{\sqrt{2}}(\frac{t}{T_1})^2}.$$

Where, V_{cc} is the gate driver collector voltage, T_1 is a time constant related to the fall time of v_{ce}. For the example in Fig. 12, V_{cc}=12V, T_1=0.5T_f with T_f being measured as ~50 ns. With these parameters, the approximated $v_{ce}(t)$ is plotted as in Figure 13 a).

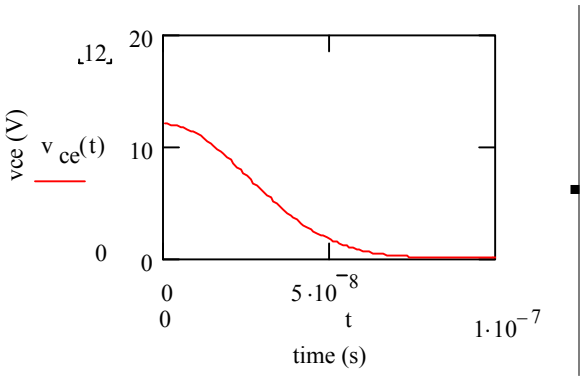


Figure 13 a). Approximated gate driver $v_{ce}(t)$ waveform.

Similarly, the gate drive current is approximated as

$$i_{gs}(t) = I_{gsp}\left(\frac{t}{T_2}\right)^2 e^{-\left(\frac{t}{T_2}\right)^2}.$$

Where, I_{gsp} is a scaling parameter proportional to the gate drive peak current, T_2 is a time constant proportional to the fall time of v_{ce}. For the example in Figure 13, I_{gsp}=3.15A, T_2=0.77T_f with T_f being measured as ~50 ns.

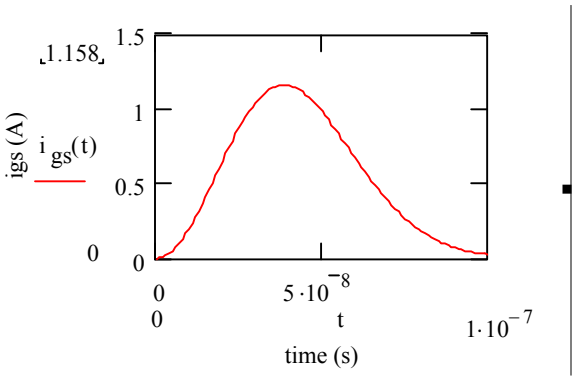


Figure 13 b). Approximated gate drive current $i_{gs}(t)$ waveform.

With these parameters, the approximated $i_{gs}(t)$ is plotted as in Figure 13 b).
Based on the approximation formulae of $v_{ce}(t)$ and $i_{gs}(t)$, one can calculate the power losses for each gate driver pair as

$$P_{gd} = \frac{1}{T_s}\int_0^{T_s} v_{ce}(t) i_{gs}(t) dt.$$

For SC2446, there are 4 gate drivers, the total gate driver losses is then $4P_{gd}$. For the example in Figure 12, the power losses for each gate driver is estimated as 122 mW when the operating frequency is about 300kHz. The total losses for the 4 gate drivers is then about 488 mW.

Remark 3: It is beneficial to select low gate charge MOSFET's for lower switching losses in the MOSFET package and lower power dissipation in the gate-driving IC. Once the MOSFET is chosen with a specified input gate charge, one can adjust the gate driving resistor to balance the driver IC losses and the power MOSFET switching losses. To the first order of approximation, smaller gate resistance leads to higher gate driving current and faster MOSFET switching. But, the driver incurs more power losses. On the other hand, larger gate drive resistance limits the gate drive current, which leads to low V_{ce} and less power losses. But, the MOSFET suffers more switching losses.
Using low gate charge MOSFET's reduces switching loss. To prevent shoot-through between the top and the bottom MOSFET's during commutation, one MOSFET should be completely turned off before the other is turned on. In the SC2446 the top and the bottom gate drive pulses are made non-overlapping. When not driving any load, the non-overlapping commutation intervals from the top to the bottom and from the bottom to the top gate drives are set at 90ns. If MOSFET's are driven from the SC2446, the non-overlapping commutation times will decrease due to finite gate-source voltage rise and fall times. The gate-source voltage waveforms of the MOSFET's should not overlap above their respective thresholds when driven from the SC2446. Use of low gate charge MOSFET's reduces transition times and the tendency of shoot-through. The combined rise and fall times during both commutations should be less than the preset non-overlapping intervals.

Current Sensing (Combi-Sense)
Inductor current sensing is required for the current-mode control. Although the inductor current can be sensed with a precision resistor in series with the inductor, a novel lossless Combi-sense technique is used in the SC2446. This SEMTECH proprietary technique has the advantages of

Application Information (Cont.)

1) lossless current sensing,
2) higher signal-to-noise ratio, and
3) preventing thermal run-away.

The basic arrangement of the Combi-sense is shown in Figure 14.

Where, R_L is the equivalent series resistance of the output inductor. The added R_s and C_s form a RC branch for inductor current sensing. This branch is driven from a small totem pole driver (Q3 and Q4) integrated within SC2446. The base driving signals Vbe3 and Vbe4

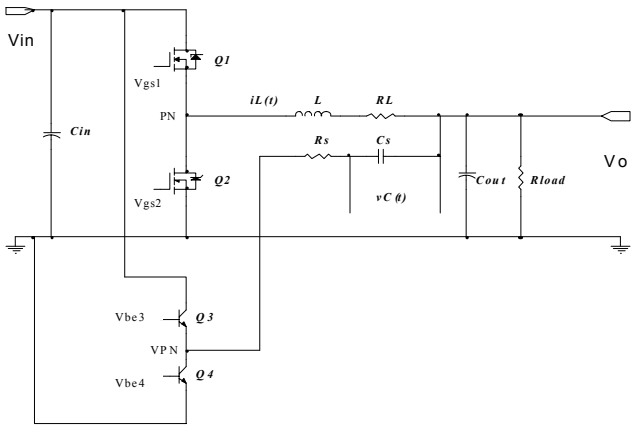


Figure 14. The basic structure of Combi-Sense.

are designed to follow the gate drive signals Vgs1 and Vgs2, respectively, with minimal delay drive. Ideally, the leading and falling edges of the Virtual Phase Node (VPN) follow that of the Phase Node (PN) when Q1~Q4 switch accordingly.

Specifically, when Q1/Q3 are ON and Q2/Q4 are OFF, the equivalent circuit of Figure 14 reduces to Figure 15 a). Where, Rds1 is the on-resistance of the top MOSFET. The two branches, consisting of {(Rds1+RL), L} and {R_s, C_s}, are in parallel. The DC voltage drop (Rds1+RL)I_o equals V_{Cs}. In this way, the output current is sensed from V_{Cs} when (Rds1+RL) is known.

When Q1/Q3 are OFF and Q2/Q4 are ON, the equivalent circuit of Figure 14 becomes the sub-circuit as shown in Figure 15 b). Where, Rds2 is the channel resistance of the bottom MOSFET. In this case, the branch {R_s,C_s} is in parallel with {(Rds2+RL), L} and V_{Cs}=(Rds2+RL)I_o. In average,

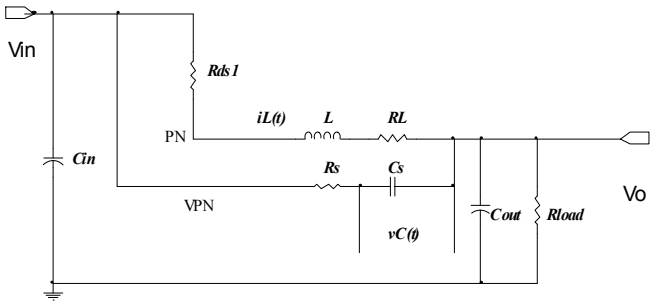


Figure 15 a). Equivalent sub-circuit.

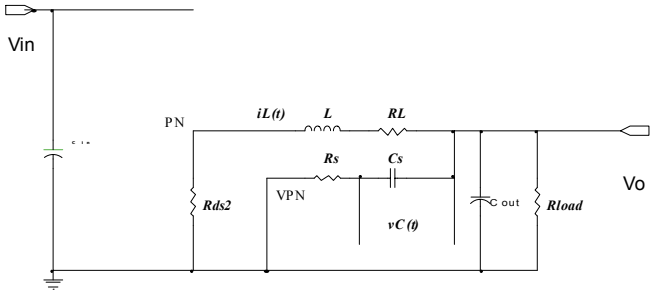


Figure 15 b). Equivalent sub-circuit.

$$V_{Cs}=[D(Rds1+RL)+(1-D)(Rds2+RL)]I_o,$$

or equivalently

$$V_{Cs}=[D\ Rds1+(1-D)Rds2+RL]I_o=R_{eq}I_o.$$

It is noted that the DC value of V_{Cs} is independent of the value of L, R_s and C_s. This means that, if only the average load current information is needed (such as in average current mode control), this current sensing method is effective without time constant matching requirement. In the current mode control as implemented in SC2446, the voltage ripple on C_s is critical for PWM operation. In fact, the AC voltage ripple peak-to-peak value of V_{Cs} (denoted as ΔV_{Cs}) directly effects the signal-to-noise ratio of the PWM operation. In general, smaller ΔV_{Cs} leads to lower signal-to-noise ratio and more noise sensitive operation. Larger ΔV_{Cs} leads to more circuit (power stage)

parameter sensitive operation. A good engineering compromise is to make

$$\Delta V_{Cs} \sim R_{eq} \delta I_o.$$

The prerequisite for such relation is the so called time constant matching condition

$$\frac{L}{R_{eq}} \approx R_s C_s.$$

When Rds1=Rds2, the above relations become equations.
For an example of application circuit, L=1.3µH, RL=1.56mΩ and Rds1=Rds2=8mΩ , the time constant R_sC_s should be set as 136µs. If one selects C_s=33 nF, then R_s=4.12 kΩ.

Scaling the Current Limit

Over-current is handled differently in the SC2446 depending on the direction of the inductor current. If the differential sense voltage between CS+ and CS- exceeds +75mV, the top MOSFET will be turned off and the bottom MOSFET will be turned on to limit the inductor current. This +75mV is the cycle-by-cycle peak current limit when the load is drawing current from the converter. There is no cycle-by-cycle current limit when the inductor current flows in the reverse direction. If the voltage between CS1+ and CS- falls below -113mV, the controller will undergo overload shutdown and time-out with both the top and the bottom MOSFETs shut off. (See the section Overload Protection and Hiccup).

In the circuit of Figure 14, the equivalent inductor current limits are set according to

$$I_{LMcp} = \frac{75mV}{R_{eq}},$$

when the load is sourcing current from the converter and

$$I_{LMcn} = -\frac{110mV}{R_{eq}},$$

when the load is forcing current back to the input power source. If R_{eq} = 9.56mW, then I_{LM} = 7.8/-11.8A. The circuit in Figure 16 allows the user to scale the equivalent current limit with the same R_{eq}.

In the following design steps, the capacitor C_S in the current sensing part is commonly selected in the range of 22nF ~ 68nF.

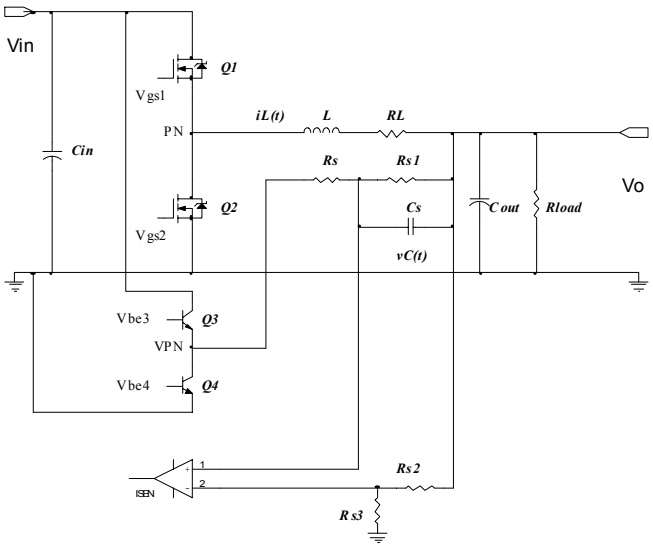


Figure 16. Scaling the equivalent current limit.

a) When the required current limit value I_{LM} is greater than I_{LMcp}, one just needs to remove R_{s3}, and solve the following equations

$$(R_s // R_{s1})\, C_s = \frac{L}{R_{eq}},$$

$$I_{LM} R_{eq} \frac{R_{s1}}{R_s + R_{s1}} = 75mV,$$

and $$R_{s2} = R_s // R_{s1}.$$

for $$R_s, R_{s1} \text{ and } R_{s2}.$$

Note that R_{S2} is selected as $R_s//R_{S1}$ in order to reduce the bias current effect of the current amplifier in SC2446. If the current limit is to be set to I_{LM} = 15A with the existing power circuit parameter and C_s = 33nF, it is calculated that R_{s2} = 4.12 kΩ, R_s = 7.87 kΩ and R_{s1} = 8.66 kΩ.
b) When the required current limit I_{LM} is less than I_{LMcp}, one just needs to remove R_{s1} and solve

Application Information (Cont.)

$$R_sC_s = \frac{L}{R_{eq}},$$

$$I_{LM}R_{eq} + \frac{R_s}{R_{s3}}V_O = 75mV,$$

for R_s and R_{S3}.

R_{s2} is then obtained from

$$R_{s2} = \frac{R_{s3}R_s}{R_{s3} - R_s}.$$

If the current limit is to be set to I_{LM} = 5A with the existing power circuit parameter and C_s, it is calculated that R_s=4.12 kΩ, R_{s3}=190 kΩ and R_{s2}=4.22 kΩ.
Similar steps and equations apply to the current limit setting and scaling for current sinking mode.

Remark 4: When the current limit I_{LM} is lower than I_{LMcp}, the designer has the freedom of selecting higher Rds(ON) MOSFETs to reduce cost. As a result, R_{eg} is increased and I_{LMcp} is reduced. Although the use of low-cost MOSFET's is always preferred, the current-limit setting technique described above allows quick adjustment on a well-tested prototype without the need to replace the power MOSFETs.

Overload Protection and Hiccup

During start-up, the capacitor from the SS/EN pin to ground functions as a soft-start capacitor. After the converter starts and enters regulation, the same capacitor operates as an overload shutoff timing capacitor. As the load current increases, the cycle-by-cycle current-limit comparator will first limit the inductor current. Further increase in loading will cause the output voltage (hence the feedback voltage) to fall. If the feedback voltage falls to less than (75% for Ch1, 72% for Ch2) of the reference voltage, the controller will shut off both the top and the bottom MOSFET's. Meanwhile an internal 1.4µA current source discharges the soft-start capacitor C_{32}(C_{33}) connected to the SS/EN pin.

When the capacitor is discharged to 0.5V, a 2µA current source recharges the SS/EN capacitor and converter restarts. If overload persists, the controller will shut down the converter when the soft start capacitor voltage exceeds 3.2V. The converter will repeatedly start and shut off until it is no longer overloaded. This hiccup mode of overload protection is a form of foldback current limiting. The following calculations estimate the average inductor current when the converter output is shorted to the ground.

a) The time taken to discharge the capacitor from 3.2V to 0.5V

$$t_{ssf} = C_{32}\frac{(3.2-0.5)V}{1.4\mu A}.$$

If C_{32} = 0.1µF, t_{ssf} is calculated as 193ms.
b) The soft start time from 0.5V to 3.2V

$$t_{ssr} = C_{32}\frac{(3.2-0.5)V}{2\mu A}.$$

When C_{32} = 0.1µF, t_{ssr} is calculated as 135ms. Note that during soft start, the converter only starts switching when the voltage at SS/EN exceeds 1.2V.
c) The effective start-up time is

$$t_{sso} = C_{32}\frac{(3.2-1.2)V}{2\mu A}.$$

The average inductor current is then

$$I_{Leff} = I_{LMcp}\frac{t_{sso}}{t_{ssf} + t_{ssr}}.$$

$I_{Leff} \approx 0.30\ I_{LMcp}$ and is independent of the soft start capacitor value. The converter will not overheat in hiccup.

Setting the Output Voltage

The non-inverting input of the channel-one error amplifier is internally tied the 0.5V voltage reference output (Pin 8). The non-inverting input of the channel-two error amplifier is brought out as a device pin (Pin 10) to which the user can connect Pin 8 or an external voltage reference. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. The voltage feedback gain h=0.5/V_o is related to the divider resistors value as

$$R_{o2} = \frac{h}{1-h}R_{o1.}$$

Application Information (Cont.)

Once either R_{o1} or R_{o2} is chosen, the other can be calculated for the desired output voltage V_o. Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

Vo (V)	**0.6**	0.9	**1.2**	**1.5**	1.8	2.5	3.3
(1-h)/h	**0.2**	0.8	**1.4**	**2**	2.6	4	5.6
Ro1 (Ohm)	**200**	806	**1.4K**	**2K**	2.61K	4.02K	5.62K
Ro2 (Ohm)	**1K**	1K	**1K**	**1K**	1K	1K	1K

Only the voltages in boldface can be precisely set with standard 1% resistors.

From this table, one may also observe that when the value

$$\frac{1-h}{h} = \frac{V_o - 0.5}{0.5}$$

and its multiples fall into the standard resistor value chart (1%, 5% or so), it is possible to use standard value resistors to exactly set up the required output voltage value.

The input bias current of the error amplifier also causes an error in setting the output voltage. The maximum inverting input bias currents of error amplifiers 1 and 2 is -250nA. Since the non-inverting input is biased to 0.5V, the percentage error in the second output voltage will be $-100\% \cdot (0.25\mu A) \cdot R_{o1}R_{o2}/[0.5 \cdot (R_{o1}+R_{o2})]$. To keep this error below 0.2%, $R_{o2} < 4k\Omega$.

Loop Compensation

SC2446 uses current-mode control for both step-down channels. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC networks is split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the sensed-current. In the SC2446 the compensation ramp is made duty-ratio dependent. The compensation ramp is approximately

$$I_{ramp} = De^{1.76D} * 30\mu A.$$

The slope of the compensation ramp is then

$$S_e = (1+1.76D)e^{1.76D}f_s * 30\mu A.$$

The slope of the internal compensation ramp is well above the minimal slope requirement for current loop stability and is sufficient for all the applications.

With the inner current loop stable, the output voltage is then regulated with the outer voltage feedback loop. A simplified equivalent circuit model of the synchronous Buck converter with current mode control is shown in Figure 17.

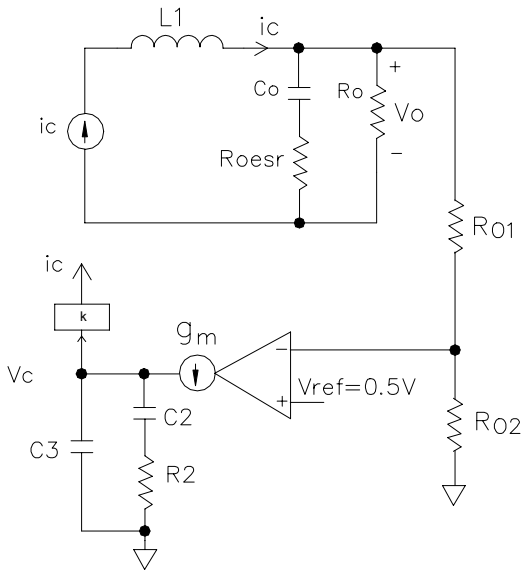


Figure 17. A simple model of synchronous buck converter with current mode control.

Application Information (Cont.)

The transconductance error amplifier (in the SC2446) has a gain g_m of 260μA/V. The target of the compensation design is to select the compensation network consisting of C_2, C_3 and R_2, along with the feedback resistors R_{o1}, R_{o2} and the current sensing gain, such that the converter output voltage is regulated with satisfactory dynamic performance.

With the output voltage V_o known, the feedback gain h and the feedback resistor values are determined using the equations given in the **"Output Voltage Setting"** section with

$$h = \frac{0.5}{V_o}.$$

For the rated output current I_o, the current sensing gain k is first estimated as

$$k = \frac{I_o}{2.1}.$$

From Figure 17, the transfer function from the voltage error amplifier output v_c to the converter output v_o is

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = kR_o \frac{1+\frac{s}{s_{z1}}}{1+\frac{s}{s_{p1}}}.$$

where, the single dominant pole is

$$s_{p1} = \frac{1}{(R_o + R_{oesr})C_o},$$

and the zero due to the output capacitor ESR is

$$s_{z1} = \frac{1}{R_{oesr}C_o}.$$

The dominant pole moves as output load varies.

The controller transfer function (from the converter output v_o to the voltage error amplifier output v_c) is

$$C(s) = \frac{g_m h}{s(C_2 + C_3)} \frac{1+\frac{s}{s_{z2}}}{1+\frac{s}{s_{p2}}},$$

where

$$s_{z2} = \frac{1}{R_2 C_2},$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}.$$

The loop transfer function is then

$$T(s)=G_{vc}(s)C(s).$$

To simplify design, we assume that $C_3 << C_2$, $R_{oesr} << R_o$, selects $S_{p1}=S_{z2}$ and specifies the loop crossover frequency f_c. It is noted that the crossover frequency determines the converter dynamic bandwidth. With these assumptions, the controller parameters are determined as following.

$$C_2 = \frac{g_m h k R_o}{2\pi f_c},$$

$$R_2 = \frac{R_o C_o}{C_2},$$

and

$$C_3 = \frac{R_{oesr} C_o}{R_2} K,$$

with a constant K.

For example, if V_o=2.5V, I_o=15A, f_s=300kHz, C_o=1.68mF, R_{oesr}=4.67mΩ, one can calculate that

$$R_o = \frac{V_o}{I_o} = 167\text{m}\Omega,$$

$$h = \frac{0.5}{V_o} = 0.2,$$

and

$$k = \frac{I_o}{2.1} = 7.14.$$

Application Information (Cont.)

If the converter crossover frequency is set around 1/10 of the switching frequency, f_c = 30kHz, the controller parameters then can be calculated as

$$C_2 = \frac{g_m hk R_o}{2\pi f_c} \approx 0.328\text{nF}.$$

where, gm is the error amplifier transconductance gain (260 $\mu\Omega^{-1}$).

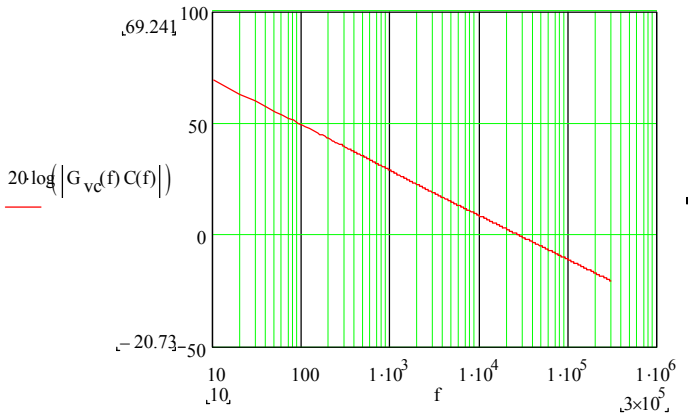
If we use C_2 = 0.33 nF,

$$R_2 = \frac{R_o C_o}{C_2} \approx 848.5\text{k}\Omega,$$

use R_2 = 770kΩ.
With K = 1, it is further calculated that

$$C_3 = \frac{R_{oesr} C_o}{R_2} K \approx 10.2\text{pF},$$

use C_3 = 10pF. The Bode plot of the loop transfer function (magnitude and phase) is shown in Figure 18



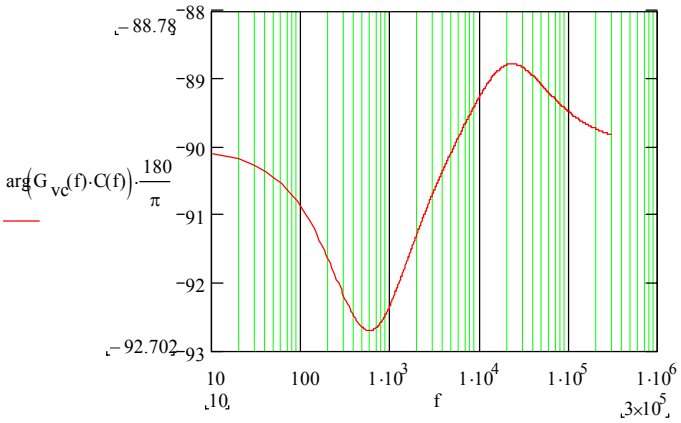


Figure 18. The loop transfer function Bode plot of the example.

It is clear that the resulted crossover frequency is about 27.1 *kHz* with phase margin 91°.

It is noted that the current sensing gain k was first estimated using the DC value in order to quickly get the compensation parameter value. When the circuit is operational and stable, one can further improve the compensation parameter value using AC current sensing gain. One simple and practical method is to effectively measure the output current at two points, e.g. I_{o1} and I_{o2} and the corresponding error amplifier output voltage V_{c1} and V_{c2}. Then, the first order AC gain is

$$k = \frac{\Delta I_o}{\Delta V_c} = \frac{I_{o1} - I_{o2}}{V_{c1} - V_{c2}}$$

With this k value, one can further calculate the improved compensator parameter value using the previous equations.

For example, if one measured that I_{o1}=1A, I_{o2}=15A and V_{c1}=2.139V, V_{c2}=2.457V. k is then calculated as 44. Substituting this parameter to the equations before, one can derive that

$C_2 \approx$ 2.024nF. Select C_2 = 2.2nF.
$R_2 \approx$ 127.3kΩ. Select R_2 = 127kΩ.
$C_3 \approx$ 61.78pF. Select C_3 = 47pF

Application Information (Cont.)

In some initial prototypes, if the circuit noise makes the control loop jittering, it is suggested to use a bigger C_3 value than the calculated one here. Effectively, the converter bandwidth is reduced in order to reject some high frequency noises. In the final working circuit, the loop transfer function should be measured using network analyzer and compared with the design to ensure circuit stability under different line and load conditions. The load transient response behavior is further tested and measured to meet the specification.

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

Power Stage

1) Separate the power ground from the signal ground. In SC2446, the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor.

2) Minimize the size of high pulse current loop. Keep the top MOSFET, bottom MOSFET and the input capacitors within a small area with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFET's to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node.

4) Shorten the gate driver path. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFET's. These inductances may also ring with the gate capacitance.

5) Put the decoupling capacitor for the gate drive power supplies (BST and PVCC) close to the IC and power ground.

Control Section

6) The frequency-setting resistor Rosc should be placed close to Pin 3. Trace length from this resistor to the analog ground should be minimized.

7) Solder the bias decoupling capacitor right across the AVCC and analog ground AGND.

8) Place the Combi-sense components away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R type ceramic capacitor for the Combi-sense capacitor because of their temperature stability.

9) Use an isolated local ground plane for the controller and tie it to the negative side of output capacitor bank.