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SC2544
High Performance Wide Input Range Dual Synchronous Buck Controller

POWER MANAGEMENT

Description

The SC2544 is a high performance dual PWM controller. It is designed to convert a wide ranged input voltage down to two independent output rails. The PWM operations of the two channels are 180 degree out of phase which can greatly reduce the size and the cost of the input capacitors. Synchronous Buck PWM topology and voltage mode control allow high efficiency operation, fast transient responses, and flexible component selection for easy designs. A 10V internal linear regulator provides the bias for the controller, and this voltage is optimized for gate drivers to deliver high efficiency. The power sequencing is fully supported including independent start up, and power good output. In the shut down mode the controller only draws 100nA from the supply. The controller also offers full protection features for the conditions of under voltage, over voltage, and the over current. There is no need for a current sensing resistor because the MOSFET on resistance is used for the sensing element. The switching frequency is adjustable from 100 kHz to 300 kHz. Two packages TSSOP-24 and MLPQ-24 are offered.

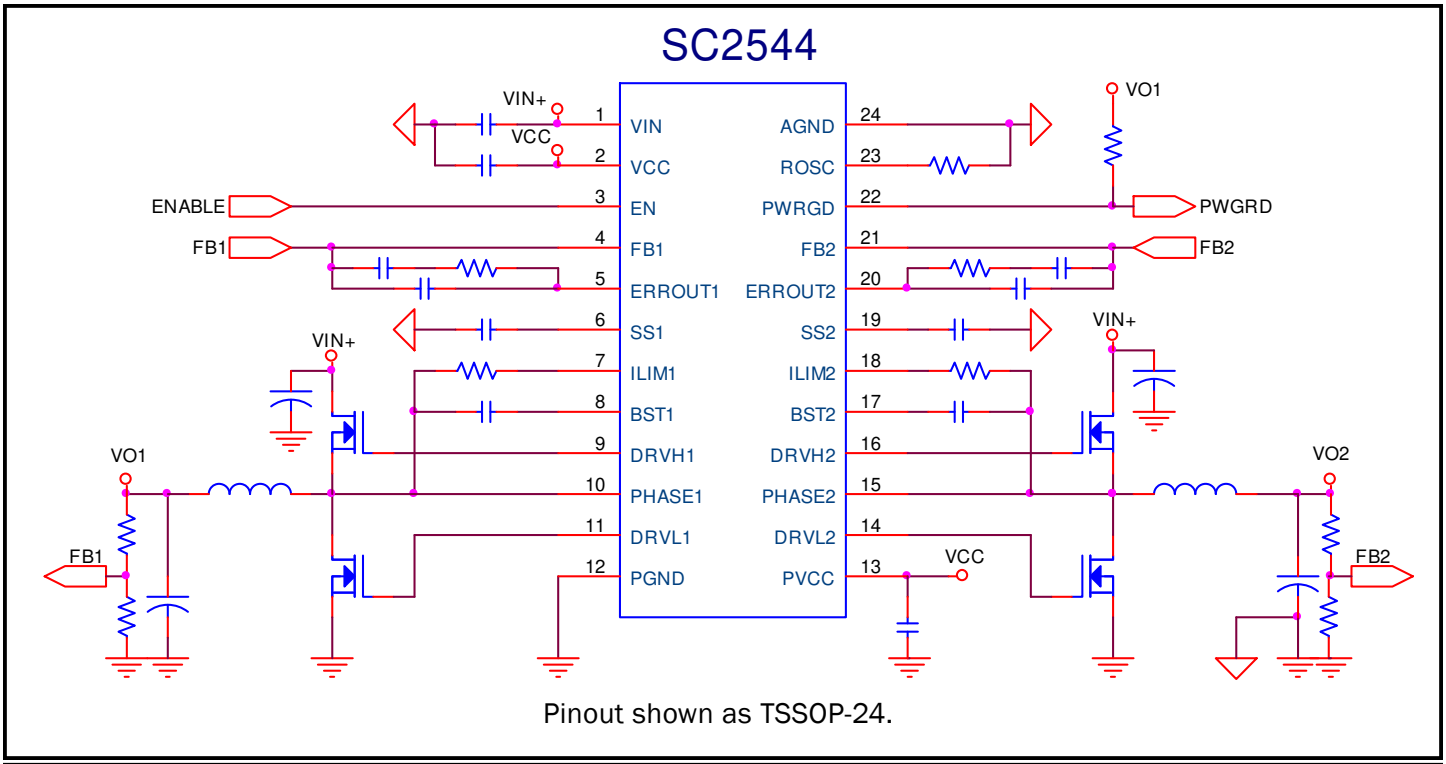
Features

- Independent dual-outputs
- Wide input voltage range: 4.5V~28V
- Adjustable output voltage down to 0.75V
- Sequential and ratiometric start-up
- Power good output
- Synchronous Buck topology with voltage mode control
- Out of phase operation to reduce cost of input capacitor
- 10V internal regulator for gate driver to deliver high efficiency
- Programmable switching frequency: 100kHz~300kHz
- Full protection: UVLO, OVP and programmable OCP
- No need for current sense resistor
- Low shutdown current (100nA typical)
- 24 lead TSSOP and MLPQ packages
- Fully WEEE and RoHS Compliant

Applications

- Systems with 4.5V~28V input
- LCDTV and PDPTV
- Network and telecom systems
- Portable devices

Typical Application Circuit



Pinout shown as TSSOP-24.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction.
Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
BST1, BST2 to PGND	V_{bst}	38	V
VIN to PGND	V_{in}	28	V
ILIM1, ILIM2 and EN to PGND		VIN	V
VCC and PVCC to PGND		14	V
PGND to AGND		+/- 0.3	V
BST1 to PH1, BST2 to PH2, DRVH1 to PH1, DRVH2 to PH2		-0.3 to 14	V
DRVL1, DRVL2 to PGND		-0.3 to VCC	V
PHASE, DRVL to AGND pulse (100nS), peak voltage		-3	V
All Other Pins to AGND		-0.3 to VCC	V
Storage Temperature Range	T_{STG}	-60 to +150	°C
Junction Temperature	T_J	-40 to +150	°C
Lead Temperature (Soldering) 10 Sec for TSSOP-24 Lead Temperature (IR Reflow) for MLPQ-24	T_{LEAD}	260	°C
Thermal Resistance Junction to Case TSSOP-24 MLP-24	θ_{JC}	 23 2	°C/W
Thermal Resistance Junction to Ambient TSSOP-24 MLP-24	θ_{JA}	 78 25	°C/W

Note: This device is ESD sensitive. Use of standard ESD handling precautions is required.

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IN}=16V, Fs=200KHz .

Parameter	Test Conditions	Min	Typ	Max	Unit
Undervoltage Lockout					
Start Threshold	Vcc rising			4.5	V
UVLO Hysteresis	Vcc falling		200		mV
Power Supply					
Operating Current (I_{IN}-I_{PVCC})	SS1/SS2/EN =High, F_S=200kHz		6.0	10	mA
Vcc Regulated	VIN > 12V		10		V
Vcc Load Regulation Level	I_load=0~20mA		2		%
Vcc Line Regulation	Vin=12~24V		2		%
PVcc Operating Current	200KHz, 1nF on HG, 1nF on LG		14		mA
Disable Quiescent Current	EN=low		0.1	10	uA
Main Switcher output					
Line Regulation	5V<Vin <28V		0.5		%
Load Regulation	0A<load current <10A		0.5		%
Output Voltage Accuracy	Without feedback attenuation , T_A = -40 °C to +85 °C	0.735	0.750	0.765	V

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IIN}=16V, Fs=200KHz

Parameter	Test Conditions	Min	Typ	Max	Unit
ENABLE					
EN Ramp Up Threshold Voltage				2	V
EN Ramp Down Threshold Voltage		0.6			V
Soft Start					
Soft Start Charge Current			84		uA
Soft Start Discharge Current			15		uA
Threshold Voltage for DRVL Out of Tri-State	Pull below this level, turning on DRVL (Turn on low side MOSFET)		0.65		V
Error Amplifier					
Voltage Feedback Reference	T_A = -40°C to +85°C	0.735	0.750	0.765	V
Input Bias Current				2	uA
Open Loop Gain (1)			70		dB
Unity Gain Bandwidth (1)			3		MHz
Output Source/Sink Current			1		mA
Slew Rate (1)	100pF capacitive loading		10		V/uS
PWM Comparator to Output Delay (1)			75		nS
Oscillator					
Frequency Range per phase		100		300	kHz
Oscillator Frequency per phase	Rosc=73K OHM	175	210	245	kHz
Oscillator Ramp Peak Voltage			2.3		V
Oscillator Ramp Valley Voltage			1		V
Current Limit					
ILIM Source Current		9	10	11	uA
ILIM Offset Voltage			2		mV
Duty Cycle					
PWM 1 & 2 Maximum Duty Cycle	Rosc = 73K OHM		90		%
PWM 1 & 2 Minimum Duty Cycle	Rosc = 73K OHM		0		%

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{IN}=16V, Fs=200KHz

Parameter	Test Conditions	Min	Typ	Max	Units
Driver					
DRVH1, DRVH2 Drive Current	Source/Sink		0.5		A
DRVL1, DRVL2 Drive Current	Source/Sink		0.5		A
Gate Drive Rise Time (10% to 90%)	Vcc=10V, C_{OUT} = 1000pF		30		nS
Gate Drive Fall Time (90% to 10%)	Vcc=10V, C_{OUT} = 1000pF		30		nS
Dead Time			80		nS
OVP					
OVP Threshold Voltage	Feedback voltage		0.89		V
Power good					
Threshold Voltage	FB1 & FB2 rising		0.675		V
Threshold Voltage	FB1 & FB2 falling		0.57		V
Power Good Pull Down	Sink 1mA			0.4	V

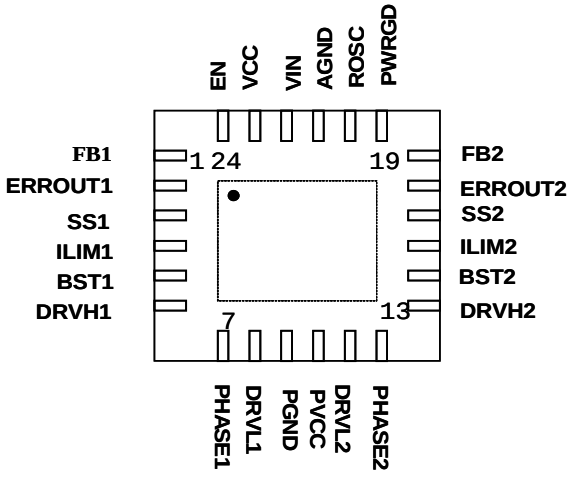
Note:
(1) Guaranteed by design.

Ordering Information

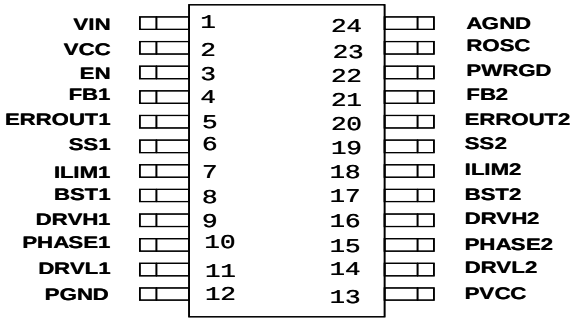
Part Number	Package	Temp. Range (T_A)
SC2544TSTRT(1),(2)	TSSOP-24	-40°C to +85°C
SC2544MLTRT(1),(2)	MLPQ-24	-40°C to +85°C

Notes:
(1) Only available in tape and reel packaging. A reel contains 3000 devices for MLPQ-24 package and 2500 devices for TSSOP-8 package.
(2) Lead free package. Device is fully WEEE and RoHS compiant.

Pin Configurations



Top View



24 PIN TSSOP

Pin Descriptions for SC2544TSTRT (TSSOP)

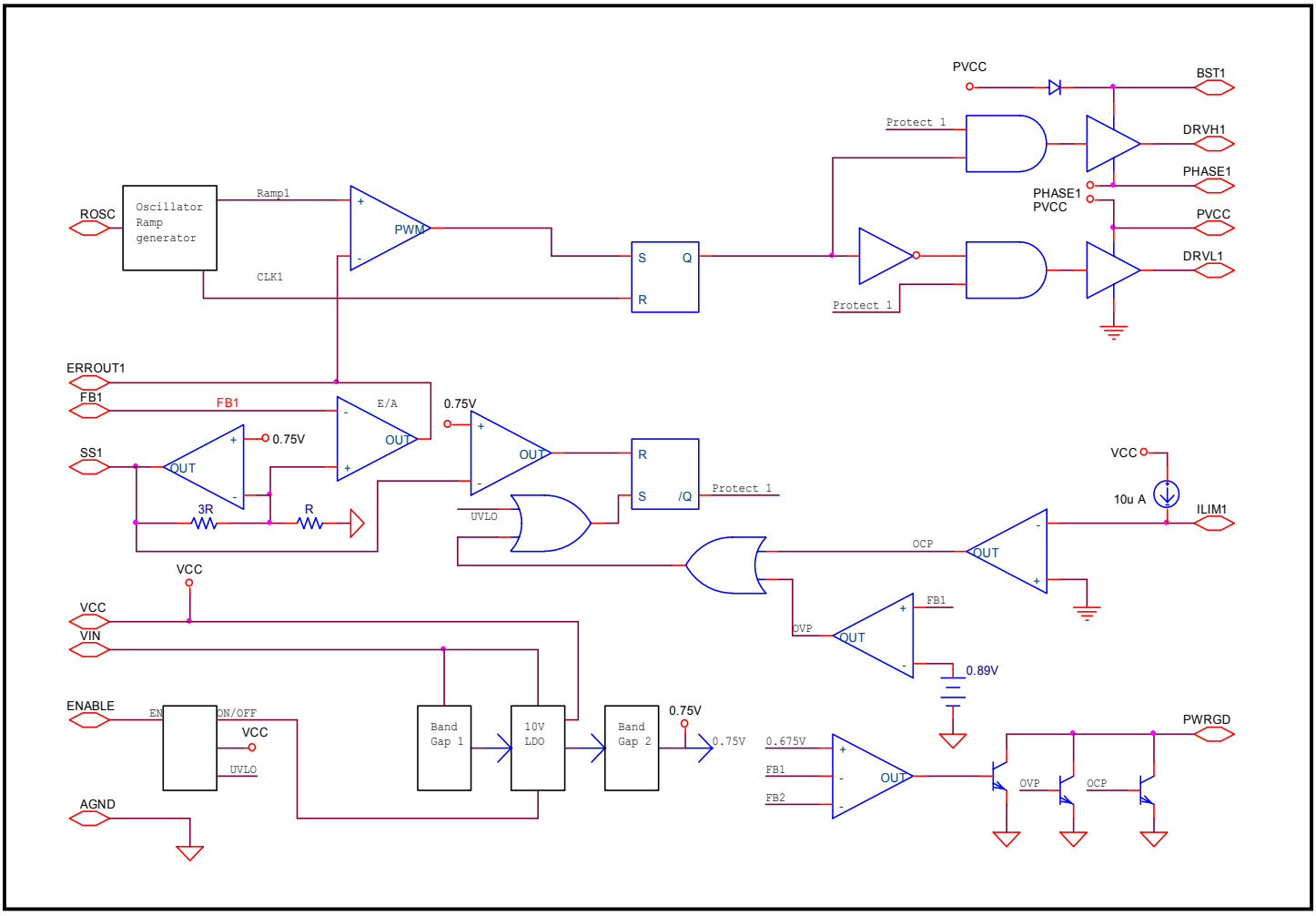
Pin #	Pin Name	Pin Function
1	VIN	Input supply voltage. The range is from 4.5V to 28V.
2	VCC	10V regulator output. Supply voltage for the gate drivers. Connect to VIN pin when Vin<10V.
3	EN	When EN pin is low all outputs are disabled. Typical shutdown current is l00nA.
4	FB1	Negative input of the error amplifier for output1.
5	ERROUT1	Error amplifier output for buck converter1.
6	SS1	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output1 by pulling this pin below 1V.
7	ILIM1	An external resistor connected from this pin to PHASE1 sets the over current shutdown trip point.
8	BST1	Boost capacitor connection for output1 high side gate drive. Connect an external capacitor as shown in the typical application circuit.
9	DRVH1	Gate drive for the high side MOSFET of output1. 180 degrees out of phase with DRVH2.
10	PHASE1	Phase node for output 1.
11	DRVL1	Low side gate drive for output 1.
12	PGND	Power ground of low-side drivers.
13	PVCC	Supply voltage for low-side gate drivers.
14	DRVL2	Low-side gate drive for output 2.
15	PHASE2	Phase node for output 2.
16	DRVH2	Gate drive for the high side MOSFET of OUTPUT2. 180 degrees out of phase with DRVH1.
17	BST2	Boost capacitor connection for OUTPUT2 high side gate drive. Connect an external capacitor as shown in the typical application circuit.
18	ILIM 2	An external resistor connected from this pin to PHASE2 sets the over current shutdown trip point.
19	SS2	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output1 by pulling this pin below 1V.
20	ERROUT2	Error amplifier output for buck converter2.
21	FB2	Negative input of the error amplifier of output2.
22	PWRGD	Open collector output. It is internally pulled low when either output is below the power good threshold level.
23	ROSC	A resistor from this pin to AGND sets oscillator frequency.
24	AGND	Analog signal ground. Star connected to the system ground plane.

Pin Descriptions for SC2544MLTRT (MLPQ)

Pin #	Pin Name	Pin Function
1	FB1	Negative input of the error amplifier for output1.
2	ERROUT1	Error amplifier output for buck converter1.
3	SS1	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output1 by pulling this pin below 1V.
4	ILIM1	An external resistor connected from this pin to PHASE1 sets the over current shutdown trip point.
5	BST1	Boost capacitor connection for output1 high side gate drive. Connect an external capacitor as shown in the typical application circuit.
6	DRVH1	Gate drive for the high side MOSFET of output1. 180 degrees out of phase with DRVH2.
7	PHASE1	Phase node for output 1.
8	DRVL1	Low side gate drive for output 1.
9	PGND	Power ground of low-side drivers.
10	PVCC	Supply voltage for low-side gate drivers.
11	DRVL2	Low-side gate drive for output 2.
12	PHASE2	Phase node for output 2.
13	DRVH2	Gate drive for the high side MOSFET of output2. 180 degrees out of phase with DRVH1.
14	BST2	Boost capacitor connection for output2 high side gate drive. Connect an external capacitor as shown in the typical application circuit.
15	ILIM2	An external resistor connected from this pin to PHASE2 sets the over current shutdown trip point.
16	SS2	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output1 by pulling this pin below 1V.
17	ERROUT2	Error amplifier output for buck converter2.
18	FB2	Negative input of the error amplifier of output2.
19	PWRGD	Open collector output. It is internally pulled low when either output is below the power good threshold level.
20	ROSC	A resistor from this pin to AGND sets oscillator frequency.
21	AGND	Analog signal ground. Star connected to the system ground plane.
22	VIN	Input supply voltage. The range is from 4.5V to 28V.
23	VCC	10V regulator output. Supply voltage for the gate drivers. Connect to VIN pin when Vin<10V.
24	EN	When EN pin is low all outputs are disabled. Typical shutdown current is 100nA.

POWER MANAGEMENT

Block Diagram (One PWM channel shown)



Applications Information

Overview

The SC2544 is a constant frequency 2-phase voltage mode step-down PWM switching controller driving all N-channel MOSFETs. The two channels of the controller operate at 180 degree out of phase from each other. Since input currents are interleaved in a two-phase converter, input ripple current is lower and smaller input capacitance can be used for filtering. Also, with lower inductor current and smaller inductor ripple current per phase, overall I^2R losses are reduced.

Frequency Setting

The frequency of the SC2544 is user- programmable. The oscillator of SC2544 can be programmed with an external resistor from the Rosc pin to the ground. The step-down controller is capable of operating up to 300KHz. The relationship between oscillation frequency versus oscillation resistor is shown in Figure 1.

The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFETs/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

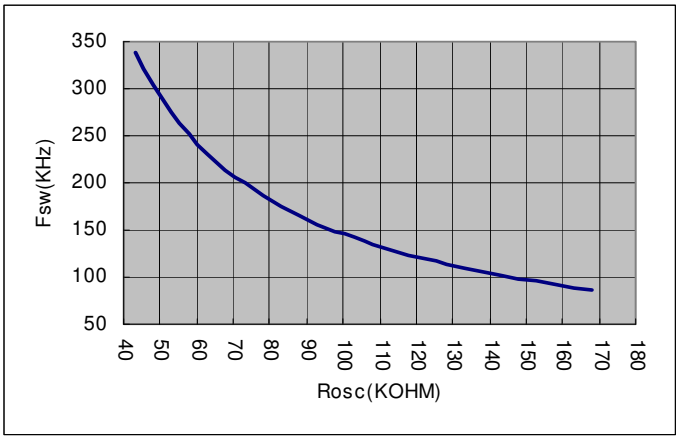


Figure 1. Switching frequency versus Rosc.

Start-up

During start-up, the reference voltage of the error amplifier equals 30% of the voltage on Css (soft-start capacitor) which is connected between the SS pin and ground. When the controller is enabled (by pulling EN pin high), one internal 84uA current source, $I_{SS,}$ (soft start current) will charge the soft-start capacitor gradually. The PWM output starts pulsing when the soft start voltage reaches 1V.

This soft start scheme will ensure the duty cycle to increase slowly, therefore limiting the charging current into the output capacitor and also ensuring the inductor does not saturate. The soft start capacitor will eventually be charged up to 2.5V.
The soft-start sequence is initiated when EN pin is high and Vcc >4.5V or during recovery from a fault condition (OCP, OVP, or UVLO).

The period of start up can be programed by the soft start capacitor:

$$Tss = \frac{Css \times 2.5V}{84\mu A}$$

By connecting different capacitors at SS1 and SS2 pins, VO1 and VO2 will start at different time, achieving sequential start-up for the outputs. Connecting SS1 and SS2 together would make the 2 outputs start and reach steady state values at the same time, achieving ratiometric start-up.

Shutdown

When the EN pin is pulled low, an internal 15uA current source discharges the soft-start capacitor and DRVH/ DRVL signals stop pulsing. The output voltage ramps down at a rate determined by the load condition.

The SC2544 can also be shutdown by pulling down directly on the SS pin. The designer needs to consider the slope of the SS pin voltage and choose a suitable pull down resistor to prevent the output from undershooting.

Shutdown can also be triggered when an OCP condition occurs. When an OCP condition is detected, DRVH and DRVL will stop pulsing and enter a “tri-state shutdown” with the output voltage ramping down at a rate determined by the load condition. The internal 15uA current source will begin discharging the soft-start capacitor and when the soft-start voltage reaches 0.65V, DRVL will go high.

Applications Information (Cont.)

Over Current Protection (OCP)

The inductor current is sensed by using the low side MOSFET $R_{ds(on)}$. After low side MOSFET is turned on, the OCP comparator starts monitoring the voltage drop across the MOSFET. The OCP trip level is programmed by the resistor from the ILIM pin to the phase node. There is an internal current source that flows out of the ILIM pin which will generate a voltage drop on the setting resistor. When the sum of the setting resistor voltage and the MOSFET drain to source voltage is less then zero, the OCP condition will be flagged. This functionality is depicted in Figure 2.
The following formula is used to set the OCP level

$$10\mu A \times R_{ILIM} = I_{L\_PEAK} \times R_{DS(ON)}$$

When OCP is tripped, both high side and low side MOSFETs will be turned off and this condition is latched. At the same time, the soft start cap will be discharged by the internal current source of 15uA. When the Vss drops bellow 0.65V, the DRVL pin will go high again.

To avoid switching noise during the phase node commutation, a 100nS blanking time is built in after the low side MOSFET is turned on, as shown in Fig. 3.

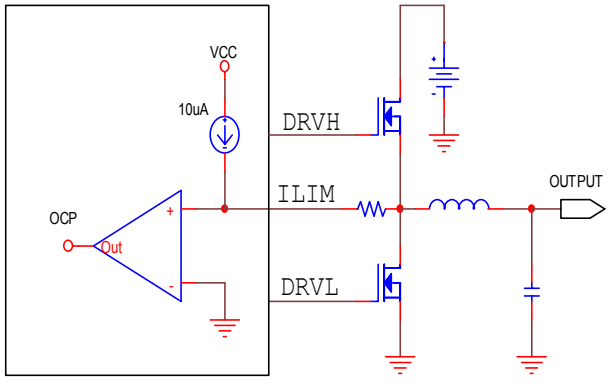


Figure 2. Block diagram of over current protection.

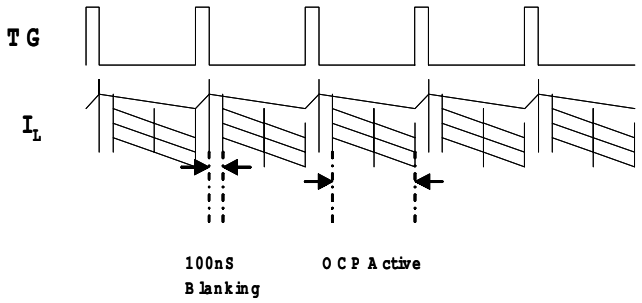


Figure 3. OCP comparator timing chart.

Under Voltage Lock Out (UVLO)

The UVLO circuitry monitors Vcc and the soft start begins once Vcc ramps up above 4.5V. There is a built in 200mV hysteresis for the UVLO ramp down threshold. The gate driver output will be in "tri-state" (both high side and low side MOSFET off) once Vcc ramps down bellow 4.2V (typical), and the soft start cap will be discharged by internal 15uA current sink.

Over Voltage Protection (OVP)

The OVP circuitry monitors the feedback voltages, If either feedback voltage exceeds 0.89V, the OVP condition is registered. Under this condition, the DRVH pins will be pulled low, and the DRVL pins will be pulled high. This will create a "crow bar" condition for the input power rail in case the high side MOSFET is failed short. The crow bar operation may trip the input supply to prevent the load from seeing more voltage.

Power Good Output

The power good is an open collector output. The PWRGD pin is pulled low at start up if any of the two feedback voltages below 90% of its regulation level. The ramp down threshold of the signal is 80% of the regulation target. External pull up is required for the PWRGD pin, and the pull up resistor should be chosen such that the pin does not sink more than 2mA when PWRGD is low.

Applications Information (Cont.)

General Design Procedure for a Step-down Power Converter

Selection criterias and design procedures for the following parameters are described:

1) Output inductor (L) type and value
2) Output capacitor (C_o) type and value
3) Input capacitor (C_{in}) type and value
4) Power MOSFETs
5) Current sensing and limiting circuit
6) Voltage sensing circuit
7) Loop compensation network

The following step-down converter specifications are needed:

Input voltage range: $V_{in,min}$ and $V_{in,max}$
Input voltage ripple (peak-to-peak): DV_{in}
Output voltage: V_o
Output voltage accuracy: e
Output voltage ripple (peak-to-peak): DV_o
Nominal output (load) current: I_o
Maximum output current limit: $I_{o,max}$
Output (load) current transient slew rate: dI_o (A/ s)
Circuit efficiency: η

Inductor (L) and Ripple Current

Both step-down controllers in the SC2544 operate in synchronous continuous-conduction mode (CCM) regardless of the output load level. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductance but it takes longer to change the inductor current during load transients. Conversely smaller inductance results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.

Assuming that the inductor current ripple (peak-to-peak) value is δ *I_o, the inductance value will then be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}.$$

The peak current in the inductor becomes

$$(1+\delta/2)*Io$$

and the RMS current is

$$I_{L,rms} = I_o\sqrt{1+\frac{\delta^2}{12}}.$$

The followings are to be considered when choosing inductors.

a) Inductor core material: For higher efficiency applications above 300 KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 300 KHz but with attendant higher core losses.

b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.

c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR and ESL as shown in Figure 4.

Figure 4. An equivalent circuit of *output*.

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t).$$

This basic equation illustrates the effects of ESR, ESL, and C_o on the output voltage.

Applications Information (Cont.)

The first term is the DC voltage across C_o at time *t=0*. The second term is the voltage variation caused by the charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is

$$\Delta v_C \approx \frac{\delta I_o}{8 C_o f_s},$$

the ripple-voltage due to ESL is

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D},$$

and the ESR ripple-voltage is

$$\Delta v_{ESR} = R_{esr} \delta I_o.$$

Aluminum capacitors (e.g. electrolytic) have high capacitances and low ESLs. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR. Other types to choose are solid OS-CON, POSCAP, and tantalum.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To meet the steady state output ripple-voltage spec, the ESR should satisfy

$$R_{esr1} < \frac{\Delta V_O}{\delta I_O}$$

To limit the dynamic output voltage overshoot/ undershoot within a (say 3%) of the steady state output voltage from no load to full load, the ESR value should satisfy

$$R_{esr2} < \frac{3\% V_O}{I_O}$$

Then, the required ESR value of the output capacitors should be

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}.$$

The voltage rating of aluminum capacitors should be at least $1.5V_o$. The RMS current ripple rating should also be greater than

$$\frac{\delta I_o}{2\sqrt{3}}.$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple caused by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{esr}}.$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant. For example, if a 10 μF, 4mΩ ceramic capacitor is connected in parallel with 2x1500 μF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100 μF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100 μF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formula.

$$C_{eq}(\omega) = \frac{(R_{1a}+R_{1b})^2 \omega^2 C_{1a}^2 C_{1b}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}^2 C_{1a} + R_{1b}^2 C_{1b})\omega^2 C_{1a} C_{1b} + (C_{1a}+C_{1b})}$$

Applications Information (Cont.)

$$C_{eq}(\omega) = \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}^{\ 2}C_{1b}^{\ 2} + (R_{1b}C_{1b}^{\ 2} + R_{1a}C_{1a}^{\ 2})}{(R_{1a}+R_{1b})^2\omega^2 C_{1a}^{\ 2}C_{1b}^{\ 2} + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors, respectively (Figure 5).

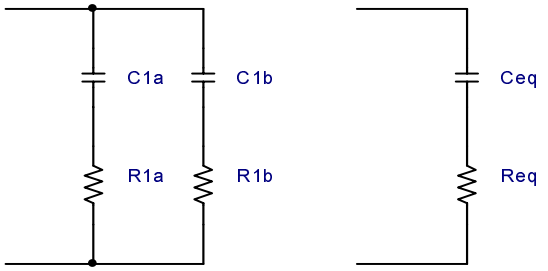


Figure 5. Equivalent RC branch.

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b} = R_1$ and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1.$$

Input Capacitor (Cin)

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 6.

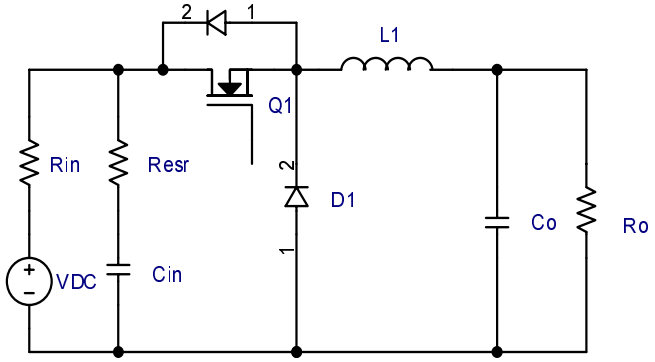


Figure 6. A simple model for the converter input.

In Figure 6 the DC input voltage source has an internal impedance R_{in} and the input capacitor C_{in} has an ESR of R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 7.

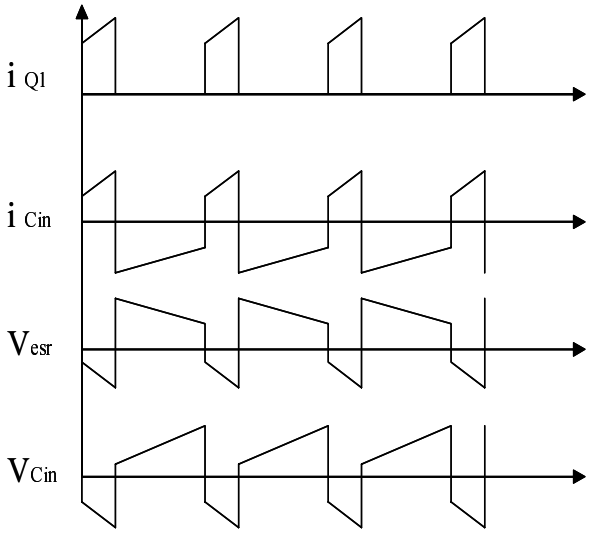


Figure 7. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFETs on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o\sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + \frac{D}{\eta^2}(1-D)]}.$$

The power dissipated in the input capacitors is then

$$P_{Cin} = I_{Cin}^{\ 2}R_{esr}.$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. It is common pratice that multiple capacitors are placed in parallel to increase the ripple current handling capability.

Applications Information (Cont.)

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_o.$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_C \approx \frac{DI_o}{C_{in}f_s},$$

From these two expressions, C_{IN} can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2544 operate at 180 degrees from each other. If both step-down channels in the SC2544 are connected to the same input rail, the input RMS currents will be reduced. Ripple cancellation effect of interleaving allows the use of smaller input capacitors.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the *RMS* value of the ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be D_1, D_2 and I_{o1}, I_{o2}, respectively.

If $D_1<0.5$ and $D_2<0.5$, then

$$I_{Cin} \approx \sqrt{D_1 I_{o1}^2 + D_2 I_{o2}^2}.$$

If $D_1>0.5$ and $(D_1-0.5) < D_2<0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + (D_1-0.5)(I_{o1}+I_{o2})^2 + (D_2-D_1+0.5) I_{o2}^2}.$$

If $D_1>0.5$ and $D_2 < (D_1-0.5) < 0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + D_2(I_{o1}+I_{o2})^2 + (D_1-D_2-0.5) I_{o2}^2}.$$

If $D_1>0.5$ and $D_2 > 0.5$, then

$$I_{Cin} \approx \sqrt{(D_1+D_2-1)(I_{o1}+I_{o2})^2 + (1-D_2) I_{o1}^2 + (1-D_1) I_{o2}^2}.$$

Choosing Power MOSFETs

Main considerations in selecting the MOSFET's are power dissipation, MOSFETs cost, and packaging. Switching losses and conduction losses of the MOSFET's are directly related to the total gate charge (C_g) and channel on-resistance ($R_{ds(on)}$). In order to judge the performance of MOSFET's, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 8.

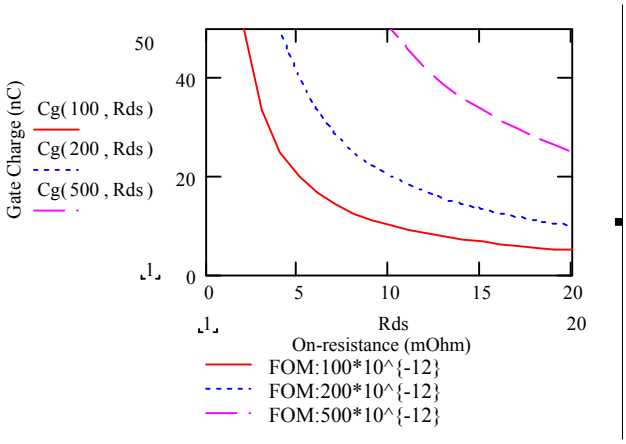


Figure 8. Figure of Merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFET's with both low C_g and low $R_{ds(on}$. Usually a trade-off between $R_{ds(on}$ and C_g has to be made.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET's with low C_g are used for the top switch and MOSFET's with low $R_{ds(on)}$ are used for the bottom switch.

MOSFET power dissipation consists of
a) conduction loss due to the channel resistance $R_{ds(on)}$;
b) switching loss due to the switch rise time t_r and fall time t_f; and
c) the gate loss due to the gate resistance R_G.

Applications Information (Cont.)

Top Switch

The *RMS* value of the top switch current is calculated as

$$I_{Q1,rms} = I_o\sqrt{D(1+\frac{\delta^2}{12})}.$$

The conduction losses are then

$$P_{tc} = I_{Q1,rms}{}^2 R_{ds(on)}.$$

$R_{ds(on)}$ varies with temperature and gate-source voltage. Curves showing $R_{ds(on)}$ variations can be found in manufacturers' data sheet. From the Si4860 datasheet, $R_{ds(on)}$ is less than 8mΩ when V_{gs} is greater than 10V. However $R_{ds(on)}$ increases by 50% as the junction temperature increases from 25°C to 110°C.

The switching losses can be estimated using the simple formula

$$P_{ts} = \frac{1}{2}(t_r + t_f)(1+\frac{\delta}{2})I_o V_{in} f_s.$$

where t_r is the rise time and t_f is the fall time of the switching process. Different manufactures have different definitions and test conditions for t_r and t_f. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 9.

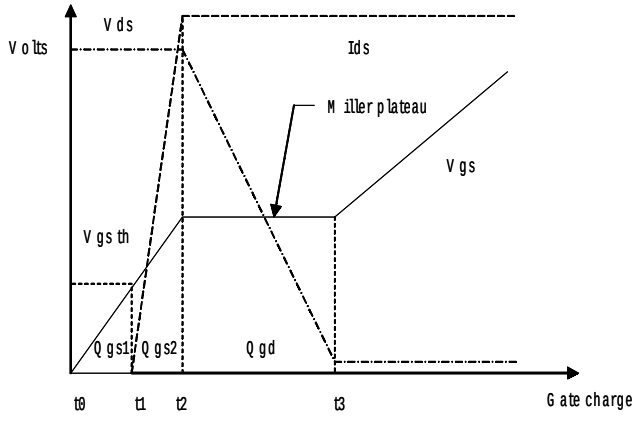


Figure 9. MOSFET switching characteristics

In Figure 9, Q_{gs1} is the gate charge needed to bring the gate-to-source voltage V_{gs} to the threshold voltage V_{gs_th}.

Q_{gs2} is the additional gate charge required for the switch current to reach its full-scale value I_{ds}, and Q_{gd} is the charge needed to charge gate-to-drain (Miller) capacitance when V_{ds} is falling.

Switching losses occur during the time interval [t_1, t_3]. Defining $t_r = t_3 - t_1$ and t_r can be approximated as

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}.$$

where R_{gt} is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance R_{gi}, external resistance R_{ge} and the gate resistance R_g within the MOSFET :

$$R_{gt} = R_{gi} + R_{ge} + R_g.$$

V_{gsp} is the Miller plateau voltage shown in Figure 9. Similarly an approximate expression for t_f is

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}.$$

Only a portion of the total losses $P_g = Q_g V_{cc} f_s$ is dissipated in the MOSFET package. Here Q_g is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total power loss of the top switch is then

$$P_t = P_{tc} + P_{ts} + P_{tg}.$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction losses are inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Applications Information (Cont.)

Bottom Switch

The *RMS* current in bottom switch is given by

$$I_{Q2,rms} = I_o\sqrt{(1-D)(1+\frac{\delta^2}{12})}.$$

The conduction losses are then

$$P_{bc} = I_{Q2,rms}^{\ 2} R_{ds(on)}.$$

where $R_{ds(on)}$ is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g. V_{in}=12V, V_o=1.5V), the duty ratio D will be small. Since the bottom switch conducts with duty ratio (1-D), the corresponding conduction losses can be quite high.

Due to non-overlapping conduction between the top and the bottom MOSFET's, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss is negligible due to near zero-voltage switching.

The gate losses are estimated as

$$P_{bg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total bottom switch losses are then

$$P_b = P_{bc} + P_{bg}.$$

Once the power losses for the top and bottom MOSFET's are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ($T_{j,max}$, usually 125°C) is not exceeded under the worst-case condition. The equivalent thermal impedance from junction to ambient (θ_{ja}) should satisfy

$$\theta_{ja} \le \frac{T_{j,max} - T_{a,max}}{P_{loss}}.$$

θ_{ja} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area, and the air flow condition (natual or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

Main Control Loop Design

The goal of compensation is to shape the frequency response charatericstics of the buck converter to achieve a better DC accuracy and a faster transient response for the output voltage, while maintaining the loop stability.

The block diagram in Figure 10 represents the control loop of a buck converter designed with the SC2544. The control loop consists of a compensator, a PWM modulator, and an LC filter.

The LC filter and PWM modulator represent the small signal model of the buck converter operating at fixed switching frequency. The transfer function of the model is given by:

$$\frac{V_O}{V_C} = \frac{V_{IN}}{V_m} \cdot \frac{1 + sR_{ESR}C}{1 + sL/R + s^2LC}$$

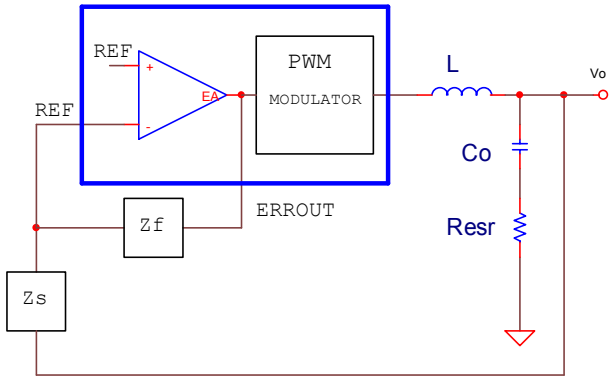


Fig. 10. Block diagram of the control loop.

where V_{IN} is the input voltage, Vm is the amplitude of the internal ramp, and R is the equivalent load.

The model is a second order system with a finite DC gain, a complex pole pair at Fo, and an ESR zero at Fz, as shown in Figure 11. The locations of the poles and zero are determined by:

$$F_O = \frac{1}{2\pi\sqrt{LCo}}$$

$$F_Z = \frac{1}{2\pi R_{esr} Co}$$

Applications Information (Cont.)

The compensator in Figure 10 includes an error amplifier and impedance networks Zf and Zs. It is implemented by the circuit in Figure 12. The compensator provides an integrator, double poles, and double zeros. As shown in Figure 11, the integrator is used to boost the gain at low frequency. Two zeros are introduced to compensate excessive phase lag at the loop gain crossover due to the integrator (-90deg) and the complex pole pair (-180deg). Two high frequency poles are designed to compensate the ESR zero and to attenuate high frequency noise.

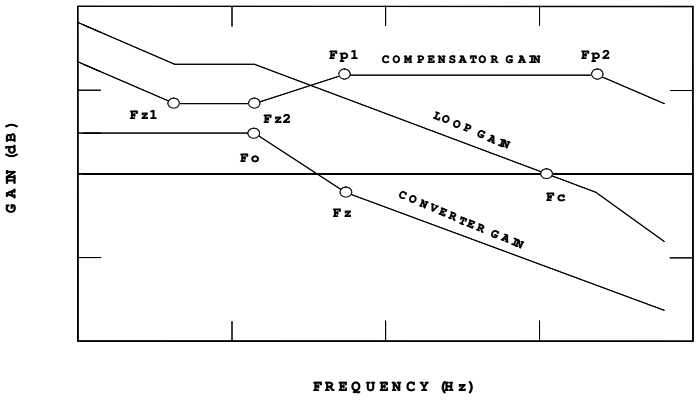


Fig. 11. Bode plots for control loop design.

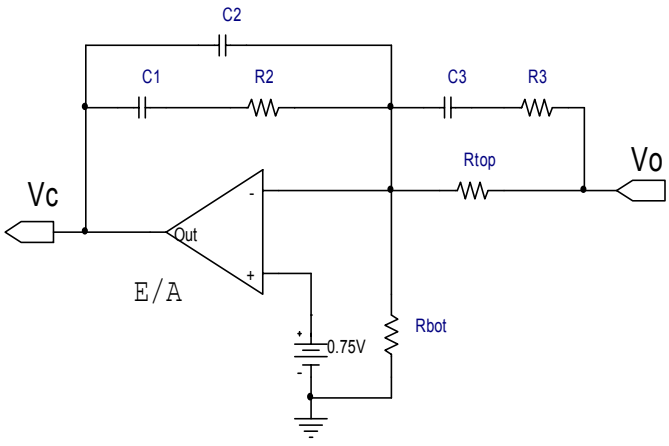


Fig. 12. Compensation network.

A resistive divider is used to program the output voltage. The top resistor Rtop of the divider in Fig. 12 can be chosen from 20kΩ to 30kΩ. Then the bottom resistor Rbot is found from:

$$Rbot = \frac{0.75V}{Vo - 0.75V} * Rtop$$

where 0.75V is the internal reference voltage of the SC2544.

The other components of the compensator can be calculated using following design procedure:

(1). Plot the converter gain, including LC filter and PWM modulator.

(2). Select the open loop crossover frequency Fc located at 10% to 20% of the switching frequency. At Fc, find the required DC gain.

(3). Use the first compensator pole Fp1 to cancel the ESR zero Fz.

(4). Have the second compensator pole Fp2 at half the switching frequency to attenuate the switching ripple and high frequency noise.

(5). Place the first compensator zero Fz1 at or below 50% of the power stage resonant frequency Fo.

(6). Place the second compensator zero Fz2 at or below the power stage resonant frequency Fo.

A MathCAD program is available upon request for the calculation of the compensation parameters.

Applications Information (Cont.)

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

Power Stage

1) Separate the power ground from the signal ground. In SC2544 design, use an isolated local ground plane for the controller and tie it to power grand.

2) Minimize the size of the high pulse current loop. Keep the top MOSFET, the bottom MOSFET and the input capacitors within a small area with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFETs to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node if the EMI is a concern for the system.

4) Shorten the gate drive trace. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFET's. These inductances may also ring with the gate capacitance.

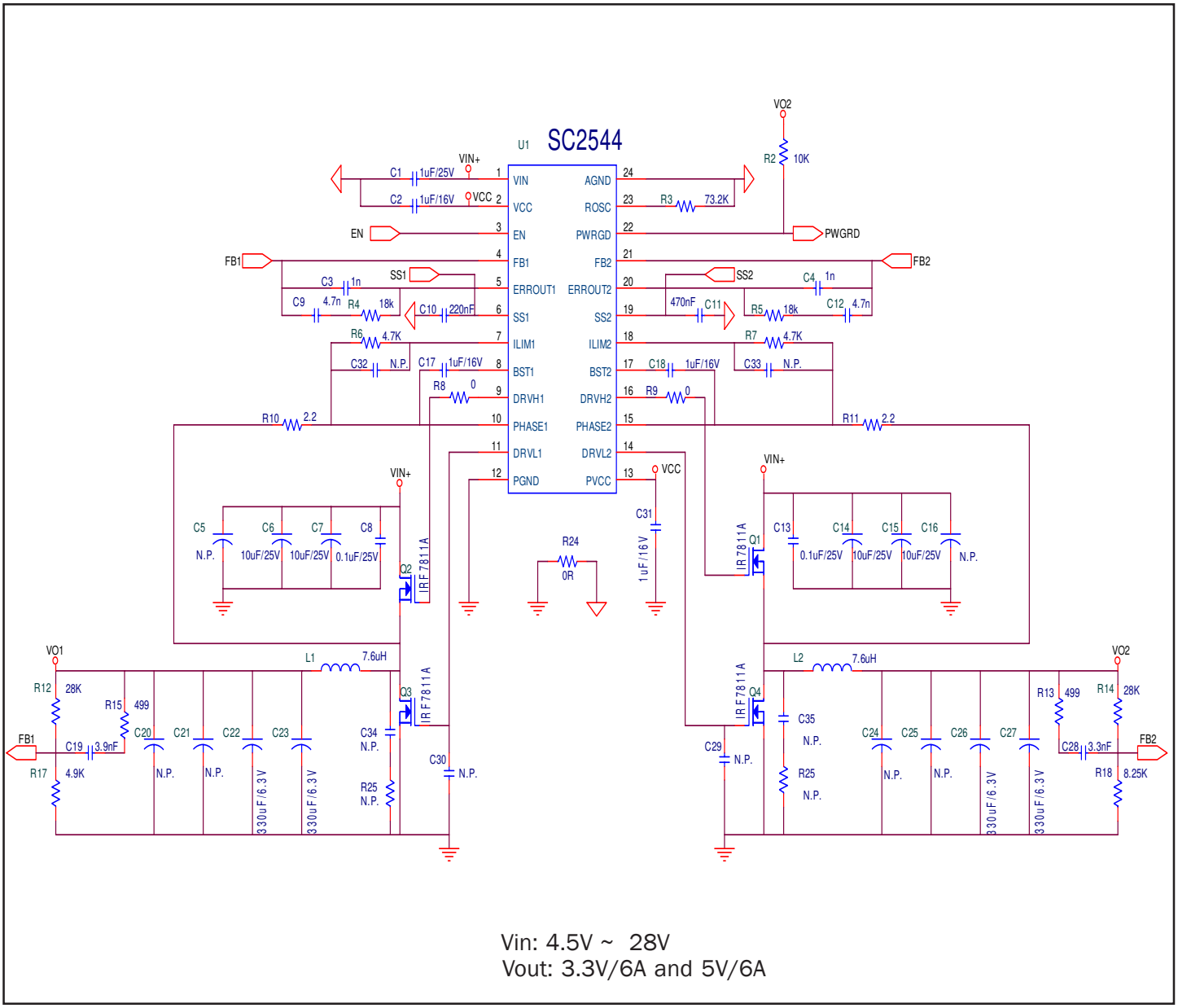
5) Put the decoupling capacitor for the gate drive power supplies (BST and PVCC) close to the IC and power ground.

Control Section

6) The frequency-setting resistor Rosc should be placed close to Pin 23. Trace length from this resistor to the analog ground should be minimized.

7) Place the bias decoupling capacitor right across the VCC and analog ground AGND.

Typical Application Circuit

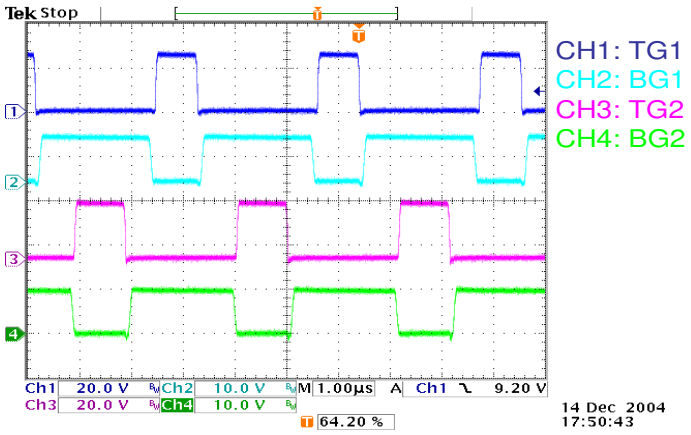


Vin: 4.5V ~ 28V
Vout: 3.3V/6A and 5V/6A

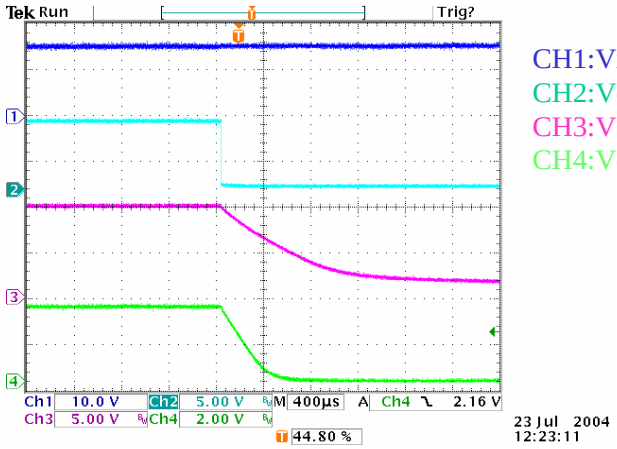
Evaluation Board - Bill of Material

Ref	Qty	Reference	Part Number/Value	Manufacturer
1	1	C1	1uF, 25V, X5R,Ceramic, 0805	Any
2	3	C2,C18,C31	1uF, 16V, X5R, Ceramic , 0805	Any
3	4	C3,C4,C34,C35	1nF, Ceramic 0805	Any
4	14	L1, L2, C5, C16, C20, C21, C24, C24, C29,C30, C32, C33,R25	N.P.	
5	4	C6, C7, C14, C15	10uF, 25V, X5R , Ceramic 1206	Panasonic, ECJ3YB1E106M
6	2	C8, C13	0.1uF, 25V, 0603	Any
7	2	C12, C9	4.7nF, Ceramic, 0603	Any
8	1	C10,	220nF, Ceramic, 0603	Any
9	1	C11	470nF, Ceramic, 0603	Any
10	1	C17	1nF, Ceramic, 0603	Any
11	2	C28,C19	3.3nF, Ceramic, 0603	Any
12	2	C22, C23, C26, C27	33uF, 6.3V, 18mohm, PosCap	Sanyo, 6TPE330MIL
13	2	L1, L2	7.6uH, 6.8A, 16mohm	Sumida, CDRH127
14	4	Q1, Q2, A3, Q4	IRF7811A	IR
15	1	R2	10K, 0603	Any
16	1	R3	73.2K, 0603	Any
17	2	R5, R4	18K, 0603	Any
18	1	R6	6.8K, 0603	Any
19	1	R7	4.7K, 0603	Any
20	1	R10	4.7, 0603	Any
21	1	R25, R11	4.7, 0603	Any
22	2	R14, R12	2.2, 0603	Any
23	2	R15,R13	499, 0603	Any
24	2	R18, R17	4.9K, 0603	Any
25	1	R24	0, 0603	Any
26	1	U1	SC2544	Semtech

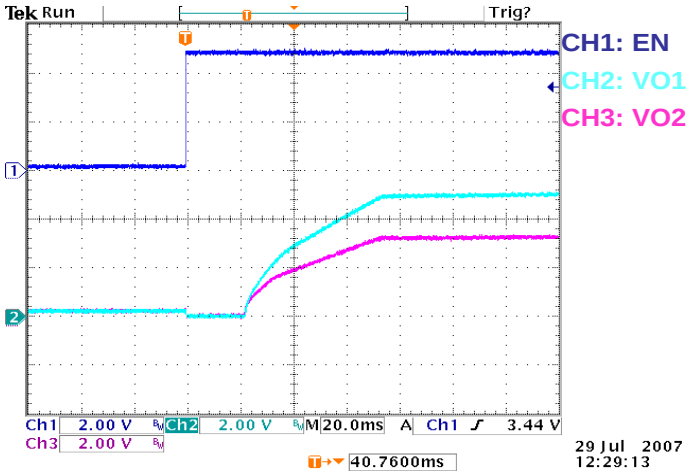
Typical Characteristics



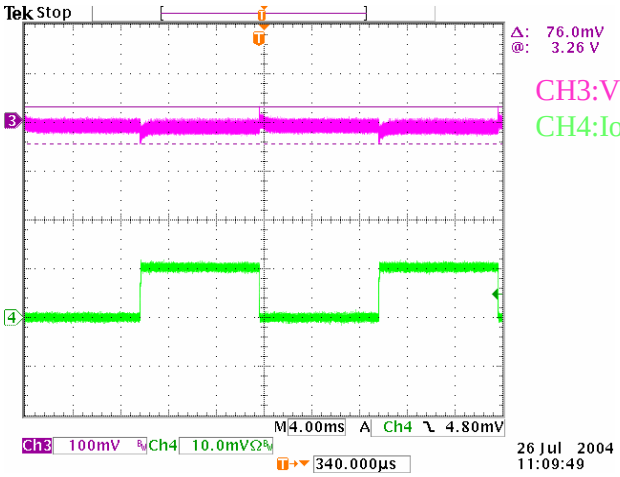
Gate waveform



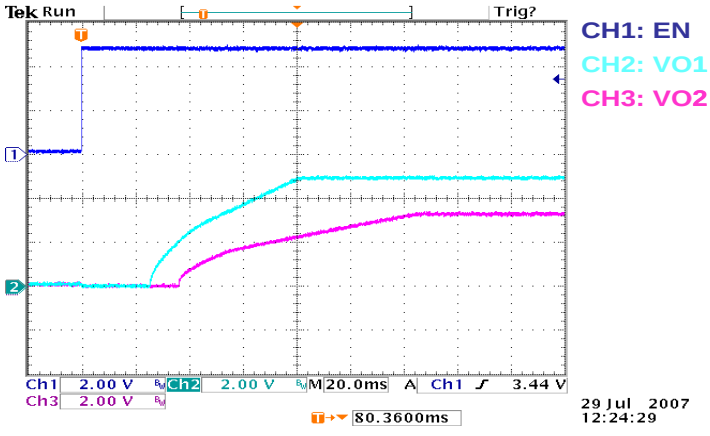
Shut down by pulling down EN pin voltage.



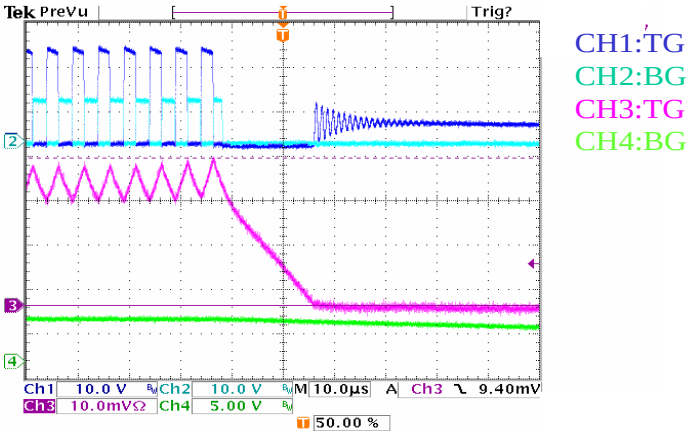
Ratiometric start up(connect SS1,SS2 together).



Transient response(0-5A).

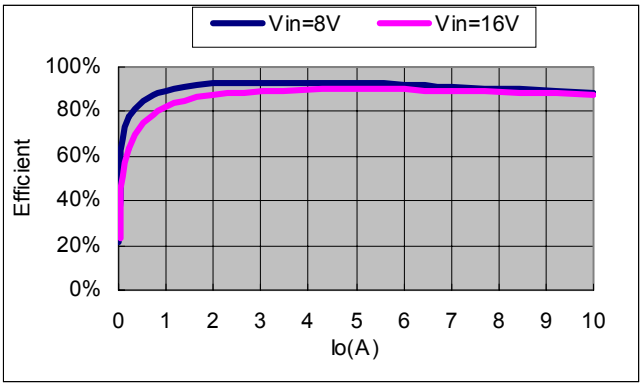


Sequential start up (Seperate SS1,SS2).

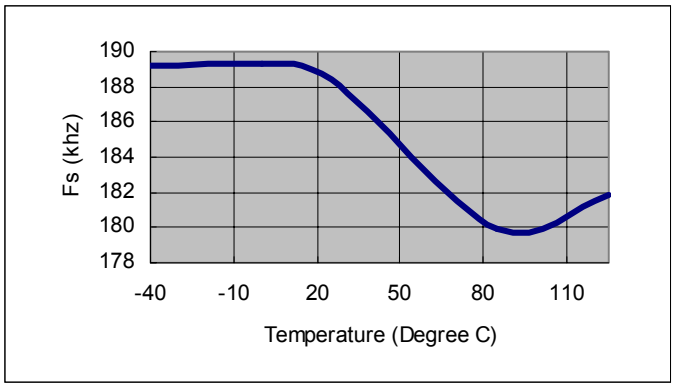


Over current protection (5A/10mV)

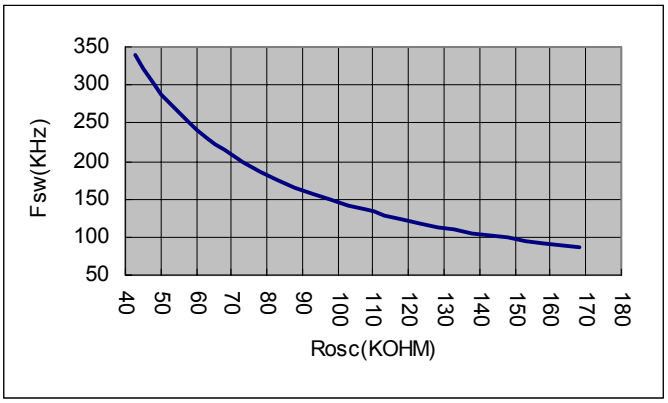
Typical Characteristics (Cont.)



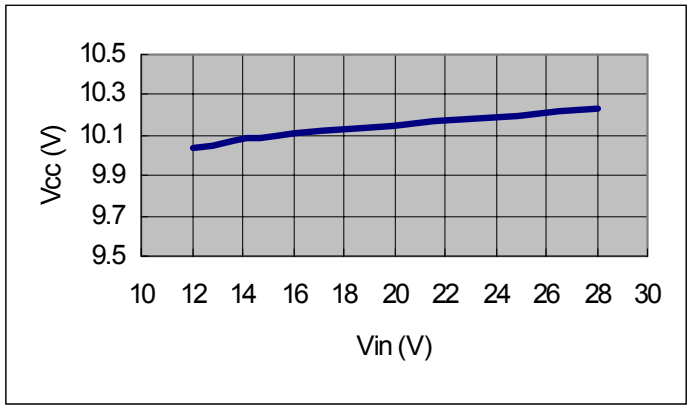
Efficiency Curve for Vout=3.3V.



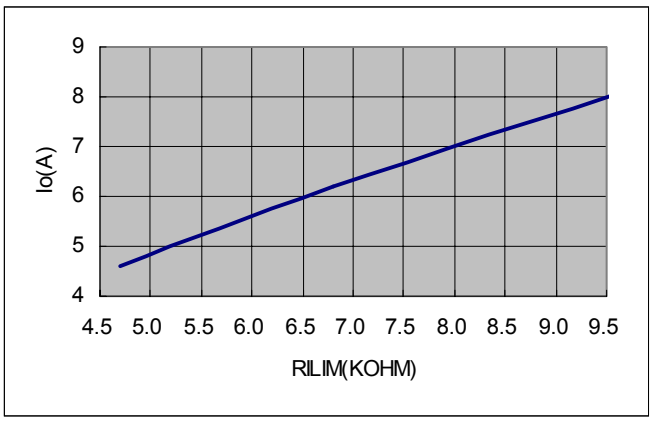
Freq. vs. Temp. (Rosc=75kohm, Vin=16V).



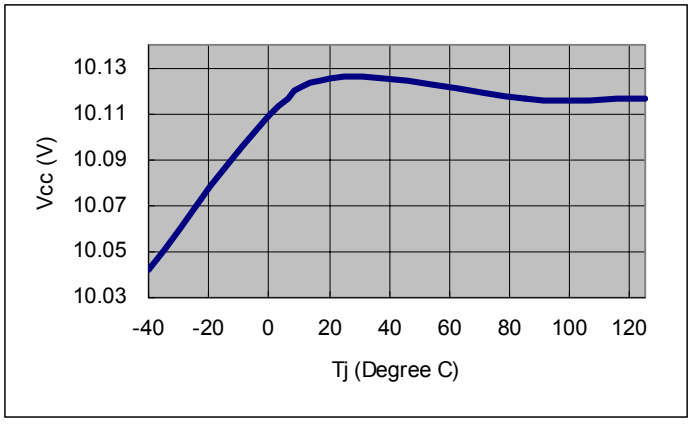
Operating frequency vs. Rosc.



Vcc vs. Vin (Ta=25 Degree C).

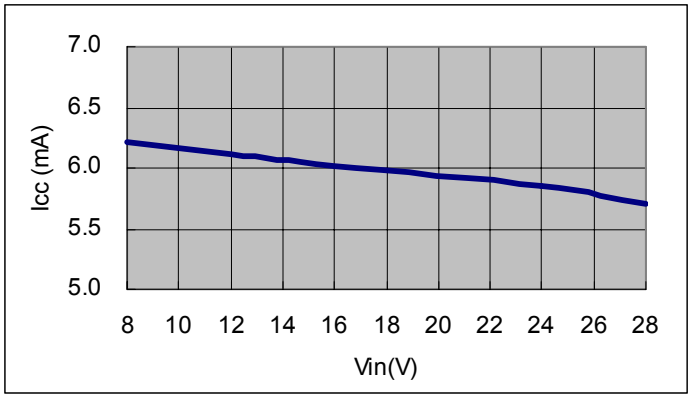


RILIM vs. OCP (Vi=12V).

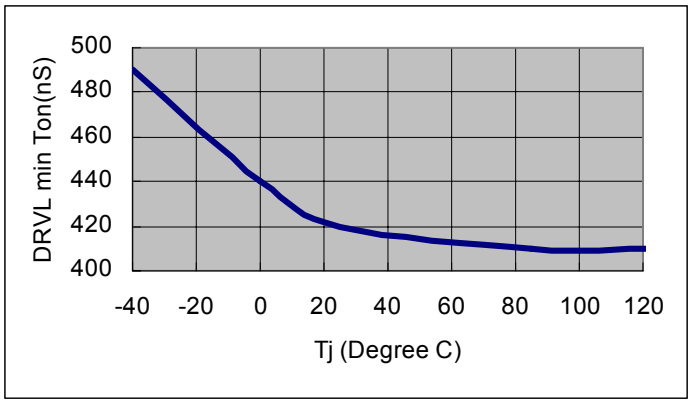


Vcc vs. Temp.

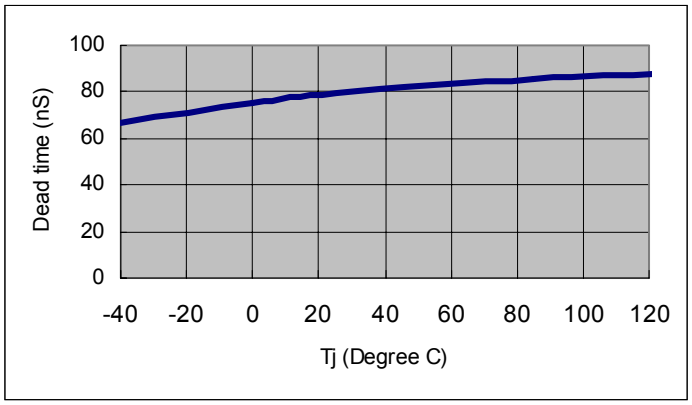
Typical Characteristics (Cont.)



Icc vs. Vin (25 DegreeC).

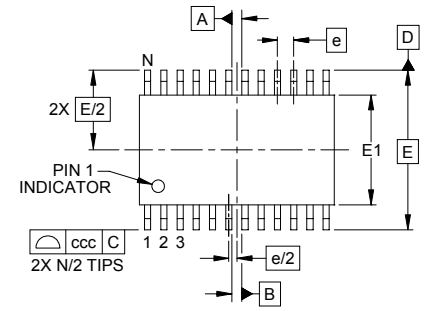


DL min Ton vs. Tj (Vin=16V).

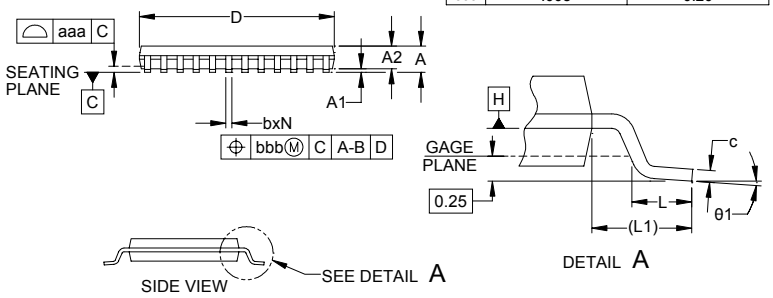


Dead time vs. Tj (Vin=16V, DH falling to DL rising).

Outline Drawing - TSSOP-24



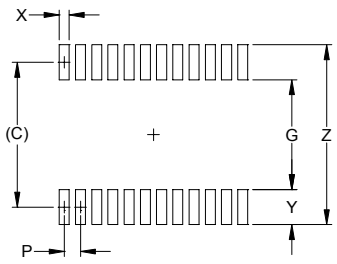
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.303	.307	.311	7.70	7.80	7.90
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	24			24		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AD.

Land Pattern - TSSOP-24



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

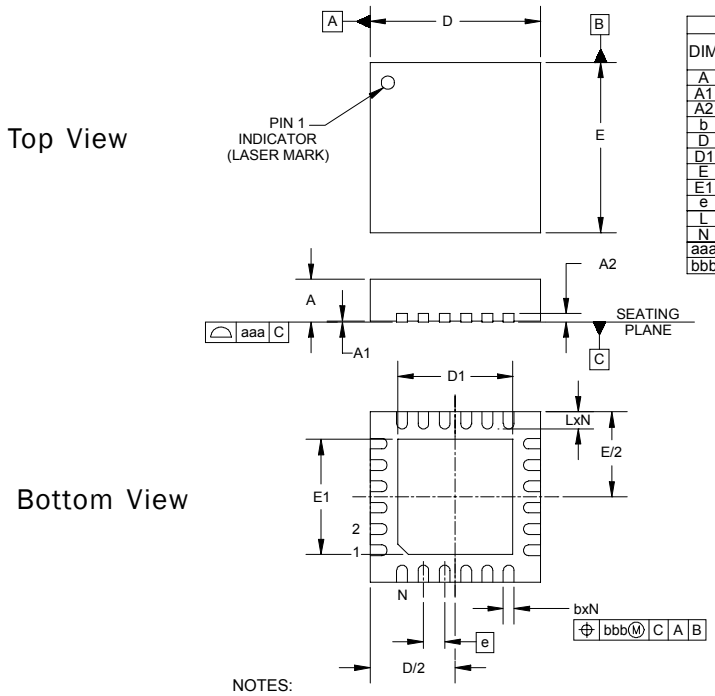
NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

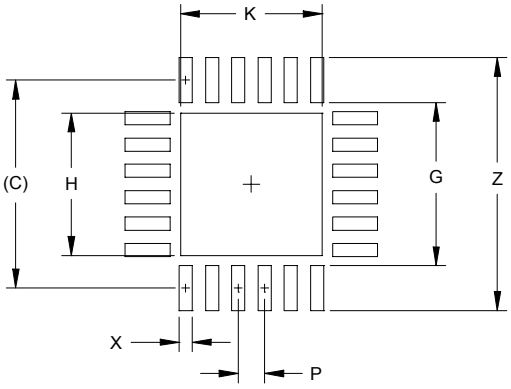
Outline Drawing - MLPQ-24 (4 x 4mm)



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.151	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.151	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.011	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPQ-24 (4 x 4mm)



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.155)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:
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