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## POWER MANAGEMENT

### Description

The SC2595 is an integrated linear DDR termination device, which provides a complete solution for DDR termination designs; while meeting the JEDEC requirements of SSTL-2 specifications for DDR-SDRAM termination.

The SC2595 can source and sink 1.5A current at the output  $V_{TT}$  while maintaining excellent load regulation.

$V_{TT}$  is designed to track the  $V_{REF}$  voltage with a tight tolerance over the entire current range while preventing shoot through on the output stage.

A  $V_{SENSE}$  pin is incorporated to provide excellent load regulation, along with a buffered reference voltage.

The SC2595 incorporates a disable function built into the  $AV_{CC}$  pin to tri-state the output during Suspend To Ram (STR) states.

### Features

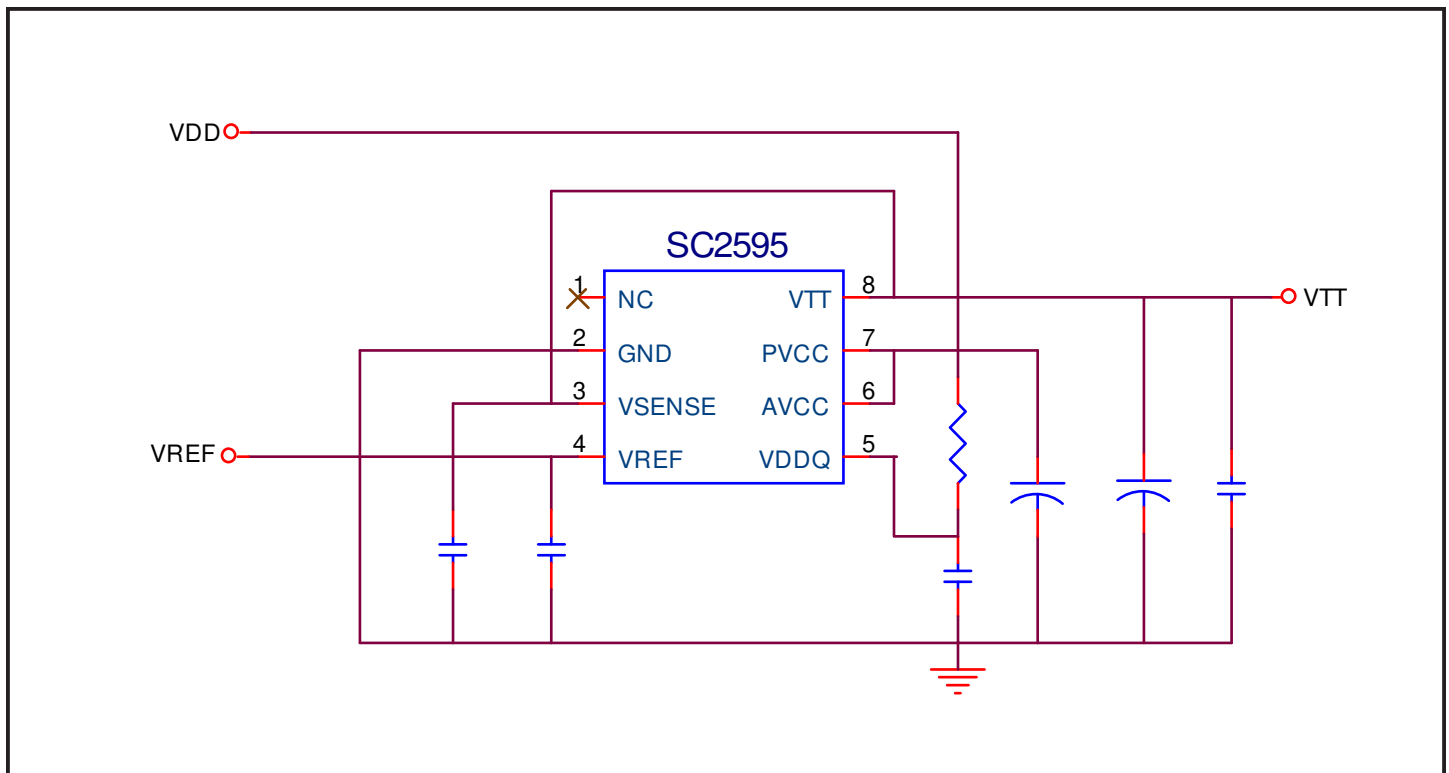
- ◆ Regulates while sourcing or sinking 1.5A
- ◆  $AV_{CC}$  range is from 2.5V to 5V
- ◆ Reference output
- ◆ Minimum number of external components
- ◆ Accurate internal voltage divider
- ◆ SOIC8-EDP package. Pb-free, Halogen free, and RoHS/WEEE compliant

### Applications

- ◆ DDR memory termination
- ◆ High speed data line termination
- ◆ PC motherboards
- ◆ Graphics boards
- ◆ Disk drives
- ◆ CD-ROM drives

**(Multiple patents pending.)**

### Typical Application Circuit



## POWER MANAGEMENT

### Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
PVCC, AVCC, VDDQ to GND	$V_{CC}$	-0.3 to +6.0	V
Thermal Resistance Junction to Case SOIC8-EDP	$\theta_{JC}$	5.5	°C/W
Thermal Resistance Junction to Ambient SOIC8-EDP	$\theta_{JA}$	36.5	°C/W
Operating Temperature Range	$T_A$	-40 to +105	°C
Operating Junction Temperature Range	$T_J$	-40 to +150	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Peak IR Reflow Temperature 10 - 40s	$T_{LEAD}$	240	°C
Peak IR Reflow Temperature 10 - 40s	$T_{LEAD}$	260	°C
ESD Rating (Human Body Model)	ESD	2	KV

### Operating Range

Parameter	Symbol	Maximum	Units
Junction Temperature Range	$T_J$	-40 to +150	°C
AVCC to GND	$AV_{CC}$	2.3 to 5.5	V
PVCC to GND	$PV_{CC}$	2.3 to $AV_{CC}$	V

### Electrical Characteristics

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$  and limits in boldface type apply over the full Operating Temperature Range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ). Unless otherwise specified,  $AV_{CC} = PV_{CC} = 2.5\text{V}$ ,  $V_{DDQ} = 2.5\text{V}$ .

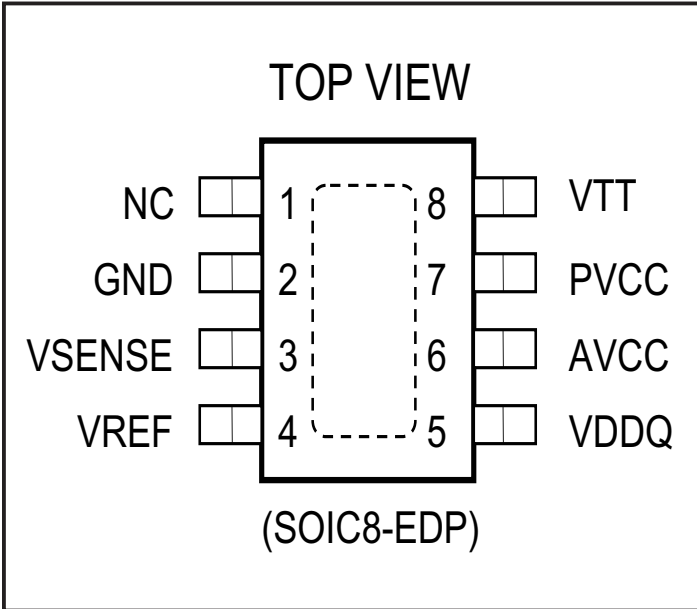
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Voltage	$V_{REF}$	$I_{REF\_OUT} = 0\text{mA}$	$V_{DDQ}/2$ - 40mV	1.25	$V_{DDQ}/2$ + 40mV	V
Load Regulation <sup>(1)</sup>	$REG_{LOAD}$	$I_{LOAD} : 0$ to $+1.5\text{A}$ $I_{LOAD} : 0$ to $-1.5\text{A}$		-0.5 +0.5		%
VTT Output Voltage Offset	$VOS_{VTT}$	$I_{OUT} = 0\text{A}$ , $V_{TT} - V_{REF}$	-20	0	+20	mV
Quiescent Current	$I_Q$	$I_{LOAD} = 0\text{A}$		400		$\mu\text{A}$
AVCC Enable Threshold				2.1		V
VDDQ Input Impedance	$Z_{VDDQ}$			100		$\text{k}\Omega$

**Note:**

(1) For Load Regulation, use a 10ms current pulse width when measuring  $V_{TT}$ .

**POWER MANAGEMENT**

**Pin Configuration**



**Ordering Information**

Part Number	Package	Temp. Range (T <sub>A</sub> )
SC2595STRT <sup>(1)(2)</sup>	SOIC8-EDP	-40 to +105°C
SC2595EVB	Evaluation Board	

**Notes:**

- (1) Only available in tape and reel packaging. A reel contains 2500 devices for SOIC8-EDP package.
- (2) Pb-free, Halogen free, and RoHS and WEEE compliant.

**POWER MANAGEMENT**
**Pin Descriptions**

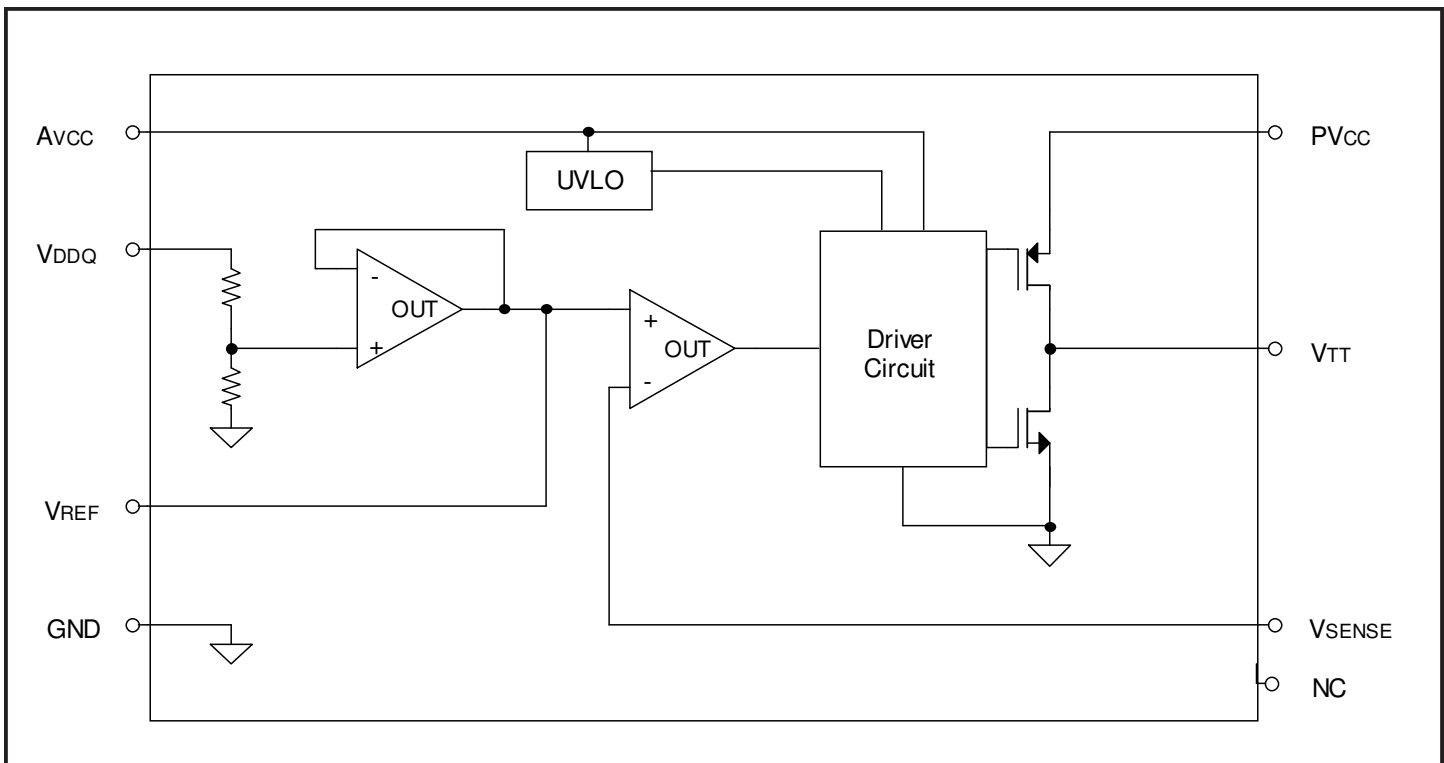
SOIC-8L EDP Pin #	Pin Name	Pin Function
1	NC	No internal connection. <sup>(1)</sup>
2	GND	Ground.
3	VSENSE	<p><math>V_{SENSE}</math> is a feedback pin. <math>V_{TT}</math> plane is always a narrow and long strip plane in most motherboard applications. This long strip plane will cause a large trace inductance and trace resistance. Consider the load transient condition; a fast load current going through <math>V_{TT}</math> strip plane can create voltage spikes on the <math>V_{TT}</math> plane. The load current can also cause a DC voltage drop on the <math>V_{TT}</math> plane. It is recommended that <math>V_{SENSE}</math> should be connected to the center of <math>V_{TT}</math> plane to improve the load regulation and the noise immunity. In case that one can't connect the <math>V_{SENSE}</math> pin to the center of the <math>V_{TT}</math> plane, one should connect it to the SC2595 <math>V_{TT}</math> pin directly. A longer trace of <math>V_{SENSE}</math> may pick up noise and cause the error of load regulation; hence the longer trace must be avoided.</p> <p>A 10nF to 100nF ceramic capacitor close to the <math>V_{SENSE}</math> pin is required to avoid oscillation during transient condition.</p>
4	VREF	<p><math>V_{REF}</math> is an output pin, which provides the buffered output of the internal reference voltage. System designer can use the <math>V_{REF}</math> output voltage for Northbridge chipset and memory. Because these input pins are typically high impedance, there should be a small amount of current drawn from the <math>V_{REF}</math> pin [figure 9, 10]. To improve the noise immunity, a ceramic capacitor (10nF - 100nF) should be added from the <math>V_{REF}</math> pin to ground with short distance.</p>
5	VDDQ <sup>(2)</sup>	<p>The <math>V_{DDQ}</math> pin is an input for creating internal reference voltage to regulate <math>V_{TT}</math>. The <math>V_{DDQ}</math> voltage is connected to internal 100Kohm resistor divider. The central tap of resistor divider (<math>V_{DDQ}/2</math>) is connected to the internal voltage buffer, which output is connected to <math>V_{REF}</math> pin and the non-inverting input of the error amplifier as the reference voltage. With the feedback loop closed, the <math>V_{TT}</math> output voltage will always track the <math>V_{DDQ}/2</math> precisely. It is recommended to use 5.1 ohm + a 1uF ceramic capacitor for <math>V_{DDQ}</math> pin's filter to increase the noise immunity.</p>
6	AVCC <sup>(2)</sup>	<p>The <math>AV_{CC}</math> pin is used to supply all of the internal control circuitry. <math>AV_{CC}</math> voltage has to be greater than its UVLO threshold voltage (2.1V typical) to allow the SC2595 be in normal operation. If <math>AV_{CC}</math> voltage is lower than the UVLO threshold voltage, the <math>V_{TT}</math> output voltage will remain at 0V.</p>
7	PVCC <sup>(2)</sup>	<p>The <math>PV_{CC}</math> pin provides the rail voltage from where the <math>V_{TT}</math> pin draws load current. There is a limitation between <math>AV_{CC}</math> and <math>PV_{CC}</math>. The <math>PV_{CC}</math> voltage must be less or equal to <math>AV_{CC}</math> voltage to ensure the correct output voltage regulation. The <math>V_{TT}</math> source current capability is dependent on <math>PV_{CC}</math> voltage. Higher the voltage on <math>PV_{CC}</math>, higher the source current; however, it will cause more power loss and higher temperature rise [figure 5, 11, 12].</p>
8	VTT	<p>The <math>V_{TT}</math> pin is the output of SC2595. It can sink and source 1.5A continuous current and 3A peak current while keeping excellent load regulation. It is recommended that one should use at least 220uF low ESR capacitors (ESR should be lower than 250m ohm) and 10uF ceramic capacitors, which are uniformly spread on the <math>V_{TT}</math> strip plane to reduce the voltage spike under load transient condition.</p>
	Thermal Pad	Thermal pad should be connected to GND.

**POWER MANAGEMENT**

**Notes:**

- (1) Can be used for vias.
- (2) Power up of  $AV_{CC}$ ,  $PV_{CC}$  and  $V_{DDQ}$  supplies.
  - (a) The preferred mode of operation is when the  $AV_{CC}$ ,  $PV_{CC}$  and  $V_{DDQ}$  pins are tied together to a single supply.
  - (b) If and when  $AV_{CC}$ ,  $PV_{CC}$  pins are tied to a supply separate to that of the  $V_{DDQ}$  supply pin; then the  $V_{DDQ}$  supply should lead  $AV_{CC}$ ,  $PV_{CC}$  supply or the  $V_{DDQ}$  supply and the  $AV_{CC}$ ,  $PV_{CC}$  supply should rise simultaneously.
  - (c) If the  $AV_{CC}$ ,  $PV_{CC}$  and  $V_{DDQ}$  supply pins are connected in a way such that,  $AV_{CC}$ ,  $PV_{CC}$  supplies precedes  $V_{DDQ}$  supply; then  $V_{TT}$  output precedes  $V_{DDQ}$ . This can cause the SDRAM device to latch-up, which may cause permanent damage to the SDRAM.

**Block Diagram**



**POWER MANAGEMENT**

**Application Information**

**Overview**

Double Data Rate (DDR) SDRAM was defined by JEDEC 1997. Its clock speed is the same as previous SDRAM but data transfers speed is twice than previous SDRAM. By now, the requirement voltage range is changed from 3.3V to 2.5V; the power dissipation is smaller than SDRAM. For above reasons, it is very popular and widely used in M/B, N/B, Video-cards, CD ROM drives, Disk drives.

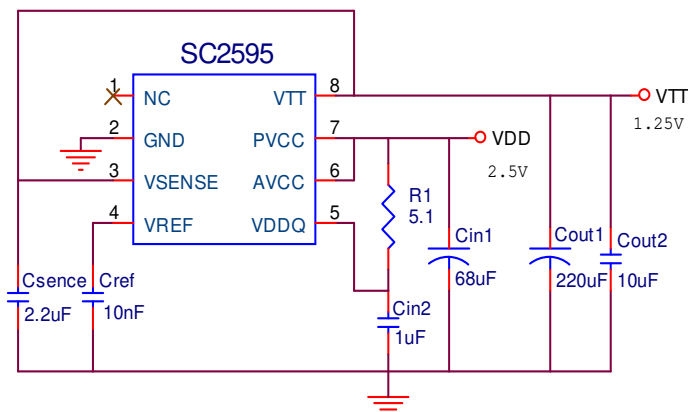
Regarding the DDR power management solution, there are two topologies can be selected for system designers. One is switching mode regulator that has bigger sink/source current capability, but the cost is higher and the board space needed is bigger. Another solution is linear mode regulator, which costs less, and needs the less board space. For two DIMM motherboards, system designers usually choose the linear mode for DDR power management solution.

**Typical Application Circuits & Waveforms**

Two different application circuits are shown below in Figure 1 to Figure 2. Each circuit is designed for specific condition. More details are described below. See Note 1. Below for recommended power up sequencing.

**Application\_1: Standard SSTL-2 Application**

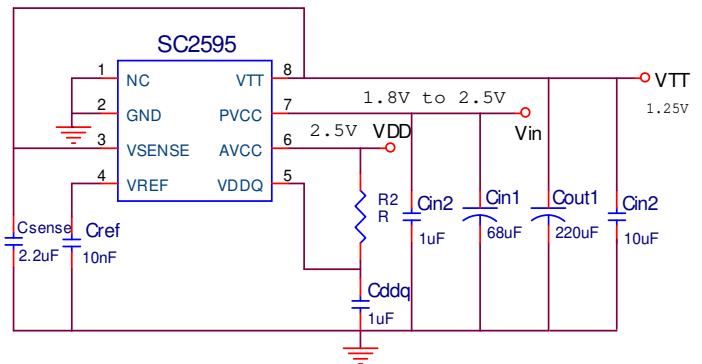
The AV<sub>CC</sub> pins, the PV<sub>CC</sub> pin, and the V<sub>DDQ</sub> pin can be tied together for SSTL-2 application. It only needs a 2.5V power rail for normal operation. System designer can save the PCB space and reduce the cost. Please refer to figures 3 to 4 for test waveforms.



**Figure 1: Standard SSTL-2 application**

**Application\_2: Lower Power Loss Configuration for SSTL-2**

If power loss is a major concern, separated the PV<sub>CC</sub> from the AV<sub>CC</sub> and the V<sub>DDQ</sub> will be a good choice. The PV<sub>CC</sub> can operate at lower voltage (1.8V to 2.5V). If 2.5V voltage is applied on AV<sub>CC</sub> and the V<sub>DDQ</sub>, but the source current is lower due to the lower operating voltage applied on the PV<sub>CC</sub>. Please find the relative test result in Figures 5, 11 and 12.



**Figure 2: Lower power loss for SSTL-2 application**

**Notes:**

- (1) Power up of AV<sub>CC</sub>, PV<sub>CC</sub> and V<sub>DDQ</sub> supplies.
  - (a) The preferred mode of operation is when the AV<sub>CC</sub>, PV<sub>CC</sub> and V<sub>DDQ</sub> pins are tied together to a single supply.
  - (b) If and when AV<sub>CC</sub>, PV<sub>CC</sub> pins are tied to a supply separate to that of the V<sub>DDQ</sub> supply pin; then the V<sub>DDQ</sub> supply should lead AV<sub>CC</sub>, PV<sub>CC</sub> supply or the V<sub>DDQ</sub> supply and the AV<sub>CC</sub>, PV<sub>CC</sub> supply should rise simultaneously.
  - (c) If the AV<sub>CC</sub>, PV<sub>CC</sub> and V<sub>DDQ</sub> supply pins are connected in a way such that, AV<sub>CC</sub>, PV<sub>CC</sub> supplies precedes V<sub>DDQ</sub> supply; then V<sub>TT</sub> output precedes V<sub>DDQ</sub>. This can cause the SDRAM device to latch-up, which may cause permanent damage to the SDRAM.

## POWER MANAGEMENT

### Application Information (Cont.)

#### Layout guidelines

1)The SC2595 has a SOIC8-EDP package. It can improve the thermal impedance ( $\theta_{JC}$ ) significantly. A suitable thermal pad should be added when PCB layout. Some thermal vias are required to connect the thermal pad to the PCB ground layer. This will improve the thermal performance .

2)To increase the noise immunity, a ceramic capacitor of 10nf to 100nf is required to decouple the  $V_{REF}$  pin with the shortest connection trace, also A 10nF to 100nF ceramic capacitor close to the  $V_{SENSE}$  pin is required to avoid oscillation during transient condition.

3)To reduce the noise on the input power rail for standard SSTL-2 application, a 68 $\mu$ F low ESR capacitor and a 1 $\mu$ F ceramic capacitor have to be used on the input power rail with shortest possible connection.

4)For lower power loss SSTL-2 application, a 220 $\mu$ F AL capacitor (ESR should be lower than 250m ohm) and a 10 $\mu$ F ceramic has to be added on the  $PV_{CC}$  pin and a 1 $\mu$ F ceramic capacitor +5.1 ohm filter has to be added on the  $V_{DDQ}$  pin with shortest possible connection.

5) $V_{TT}$  output copper plane should be as large as possible.

6) $V_{SENSE}$  trace should be as short as possible.

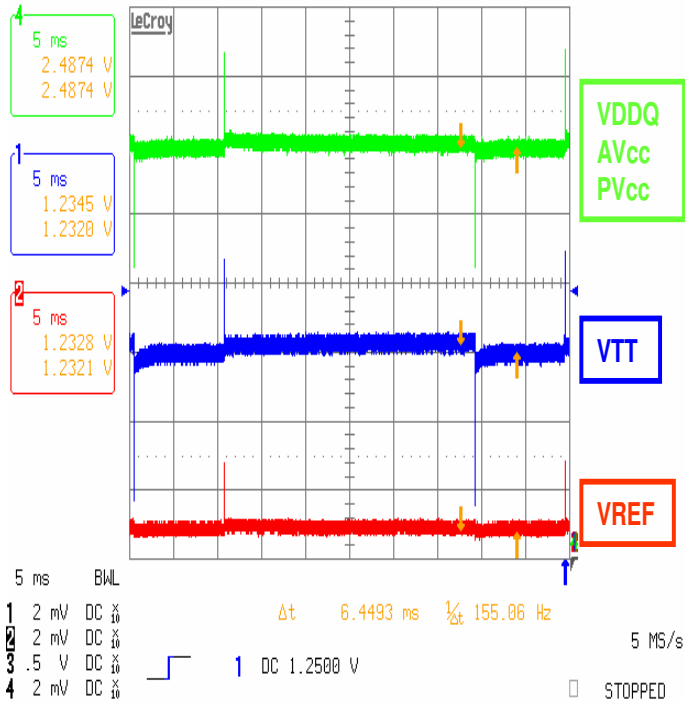


**POWER MANAGEMENT**

**Test Waveforms**

Test condition:  $Avcc=PVcc=VDDQ=2.5V, VTT=1.25V$   
 $Cout1=220\mu F, Cout2=10\mu F, Source\ 2A.$

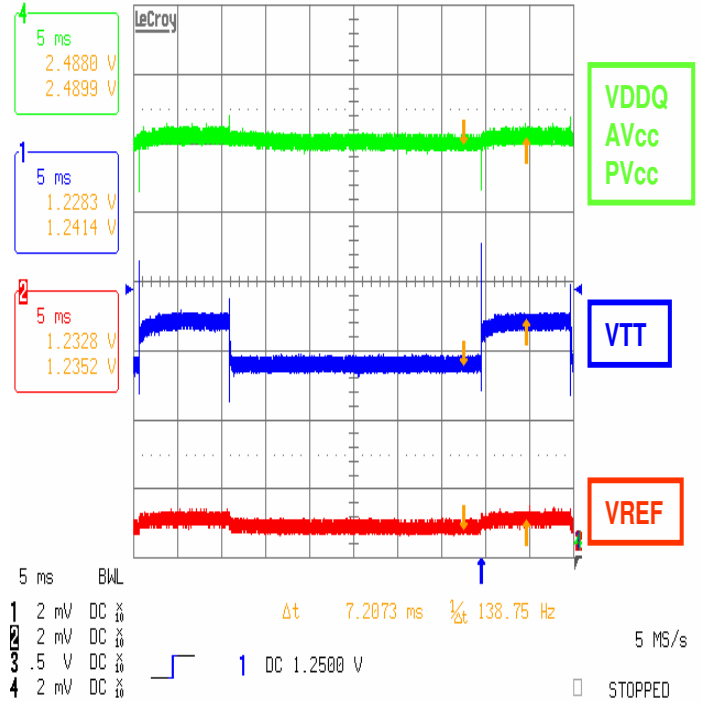
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**Figure 3**

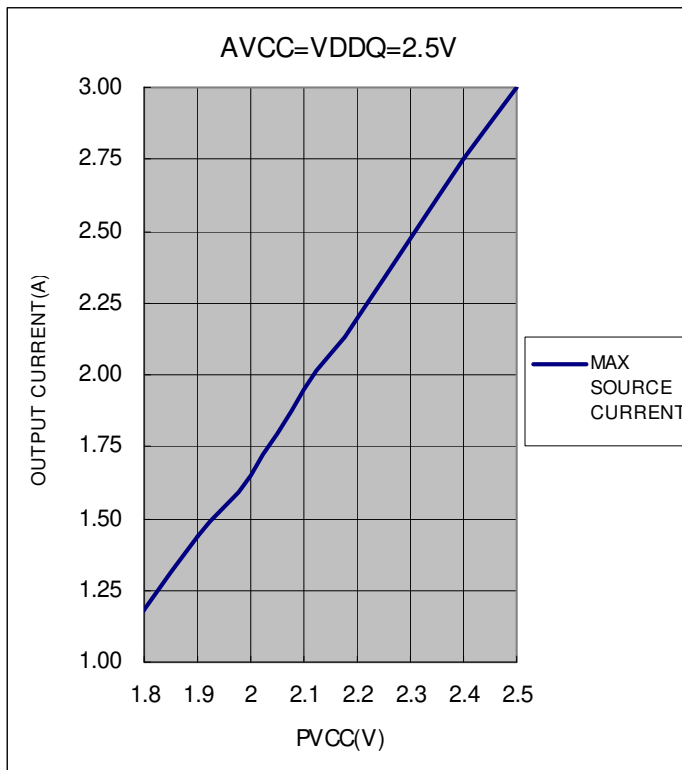
Test condition:  $Avcc=PVcc=VDDQ=2.5V, VTT=1.25V$   
 $Cout1=220\mu F, Cout2=10\mu F, Sink\ 2A.$

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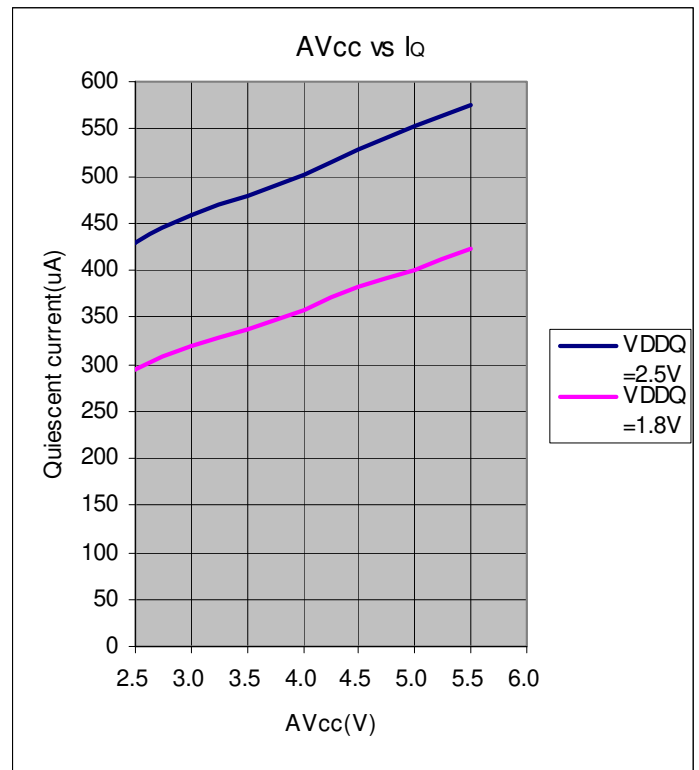


**Figure 4**

**Typical Characteristics**



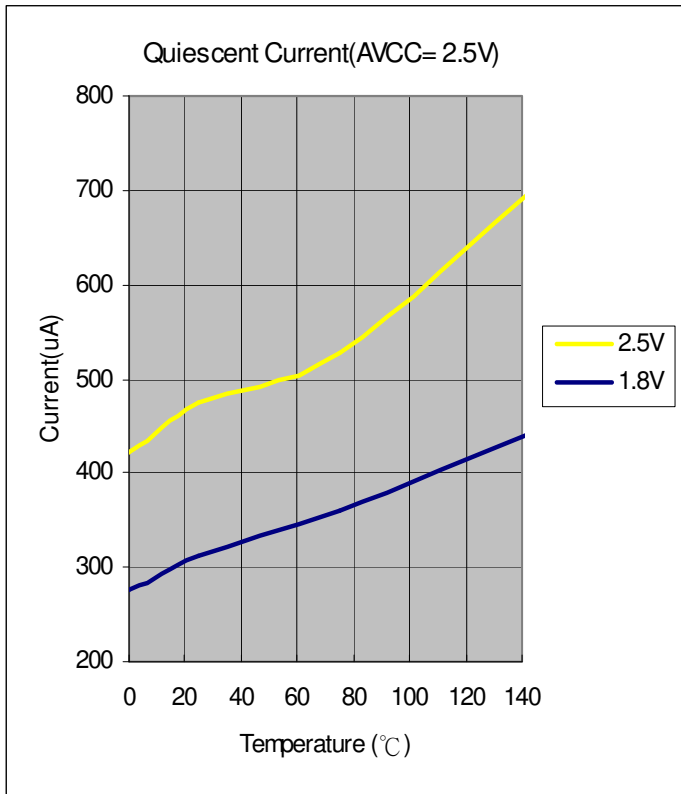
**Figure 5**



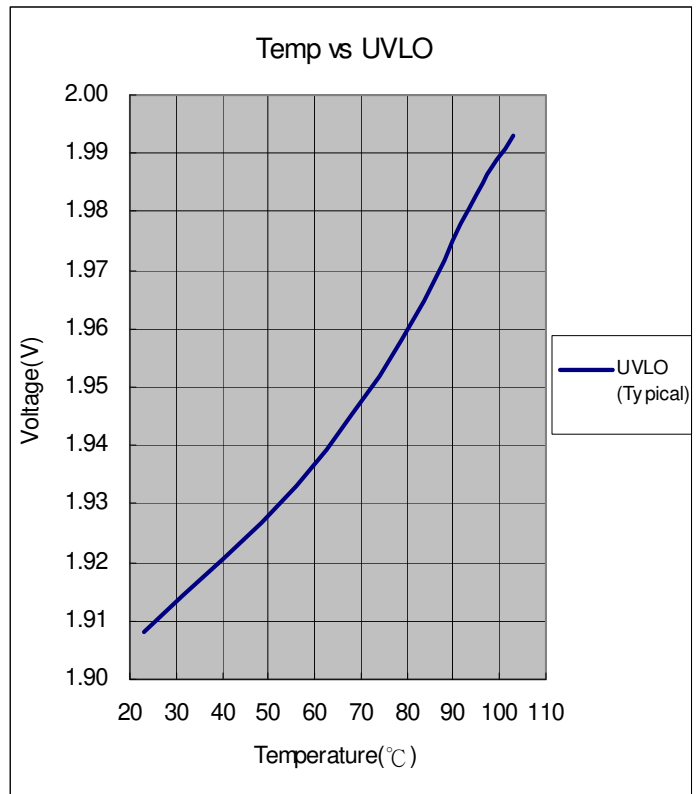
**Figure 6**

**POWER MANAGEMENT**

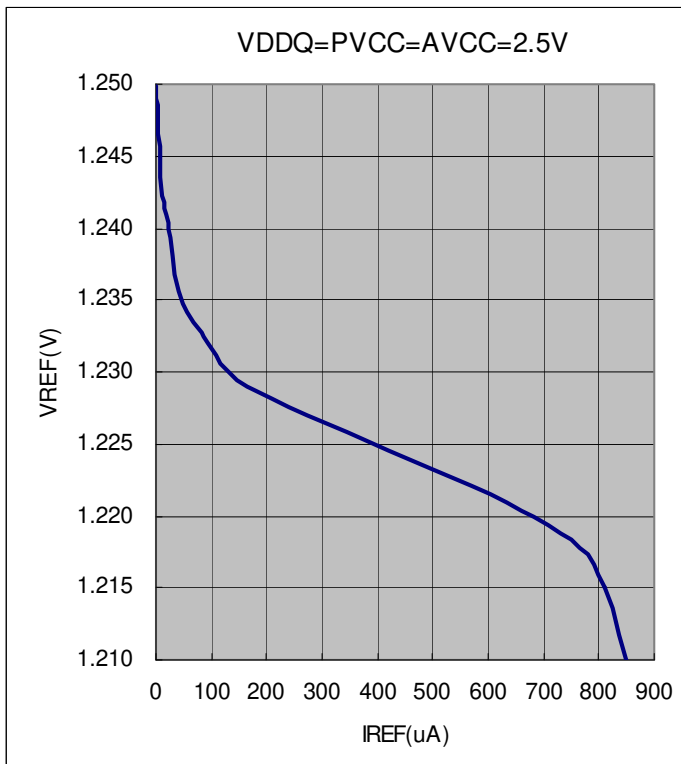
**Typical Characteristics (Cont.)**



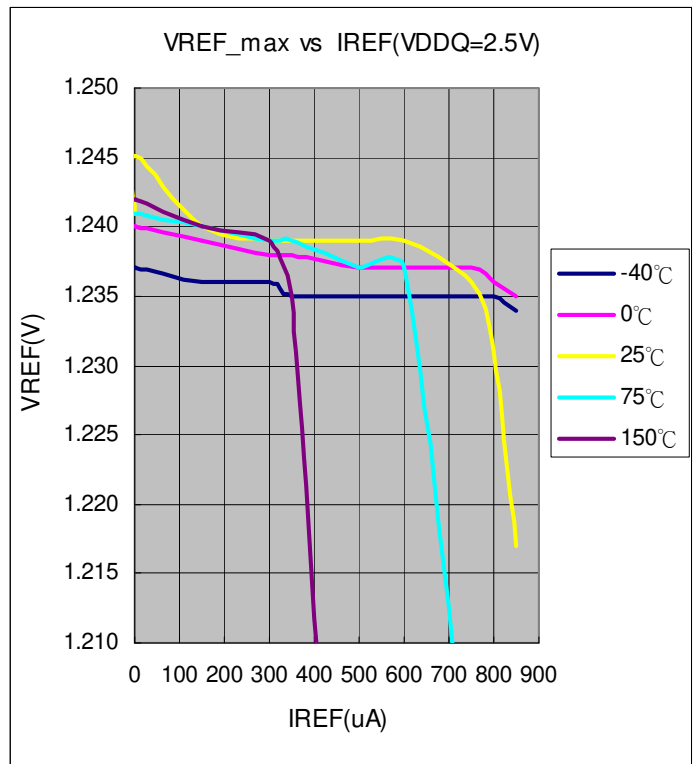
**Figure 7**



**Figure 8**



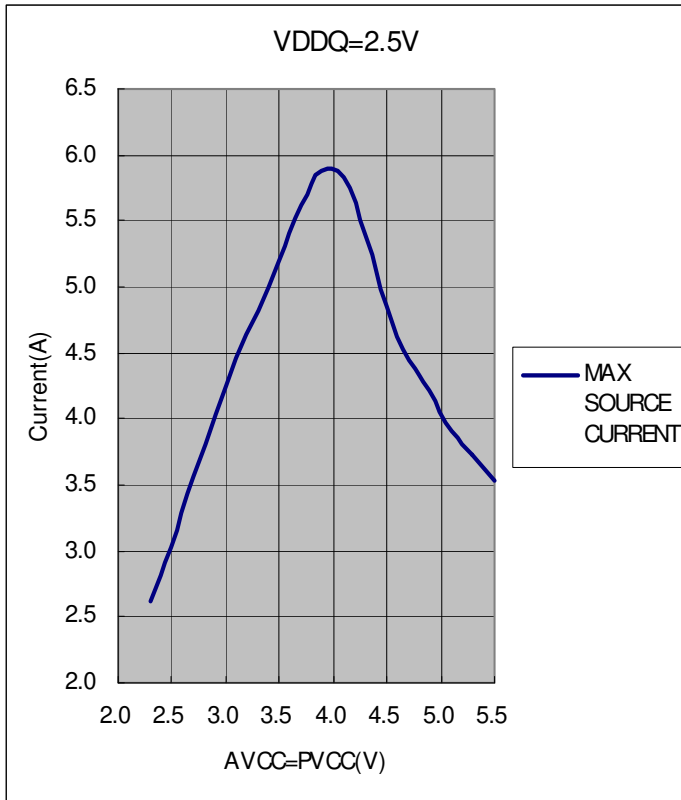
**Figure 9**



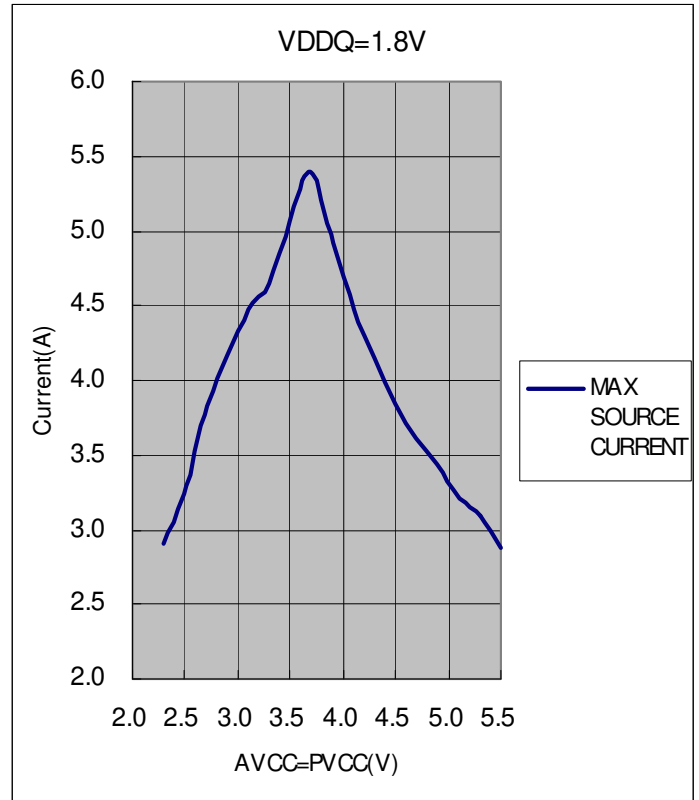
**Figure 10**

**POWER MANAGEMENT**

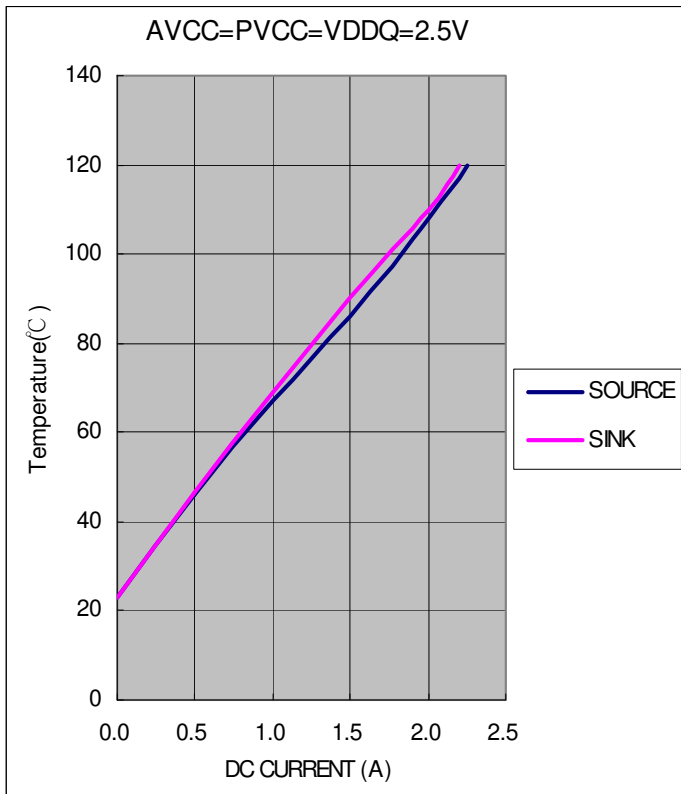
**Typical Characteristics (Cont.)**



**Figure 11**



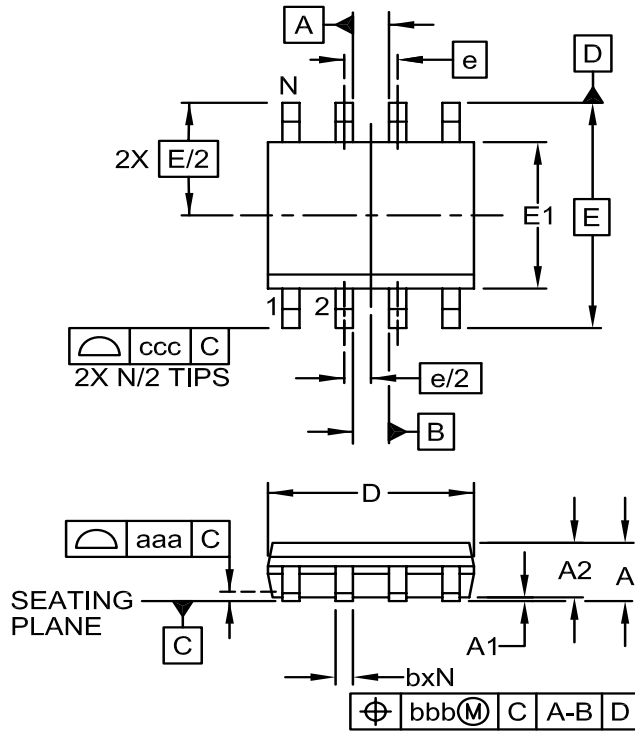
**Figure 12**



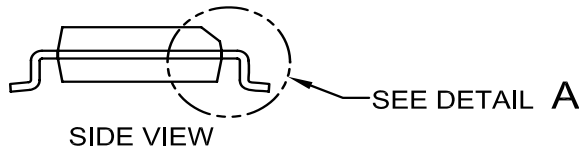
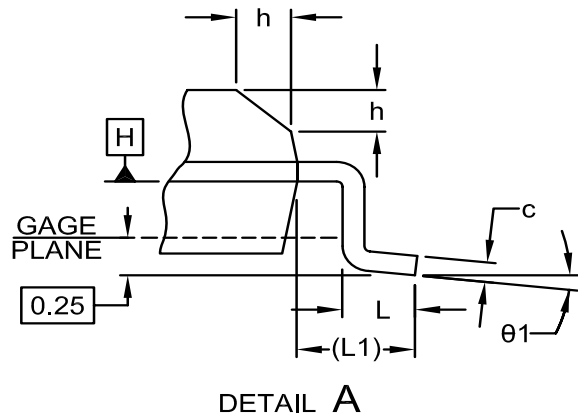
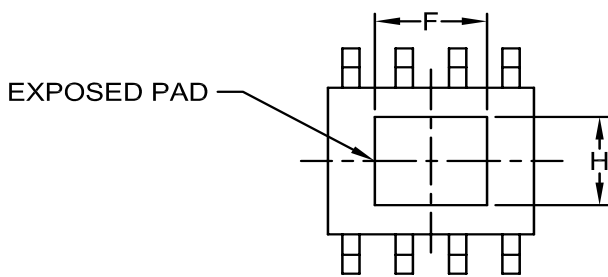
**Figure 13**

POWER MANAGEMENT

Outline Drawing - SOIC8-EDP



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.086	-	.130	2.19	-	3.30
H	.085	-	.099	2.15	-	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
theta1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

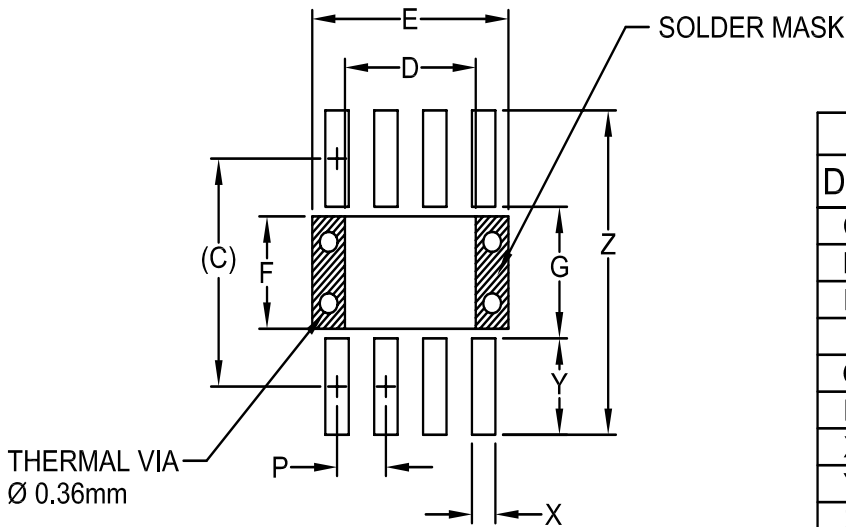


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

**POWER MANAGEMENT**

**Land Pattern - SOIC8-EDP**



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. REFERENCE IPC-SM-782A, RLP NO. 300A.
4. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

**Contact Information**

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 200 Flynn Road, Camarillo, CA 93012