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SC28L92

3.3 V/5.0 V Dual Universal Asynchronous Receiver/Transmitter (DUART)

Rev. 07 — 19 December 2007 Product data sheet

1. General description

The SC28L92 is a pin and function replacement for the SCC2692 and SC26C92 operating at 3.3 V or 5 V supply with added features and deeper FIFOs. Its configuration on power-up is that of the SC26C92. Its differences from the SCC2692 and SC26C92 are: 16 character receiver, 16 character transmit FIFOs, watchdog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (Neither the SC26C92 nor the SCC2692 is being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface. The bit 3 of the MR0A register allows the device to operate in an 8 byte FIFO mode if strict compliance with the SC26C92 FIFO structure is required.

The NXP Semiconductors SC28L92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system with modem and DMA interface.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of 28 fixed baud rates; a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided via RTS/CTS signaling to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC28L92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC28L92 is available in three package versions: PLCC44, QFP44, and HVQFN48.

2. Features

- Member of IMPACT family: 3.3 V to 5.0 V, −40 °C to +85 °C and 68xxx or 80xxx bus interface for all devices
- Dual full-duplex independent asynchronous receiver/transmitters
- 16 character FIFOs for each receiver and transmitter
- Pin programming selects 68xxx or 80xxx bus interface
- Programmable data format
  - 5 data to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1 stop, 1.5 stop or 2 stop bits programmable in $^1/_{16}$-bit increments
- 16-bit programmable counter/timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 28 fixed rates: 50 kBd to 230.4 kBd
  - Other baud rates to 1 MHz at 16×
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1× or 16× clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multi-drop mode (also called wake-up or 9-bit)
- Multi-function 7-bit input port (includes IACKN)
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically > 100 kΩ pull-up resistors
  - Change of state detectors for modem control
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
  - FIFO status for DMA interface
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed
  - Each FIFO can be programmed for four different interrupt levels
  - Watchdog timer for each receiver
- Maximum data transfer rates: 1× - 1 Mbit/s, 16× - 1 Mbit/s
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character

- On-chip crystal oscillator
- Power-down mode
- Receiver time-out mode
- Single 3.3 V or 5 V power supply
- Powers up to emulate SC26C92

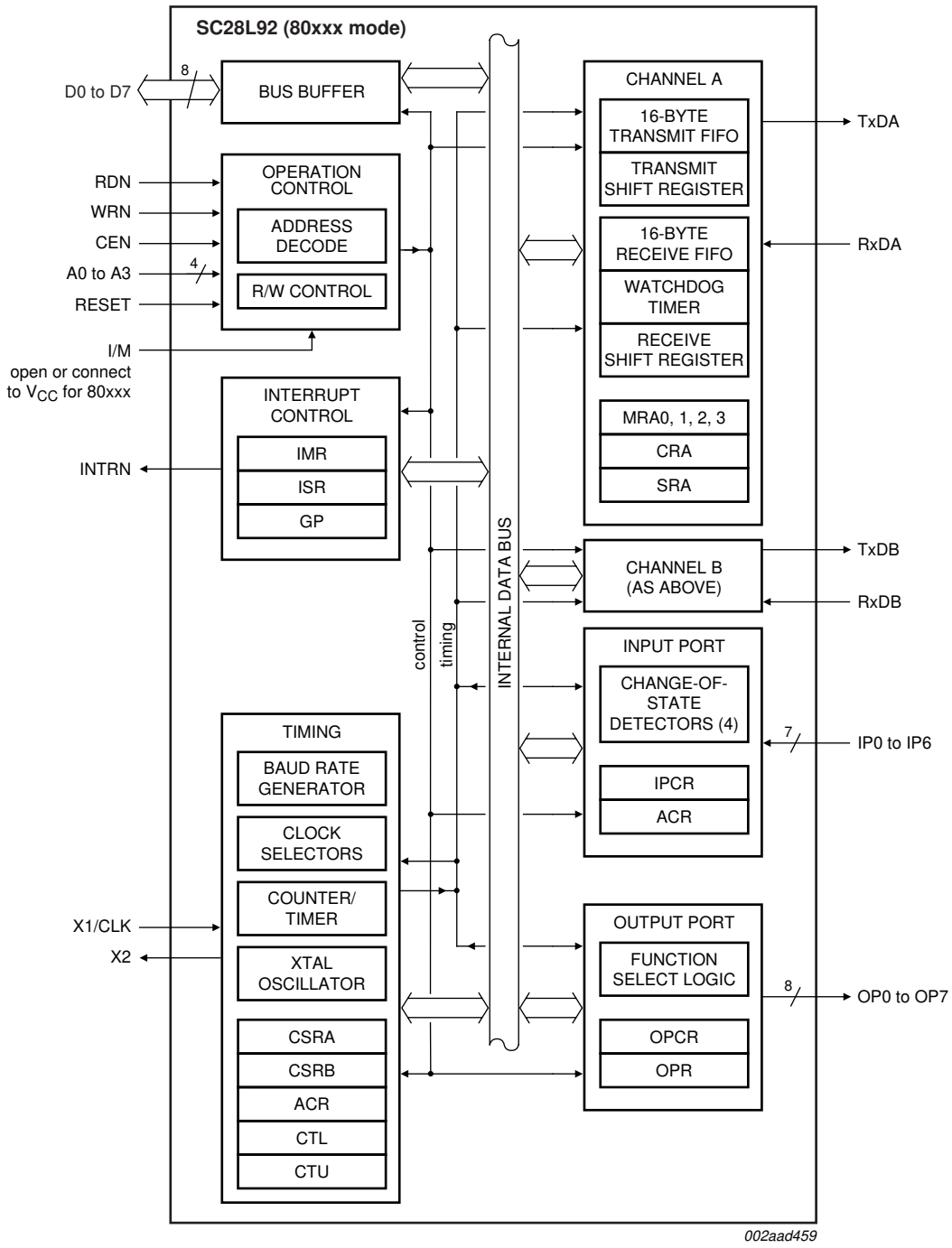
3. Ordering information

Table 1. Ordering information

V_{CC} = 3.3 V ± 10 % or V_{CC} = 5.0 V ± 10 %; T_{amb} = −40 °C to +85 °C

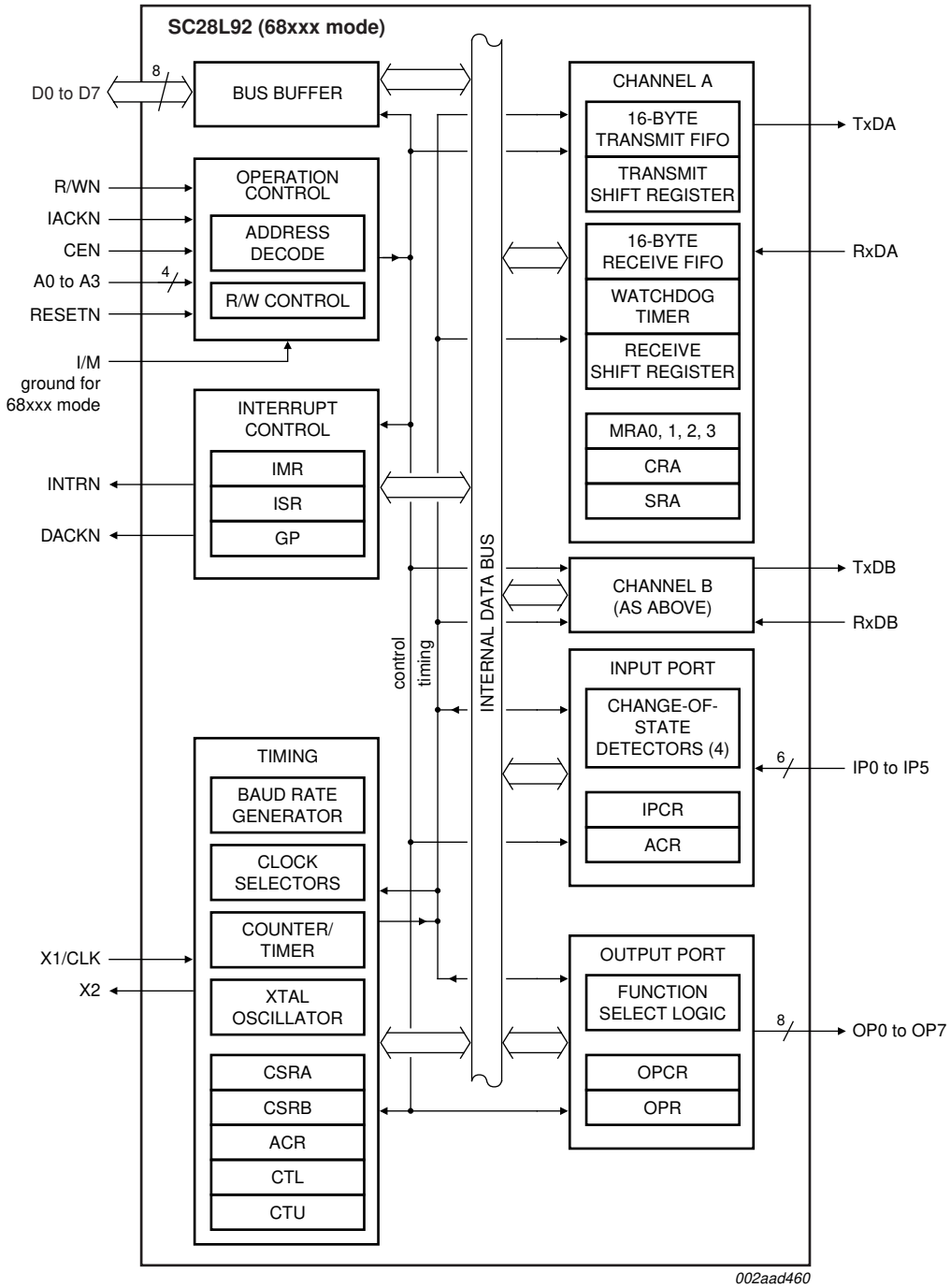
Type number	Package		
	Name	Description	Version
SC28L92A1A	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
SC28L92A1B	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
SC28L92A1BS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-4

4. Block diagram



The data pins TxD and RxD are considered idle at the logic 1 (HIGH) level when inactive, or active when at the logic 0 (LOW) level. Comments about these levels when RS232 is referenced often refer to Mark and Space levels. Mark usually means inactive and Space means active. The voltage levels represented by the terms Mark and Space are often reversed from those above: Mark is low voltage, and Space is high voltage.

Fig 1. Block diagram (80xxx mode)



The data pins TxD and RxD are considered idle at the logic 1 (HIGH) level when inactive, or active when at the logic 0 (LOW) level. Comments about these levels when RS232 is referenced often refer to Mark and Space levels. Mark usually means inactive and Space means active. The voltage levels represented by the terms Mark and Space are often reversed from those above: Mark is low voltage, and Space is high voltage.

Fig 2. Block diagram (68xxx mode)

5. Pinning information

5.1 Pinning

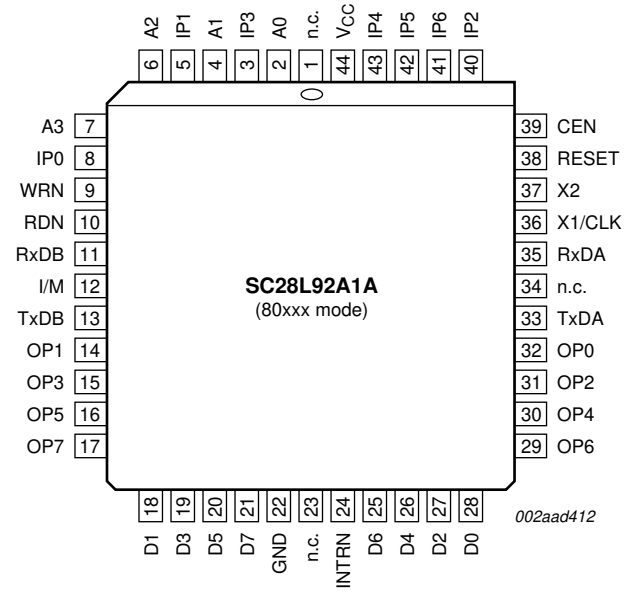


Fig 3. Pin configuration for PLCC44; 80xxx mode

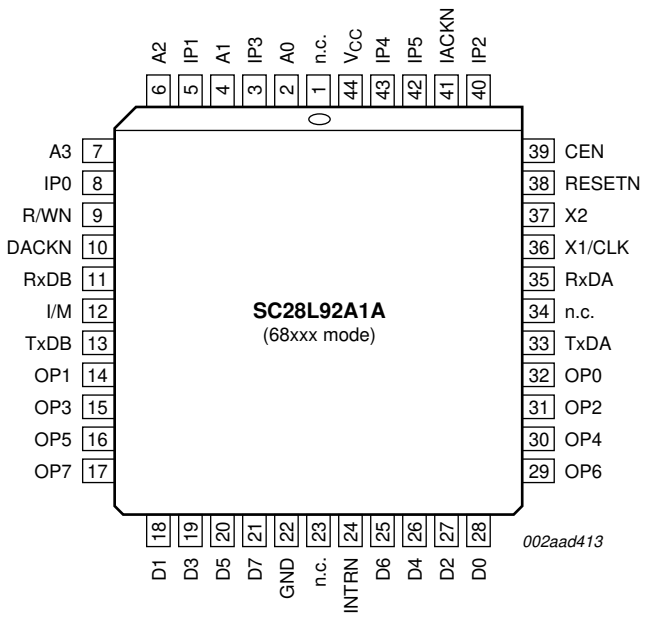


Fig 4. Pin configuration for PLCC44; 68xxx mode

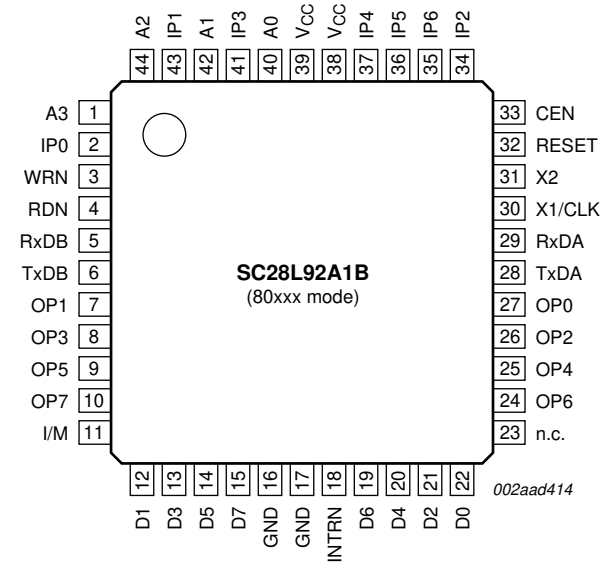


Fig 5. Pin configuration for QFP44; 80xxx mode

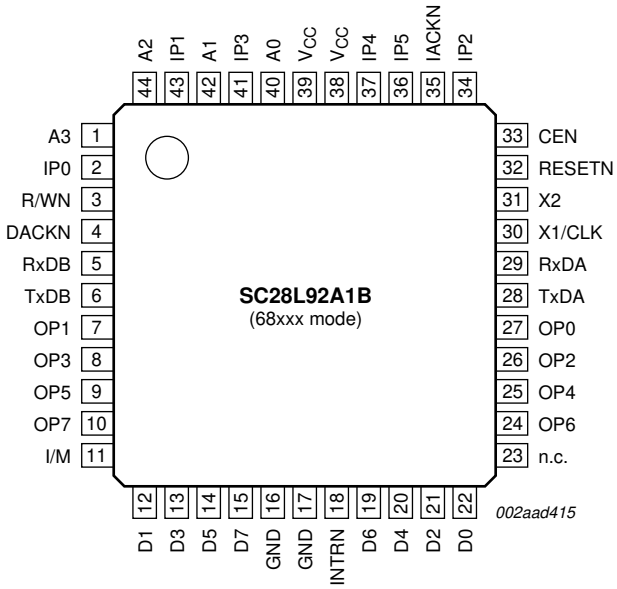


Fig 6. Pin configuration for QFP44; 68xxx mode

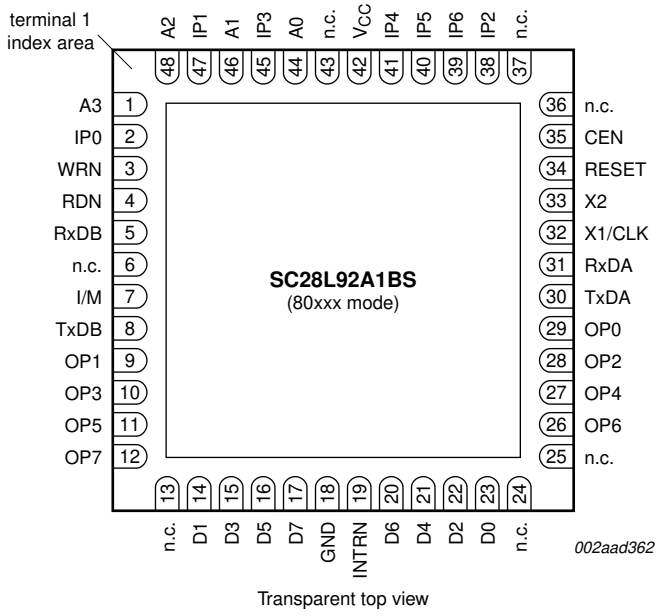


Fig 7. Pin configuration for HVQFN48; 80xxx mode

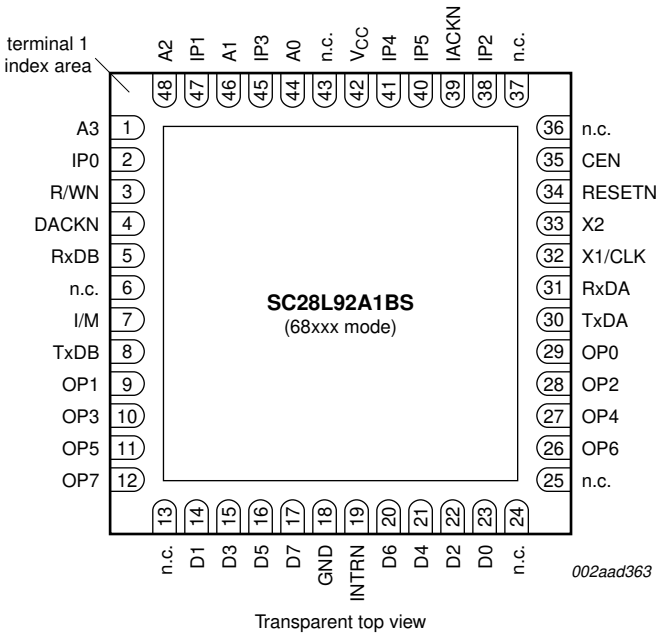


Fig 8. Pin configuration for HVQFN48; 68xxx mode

5.2 Pin description

Table 2. Pin description for 80xxx bus interface (Intel)

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
I/M	12	11	7	I	**Bus configuration**: When HIGH or not connected configures the bus interface to the conditions shown in this table.
D0	28	22	23	I/O	**Data bus**: Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
D1	18	12	14	I/O	
D2	27	21	22	I/O	
D3	19	13	15	I/O	
D4	26	20	21	I/O	
D5	20	14	16	I/O	
D6	25	19	20	I/O	
D7	21	15	17	I/O	
CEN	39	33	35	I	**Chip enable**: Active LOW input signal. When LOW, data transfers between the CPU and the DUART are enabled on D0 to D7 as controlled by the WRN, RDN and A0 to A3 inputs. When HIGH, places the D0 to D7 lines in the 3-state condition.
WRN	9	3	3	I	**Write strobe**: When LOW and CEN is also LOW, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	10	4	4	I	**Read strobe**: When LOW and CEN is also LOW, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0	2	40	44	I	**Address inputs**: Select the DUART internal registers and ports for read/write operations.
A1	4	42	46	I	
A2	6	44	48	I	
A3	7	1	1	I	
RESET	38	32	34	I	**Reset**: A HIGH level clears internal registers (SRA, SRB, IMR, ISR, OPR and OPCR), puts OP0 to OP7 in the HIGH state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (HIGH) state. Sets MR pointer to MR1. See Figure 10.
INTRN	24	18	19	O	**Interrupt request**: Active LOW, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pull-up device.
X1/CLK	36	30	32	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 17).
X2	37	31	33	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 17). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	35	29	31	I	**Channel A receiver serial data input**: The least significant bit is received first. See note on drive levels at block diagram (Figure 1).
RxDB	11	5	5	I	**Channel B receiver serial data input**: The least significant bit is received first. See note on drive levels at block diagram (Figure 1).

Table 2. Pin description for 80xxx bus interface (Intel) *...continued*

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
TxDA	33	28	30	O	**Channel A transmitter serial data output**: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle or when operating in local loopback mode. See note on drive levels at block diagram (Figure 1).
TxDB	13	6	8	O	**Channel B transmitter serial data output**: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle, or when operating in local loopback mode. See note on drive levels at block diagram (Figure 1).
OP0	32	27	29	O	**Output 0**: General purpose output or **channel** A request to send (RTSAN, active LOW). Can be deactivated automatically on receive or transmit.
OP1	14	7	9	O	**Output 1**: General-purpose output or channel B request to send (RTSBN, active LOW). Can be deactivated automatically on receive or transmit.
OP2	31	26	28	O	**Output 2**: General purpose output, or channel A transmitter 1× or 16× clock output, or channel A receiver 1× clock output.
OP3	15	8	10	O	**Output 3**: General purpose output or open-drain, active LOW counter/timer output or channel B transmitter 1× clock output, or channel B receiver 1× clock output.
OP4	30	25	27	O	**Output 4**: General purpose output or channel A open-drain, active LOW, RxA interrupt ISR[1] output.
OP5	16	9	11	O	**Output 5**: General-purpose output or channel B open-drain, active LOW, RxB interrupt ISR[5] output.
OP6	29	24	26	O	**Output 6**: General purpose output or channel A open-drain, active LOW, TxA interrupt ISR[0] output.
OP7	17	10	12	O	**Output 7**: General-purpose output, or channel B open-drain, active LOW, TxB interrupt ISR[4] output.
IP0	8	2	2	I	**Input 0**: General purpose input or channel A clear to send active LOW input (CTSAN).
IP1	5	43	47	I	**Input 1**: General purpose input or channel B clear to send active LOW input (CTSBN).
IP2	40	34	38	I	**Input 2**: General-purpose input or counter/timer external clock input.
IP3	3	41	45	I	**Input 3**: General purpose input or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	43	37	41	I	**Input 4**: General purpose input or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	42	36	40	I	**Input 5**: General purpose input or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	41	35	39	I	**Input 6**: General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	44	38, 39	42	Pwr	**Power Supply**: 3.3 V ± 10 % or 5 V ± 10 % supply input.

Table 2. Pin description for 80xxx bus interface (Intel) *…continued*

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
GND	22	16, 17	18[1]	Pwr	**Ground**
n.c.	1, 23, 34	23	6, 13, 24, 25, 36, 37, 43	Pwr	Not connected

[1] HVQFN48 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

Table 3. Pin description for 68xxx bus interface (Motorola)

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
I/M	12	11	7	I	**Bus configuration**: When LOW configures the bus interface to the conditions shown in this table.
D0	28	22	23	I/O	**Data bus**: Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
D1	18	12	14	I/O	
D2	27	21	22	I/O	
D3	19	13	15	I/O	
D4	26	20	21	I/O	
D5	20	14	16	I/O	
D6	25	19	20	I/O	
D7	21	15	17	I/O	
CEN	39	33	35	I	**Chip enable**: Active LOW input signal. When LOW, data transfers between the CPU and the DUART are enabled on D0 to D7 as controlled by the R/WN and A0 to A3 inputs. When HIGH, places the D0 to D7 lines in the 3-state condition.
R/WN	9	3	3	I	**Read/Write**: Input signal. When CEN is LOW, R/WN HIGH input indicates a read cycle; when LOW indicates a write cycle.
IACKN	41	35	39	I	**Interrupt acknowledge**: Active LOW input indicating an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	10	4	4	O	**Data transfer acknowledge**: A3-state active LOW output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0	2	40	44	I	**Address inputs**: Select the DUART internal registers and ports for read/write operations.
A1	4	42	46	I	
A2	6	44	48	I	
A3	7	1	1	I	
RESETN	38	32	34	I	**Reset**: A LOW level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0 to OP7 in the HIGH state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (HIGH) state. Sets MR pointer to MR1. See Figure 10.

Table 3. Pin description for 68xxx bus interface (Motorola) *...continued*

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
INTRN	24	18	19	O	**Interrupt request**: Active LOW, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pull-up.
X1/CLK	36	30	32	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 17).
X2	37	31	33	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 17). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	35	29	31	I	**Channel A receiver serial data input**: The least significant bit is received first. See note on drive levels at block diagram (Figure 2).
RxDB	11	5	5	I	**Channel B receiver serial data input**: The least significant bit is received first. See note on drive levels at block diagram (Figure 2).
TxDA	33	28	30	O	**Channel A transmitter serial data output**: The least significant bit is transmitted first. This output is held in the 'mark condition when the transmitter is disabled, idle or when operating in local loopback mode. See note on drive levels at block diagram (Figure 2).
TxDB	13	6	8	O	**Channel B transmitter serial data output**: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, idle, or when operating in local loopback mode. See note on drive levels at block diagram (Figure 2).
OP0	32	27	29	O	**Output 0**: General purpose output or channel A request to send (RTSAN, active LOW). Can be deactivated automatically on receive or transmit.
OP1	14	7	9	O	**Output 1**: General purpose output or channel B request to send (RTSBN, active LOW). Can be deactivated automatically on receive or transmit.
OP2	31	26	28	O	**Output 2**: General purpose output, or channel A transmitter 1× or 16× clock output, or channel A receiver 1× clock output.
OP3	15	8	10	O	**Output 3**: General purpose output or open-drain, active LOW counter/timer output or channel B transmitter 1× clock output, or channel B receiver 1× clock output.
OP4	30	25	27	O	**Output 4**: General purpose output or channel A open-drain, active LOW, RxA interrupt ISR [1] output.
OP5	16	9	11	O	**Output 5**: General purpose output or channel B open-drain, active LOW, RxB interrupt ISR[5] output.
OP6	29	24	26	O	**Output 6**: General purpose output or channel A open-drain, active LOW, TxA interrupt ISR[0] output.
OP7	17	10	12	O	**Output 7**: General purpose output, or channel B open-drain, active LOW, TxB interrupt ISR[4] output.
IP0	8	2	2	I	**Input 0**: General purpose input or channel A clear to send active LOW input (CTSAN).
IP1	5	43	47	I	**Input 1**: General purpose input or channel B clear to send active LOW input (CTSBN).
IP2	40	34	38	I	**Input 2**: General purpose input or counter/timer external clock input.

Table 3. Pin description for 68xxx bus interface (Motorola) *...continued*

Symbol	Pin			Type	Description
	PLCC44	QFP44	HVQFN48		
IP3	3	41	45	I	**Input 3**: General purpose input or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	43	37	41	I	**Input 4**: General purpose input or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	42	36	40	I	**Input 5**: General purpose input or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	44	38, 39	42	Pwr	**Power Supply**: 3.3 V ± 10 % or 5 V ± 10 % supply input.
GND	22	16, 17	18[1]	Pwr	**Ground**
n.c.	1, 23, 34	23	6, 13, 24, 25, 36, 37, 43	-	Not connected

[1] HVQFN48 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

6.1 Block diagram

The SC28L92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to Section 4 “Block diagram”.

6.1.1 Data bus buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

6.1.2 Operation control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus.

6.1.3 Interrupt control

A single active LOW interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3 to OP7 can be programmed to provide discrete interrupt outputs for the transmitter,

receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open-drain active LOW configuration. The OP pins may be used for DMA and modem control as well (see Section 7.4).

6.1.4 FIFO configuration

Each receiver and transmitter has a 16 byte FIFO. These FIFOs may be configured to operate at a fill capacity of either 8 bytes or 16 bytes. This feature may be used if it is desired to operate the SC28L92 in strict compliance with the SC26C92. The 8 byte or 16 byte mode is controlled by the MR0A[3] bit. A logic 0 value for this bit sets the 8-bit mode (the default); a logic 1 sets the 16 byte mode. MR0A bit 3 sets the FIFO size for both channels.

The FIFO fill interrupt level automatically follow the programming of the MR0A[3] bit. See Table 25 and Table 26.

6.1.5 68xxx mode

When the I/M pin is connected to GND (ground), the operation of the SC28L92 switches to the bus interface compatible with the Motorola bus interfaces. Several of the pins change their function as follows:

IP6 becomes IACKN input

RDN becomes DACKN

WRN becomes R/WN

The interrupt vector is enabled and the interrupt vector will be placed on the data bus when IACKN is asserted LOW. The interrupt vector register is located at address 0xC. The contents of this register are set to 0x0F on the application of RESETN.

The generation of DACKN uses two positive edges of the X1 clock as the DACKN delay from the falling edge of CEN. **If the CEN is withdrawn before two edges of the X1 clock occur, the generation of DACKN is terminated**. Systems not strictly requiring DACKN may use the 68xxx mode with the bus timing of the 80xxx mode greatly decreasing the bus cycle time.

6.2 Timing circuits

6.2.1 Crystal clock

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in Section 10 “Dynamic characteristics” must always be supplied to the DUART. If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 17. Nominal crystal rate is 3.6864 MHz. Rates up to 8 MHz may be used.

6.2.2 Baud rate generator

The baud rate generator operates from the oscillator or external clock input at the X1 input and is capable of generating 28 commonly used data communications baud rates ranging from 50 kBd to 38.4 kBd. Programming bit 0 of MR0 to a logic 1 gives additional baud rates of 57.6 kBd, 115.2 kBd and 230.4 kBd (500 kHz with X1 at 8.0 MHz). Note that the MR0A[2:0] control this change and that the change applies to both channels. MR0B[2:0] are reserved.

The baud rates are based on an input frequency of 3.6864 MHz. Changing the X1 frequency will change all baud rates by ratio of 3.6864 MHz to the new frequency. All rates generated by the BRG will be in the 16× mode. The clock outputs from the BRG are at 16× the actual baud rate.

The counter/timer can be used as a timer to produce a 16× clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal. The use of the counter/timer also requires the generation of a frequency 16× of the baud rate. See Section 6.2.3.

6.2.3 Counter/timer

The Counter/timer is a 16-bit programmable divider that operates in one of three modes: counter, timer and time-out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time-out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the OP pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from logic 1 to logic 0. A register read address (see Table 4) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D[7:0] is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR[3] bit in the interrupt status register.

6.2.4 Timer mode

In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from logic 1 to logic 0 (HIGH-to-LOW). This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command.

Note: Reading of the CTU and CTL registers in the timer mode is not meaningful. When the C/T is used to generate a baud rate and the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16× mode. Calculation for the number n to program the counter/timer upper and lower registers is shown in Equation 1. The value of the divisor n is

$$n = \frac{counter/timer\ input\ clock}{2 \times 16 \times (desired\ baud\ rate)} \quad (1)$$

Often this division will result in a non-integer number; 26.3 for example. One may only program integer numbers to a digital divider. Therefore 26 (0x1A) would be chosen. If 26.7 were the result of the division, then 27 (0x1B) would be chosen. This gives a baud rate error of 0.3/26.3 or 0.3/26.7 that yields a percentage error of 1.14 % or 1.12 % respectively, well within the ability of the asynchronous mode of operation. Higher input frequency to the counter reduces the error effect of the fractional division.

6.2.5 Counter mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect. Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

6.2.6 Time-out mode

The time-out mode uses the received data stream to control the counter. The time-out mode forces the C/T into the timer mode. Each time a received character is transferred from the shift register to the Rx FIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the Rx FIFO.

By programming the C/T such that it would time-out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. **Note**: This is very similar to the watchdog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the Rx FIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing 0xA to CRA or CRB will invoke the time-out mode for that channel. Writing 0xC to CRA or CRB will disable the time-out mode. Only one receiver should use this mode at a time. However, if both are on, the time-out occurs after both receivers have been inactive for the time-out period. The start of the C/T will be on the logic OR of the two receivers.

The time-out mode disables the regular start counter or stop counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the Rx FIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the Set Time-out Mode On command, CRx = 0xA, will also clear the counter ready bit and stop the counter until the next character is received. The counter/timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write

Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands in Section 7.3.3 “Command registers”.

6.2.7 Time-out mode caution

When operating in the special time-out mode, it is possible to generate what appears to be a false interrupt, i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, **before** the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been received, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the Counter Ready bit not set. If nothing else is interrupting, this read of the ISR will return a 0x00 character. This action may present the appearance of a spurious interrupt.

6.2.8 Communications channels A and B

Each communications channel of the SC28L92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (break received, framing and parity errors) are also FIFOed with each data character.

6.2.9 Input port

The inputs to this unlatched 7-bit (6-bit for 68xxx mode) port can be read by the CPU by performing a read operation at address 0xD. A HIGH input results in a logic 1 while a LOW input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic, modem and DMA.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A HIGH-to-LOW or LOW-to-HIGH transition of these inputs, lasting longer than 25 μs to 50 μs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

The input port change of state detection circuitry uses a 38.4 kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25 μs (this assumes that the clock input is 3.6864 MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25 μs if the transition occurs coincident with the first sample pulse. The 50 μs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25 μs later.

6.2.10 Output port

The output ports are controlled from six places: the OPCR, OPR, MR, Command, SOPR and ROPR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the set output port bits command and the reset output bits command. These commands are at 0xE and 0xF, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the set output port bits command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the reset output ports bits command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

These pins along with the IP pins and their change-of-state detectors are often used for modem and DMA control.

6.3 Operation

6.3.1 Transmitter

The SC28L92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC28L92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPT bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPT bit will be reset. The TxEMPT will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the Tx FIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the Tx FIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the Tx FIFO, the TxD output remains HIGH and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the Tx FIFO.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the Tx FIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the Tx FIFO when the transmitter is disabled.

When the transmitter is reset it stops sending data immediately.

The transmitter can be forced to send a break (a continuous LOW condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset.

If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be LOW in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be HIGH, the transmitter will delay the transmission of any following characters until the CTS has returned to the LOW state. CTS going HIGH during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be end of message. See description of bit MR2[5] in Table 30 “MR2A - Mode Register 2 channel A (address 0x0) bit description” for more detail. This feature may be used to automatically turn around a transceiver in simplex systems.

6.3.2 Receiver

The SC28L92 is conditioned to receive data when enabled through the command register. The receiver looks for a HIGH-to-LOW (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16× clock for 7 clocks to ½ clocks (16× clock mode) or at the next rising edge of the bit time clock (1× clock mode). If RxD is sampled HIGH, the start bit is invalid and the search for a valid start bit begins again. If RxD is still LOW, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the Rx FIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains LOW for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error and overrun error (if any) are strobed into the SR from the next byte to be read from the Rx FIFO. If a break condition is detected (RxD is LOW for the entire character including the stop bit), a character consisting of all zeros will be loaded into the Rx FIFO and the received break bit in the SR is set to 1. The RxD input must return to HIGH for two (2) clock edges of the X1 crystal clock for the receiver to recognize the end of the break condition and begin the search for a start bit.

This will usually require a HIGH time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.

6.3.3 Transmitter reset and disable

Note the difference between transmitter disable and reset. A transmitter reset stops transmitter action immediately, clears the transmitter FIFO and returns the idle state. A transmitter disable withdraws the transmitter interrupts but allows the transmitter to continue operation until all bytes in its FIFO and shift register have been transmitted including the final stop bits. It then returns to its idle state.

6.3.4 Receiver FIFO

The Rx FIFO consists of a First-In-First-Out (FIFO) stack with a capacity of 8 or 16 characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all 8 or 16 stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the Rx FIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see Section 6.3.5) are popped thus emptying a FIFO position for new data.

A disabled receiver with data in its FIFO may generate an interrupt (see Section 6.3.5). Its status bits remain active and its watchdog, if enabled, will continue to operate.

6.3.5 Receiver status bits

In addition to the data word, three status bits (parity error, framing error and received break) are also appended to each data character in the FIFO. The overrun error, MR1[5], is not FIFOed.

Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logic OR of the status for all characters coming to the top of the FIFO since the last reset error from the command register was issued. In either mode reading the SR does not affect the FIFO. The FIFO is popped only when the Rx FIFO is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be reasserted (set LOW) automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

6.3.6 Receiver reset and disable

Receiver disable stops the receiver immediately. Data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected.

A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and realign the FIFO read/write pointers.

6.3.7 Watchdog

A watchdog timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the Rx FIFO which have not been read. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the Rx FIFO or a read of the Rx FIFO is executed.

6.3.8 Receiver time-out mode

In addition to the watchdog timer described in Section 6.3.7, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time-out intervals.

The time-out mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the Rx FIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The time-out mode is enabled by writing the appropriate command to the command register. Writing 0xA to CRA or CRB will invoke the time-out mode for that channel. Writing 0xC to CRA or CRB will disable the time-out mode. The time-out mode should only be used by one channel at once, since it uses the C/T. If, however, the time-out mode is enabled from both receivers, the time-out will occur only when **both** receivers have stopped receiving data for the time-out period. CTU and CTL must be loaded with a value greater than the normal receive character period. The time-out mode disables the regular start counter or stop counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the Rx FIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the set time-out mode on command, CRx = 0xA, will also clear the counter ready bit and stop the counter until the next character is received.

6.3.9 Time-out mode caution

When operating in the special time-out mode, it is possible to generate what appears to be a false interrupt, i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, **before** the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been receiver, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the counter ready bit not set. If nothing else is interrupting, this read of the ISR will return a 0x00 character.

6.3.10 Multi-drop mode (9-bit or wake-up)

The DUART is equipped with a wake-up mode for multi-drop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to 11 for channels A and B, respectively. In this mode of operation, a master station transmits an address character followed by data characters for the addressed slave station. The slave stations, with receivers that are normally disabled, examine the received data stream and wake-up the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the Tx FIFO.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the Rx FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the Rx FIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

7. Programming

7.1 Register overview

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 4.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has three mode registers (MR0, MR1 and MR2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0x0 or 0x1 by MR control commands in the command register Miscellaneous Commands. Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0x0 or 0x1 via the miscellaneous commands of the command register. The pointer is set to 0x1 on reset for compatibility with previous Philips Semiconductors UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Section 7.2 for register bit overview. The reserved registers at addresses 0x2 and 0xA should never be read during normal operation since they are reserved for internal diagnostics.

Table 4. SC28L92 register addressing READ (RDN = 0), WRITE (WRN = 0)[1]

Binary address				Read operation (RDN = 0 and CEN = 0)	Write operation (WRN = 0 and CEN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Interrupt vector (68xxx mode)	Interrupt vector (68xxx mode)
1	1	0	0	Miscellaneous register (Intel mode), IVR Motorola mode	Miscellaneous register (Intel mode), IVR Motorola mode
1	1	0	1	Input Port Register (IPR)	Output Port Configuration Register (OPCR)
1	1	1	0	start counter command	Set Output Port Bits Command (SOPR)
1	1	1	1	stop counter command	Reset output Port Bits Command (ROPR)

[1] The three MR registers are accessed via the MR Pointer and Commands 0x1n and 0xBn (where n = represents receiver and transmitter enable bits).

Table 5. Registers for channels A and B

Register name	Channel A register	Channel B register	Access
Mode Register	MRnA	MRnB	R/W
Status Register	SRA	SRB	R only
Clock Select	CSRA	CSRB	W only

Table 5. Registers for channels A and B *...continued*

Register name	Channel A register	Channel B register	Access
Command Register	CRA	CRB	W only
Receiver FIFO	RxFIFOA	RxFIFOB	R only
Transmitter FIFO	TxFIFOA	TxFIFOB	W only

Table 6. Registers supporting both channels

Register name	Mnemonic	Access
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter/Timer Upper value	CTU	R
Counter/Timer Lower value	CTL	R
Counter/Timer Preset Upper	CTPU	W
Counter/Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port	SOPR	W
Reset Output Port	ROPR	W
Interrupt vector or GP register	IVR/GP	R/W

7.2 Condensed register bit formats

Table 7. MR0 - Mode Register 0

7	6	5	4	3	2	1	0
RxWATCHDOG	RxINT[2]	TxINT[1:0]		FIFOSIZE	BAUDRATE EXTENDED II	TEST2	BAUDRATE EXTENDED I

Table 8. MR1 - Mode Register 1

7	6	5	4	3	2	1	0
RxRTS control	RxINT[1]	ERRORMODE	PARITYMODE		PARITYTYPE	bits per character	

Table 9. MR2 - Mode Register 2

7	6	5	4	3	2	1	0
channel mode		RTSN Control Tx	CTSN Enable Tx	stop bit length			

Table 10. CSR - Clock Select Register

7	6	5	4	3	2	1	0
receiver clock select code				transmitter clock select code			

Table 11. CR - Command Register

7	6	5	4	3	2	1	0
channel command code				disable Tx	enable Tx	disable Rx	enable Rx

Table 12. SR - channel Status Register

7	6	5	4	3	2	1	0
received break	framing error	parity error	overrun error	TxEMT	TxRDY	RxFULL	RxRDY

Table 13. IMR - Interrupt Mask Register (enables interrupts)

7	6	5	4	3	2	1	0
change input port	change break B	RxRDYB	TxRDTYB	counter ready	change break A	RxRDYA	TxRDYA

Table 14. ISR - Interrupt Status Register

7	6	5	4	3	2	1	0
input port change	change break B	RxRDYB FFULLB	TxRDTYB	counter ready	change break A	RxRDYA FFULLA	TxRDYA

Table 15. CTPU - Counter/Timer Preset Register, Upper

7	6	5	4	3	2	1	0
8 MSB of the BRG timer divisor							

Table 16. CTPL - Counter/Timer Preset Register, Lower

7	6	5	4	3	2	1	0
8 LSB of the BRG timer divisor							

Table 17. ACR - Auxiliary Control Register and change of state control

7	6	5	4	3	2	1	0
BRG set select	counter/timer mode and clock source select (see Table 54 on page 44)			enable IP3 COS interrupt	enable IP2 COS interrupt	enable IP1 COS interrupt	enable IP0 COS interrupt

Table 18. IPCR - Input Port Change Register

7	6	5	4	3	2	1	0
delta IP3	delta IP2	delta IP1	delta IP0	state of IP3	state of IP2	state of IP1	state of IP0

Table 19. IPR - Input Port Register

7	6	5	4	3	2	1	0
state of IP7	state of IP6	state of IP5	state of IP4	state of IP3	state of IP2	state of IP1	state of IP0

Table 20. SOPR - Set Output Port bits Register (SOPR)

7	6	5	4	3	2	1	0
set OP7	set OP6	set OP5	set OP4	set OP3	set OP2	set OP1	set OP0