Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SC339
Ultra Low Output Voltage Linear FET Controller

POWER MANAGEMENT

Description

The SC339 is an ultra-low output voltage, linear power supply controller designed to simplify power management for notebook PCs. It is part of Semtech's Smart LDO™ family of products. The SC339 has a user adjustable output that can be set anywhere between 0.5V and 3.3V using two external resistors.

SC339 features include tight output voltage regulation (± 1% over 0°C to +85°C), enable control, open drain power good signal, under-voltage protection and soft-start. The enable pin allows the part to enter a very low power standby mode. Pulling it high enables the output. The power good pin is an open drain and asserts low when the voltage at the adjust pin is below 88% (typ) of nominal. If the voltage at the adjust pin is below 50% (typ) of nominal, the under-voltage protection circuitry will shut down the output. The SC339 is available in a tiny SOT-23 6-pin surface mount package.

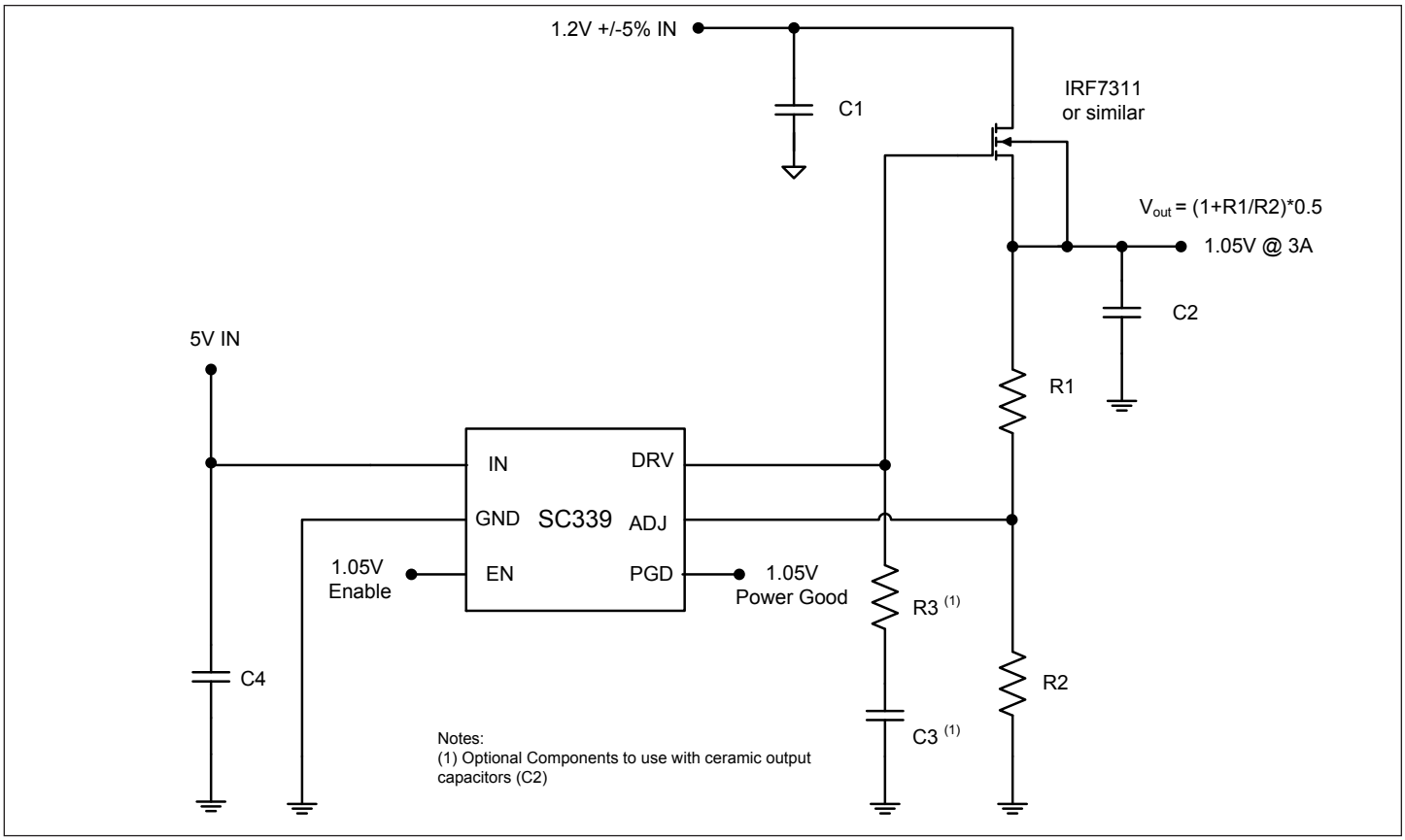
Features

- ± 1% Voltage Accuracy Over-Temperature
- Low Shutdown Current
- Runs Off 5V Supply
- Ultra-Fast Transient Response
- Enable Control for the Output
- Power Good Monitoring and Signaling for the Output
- Gate Drive from Input Supply Enables Use of N-Channel MOSFET
- User Selectable Dropout Voltage
- Under-Voltage Protection for the Output
- SOT-23 6-pin Surface Mount Package
- Compatible with Ceramic Capacitors
- Low Ripple Output
- Internal 1ms soft-start requires no external components
- Fully WEEE and RoHS compliant

Applications

- Notebook PCs
- Desktop Computers
- Battery Powered Devices
- Portable Instruments

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-0.3 to +6	V
Drive Pin	V_{DRV}	-0.3 to V_{IN} + 0.3V	V
Adjust and Power Good Pin	V_{ADJ}, V_{PGD}	-0.3 to V_{IN} + 0.3V	V
Enable Pin	V_{EN}	-0.3 to V_{IN} + 0.3V	V
Thermal Impedance Junction to Ambient	θ_{JA}	190	°C/W
Thermal Impedance Junction to Case	θ_{JC}	81	°C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IN} = V_{EN} = 5V ± 5%, V_{PWR} [(1)] = 1.5V ± 5%, 0A ≤ I_{OUT} ≤ 3A. Values in **bold** apply over full operating ambient temperature range.

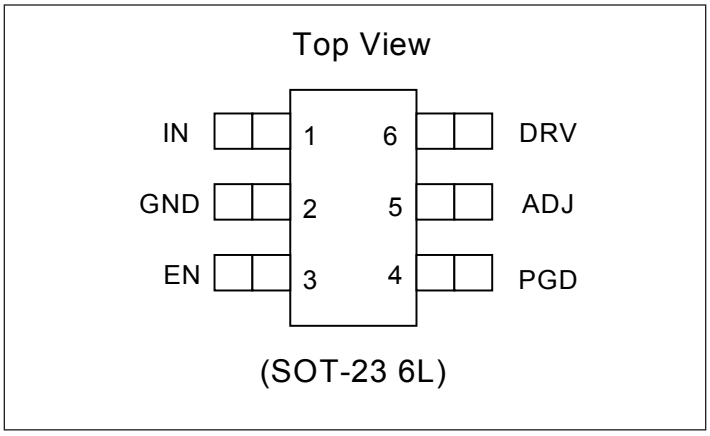
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{IN}		**4.5**	5	**5.5**	V
Quiescent Current	I_Q	V_{IN} = 5V		130	**200**	µA
Standby Current	$I_{Q(OFF)}$	EN low		0.1	**1.0**	µA
Input Under-Voltage Lockout						
Start Threshold	V_{UVLO}	V_{IN} rising		4.20		V
Hysteresis	V_{HYST}	V_{IN} falling		0.10		V
EN						
Enable Input Threshold	V_{IH}	Output on	**2.8**			V
	V_{IL}	Output off			1.8	
Enable Input Bias Current		V_{IN} = V_{EN} = 5V	**-1**		**+1**	µA

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ADJ						
Adjust Input Bias Current	I_{ADJ}	V_{ADJ} = 0.5V	**-100**	0	**+100**	nA
Reference Voltage	V_{ADJ}	0°C ≤ T_A ≤ +85°C	**-1%**	0.500	**1%**	V
DRV						
Output Current	I_{DRV}	Sourcing	**5**	20		mA
		Sinking	**5**	20		mA
Output Voltage	V_{DRV}	Full On, I_{DRV} = 0mA, V_{IN} = 5V	**4.70**	4.85		V
Output Under-Voltage Protection						
Trip Threshold(2)	$V_{TH(UV)}$	Measured at ADJ pin	**40**	50	**60**	%V_{ADJ}
PGD						
Power Good Threshold(3)	$V_{TH(PGD)}$	Measured at ADJ pin	**-15**	-12	**-8**	%V_{ADJ}
Output Logic Low Voltage	V_{PGD}	V_{ADJ} = 0.4V, I_{PGD} = -1mA			**0.4**	V
Power Good Leakage Current	I_{PGD}	V_{ADJ} = 0.5V, 0V ≤ V_{PGD} ≤ V_{IN}	**-1**	0	**+1**	µA
Soft-Start						
Output Rise Time 10% VOUT to 90% VOUT, VOUT = 1.05V	t_r	From EN rising to 99% of V_{OUT}	500	1000	2000	µs

Notes:
1) V_{PWR} = input voltage to pass device drain (or source depending upon orientation of FET).
2) If $V_{TH(UV)}$ is exceeded for longer than 1ms (nom.) the protection circuitry will shut down the output.
3) During start-up only, $V_{TH(PGD)}$ is -6% (typical), then switches to -12% (typical).

Pin Configuration

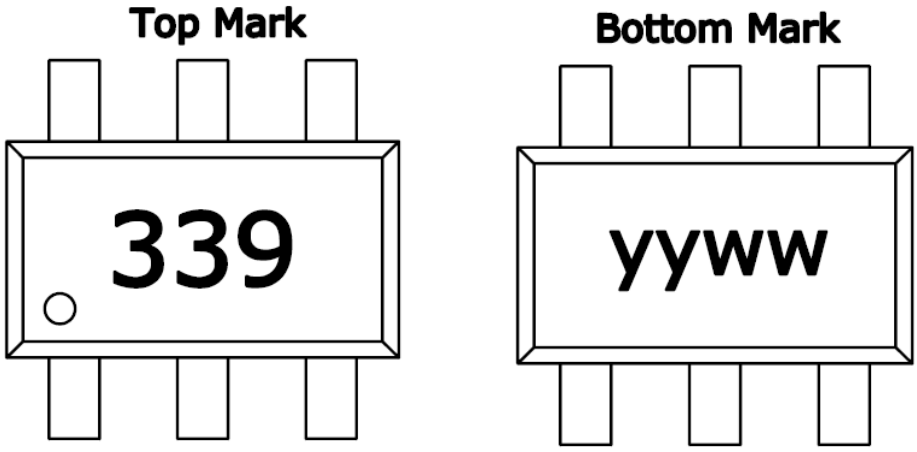


Ordering Information

Part Number	Package
SC339SKTRT	SOT-23 6 Pin
SC339EVB	Evaluation Board

Notes:
1) Only available in tape and reel packaging. A reel contains 3000 devices.
2) V_{IN} = 5V
3) V_{ADJ} is ± 1% over 0°C ≤ T_A ≤ +85°C.
4) Lead-free product. This product is fully WEEE and RoHS compliant.

Marking Information

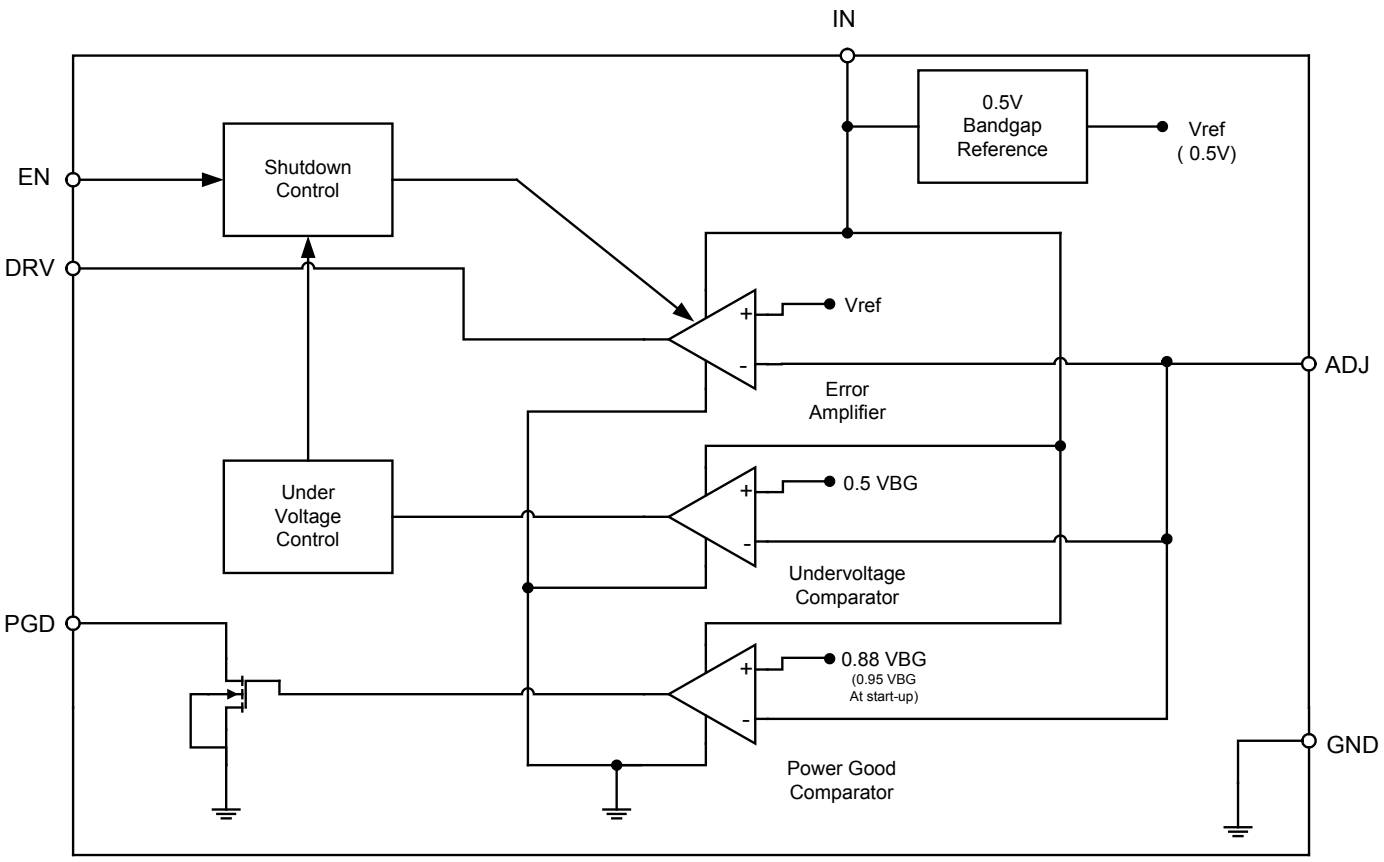


Marking for SOT23, 6 lead package:
yyww = Datecode (Example: E652)

Pin Descriptions

Pin	Pin Name	Pin Function
1	IN	5V supply
2	GND	Ground
3	EN	Active high enable control - connect to IN if not being used - do not allow to float
4	PGD	Power good signal output for V_{OUT}
5	ADJ	Regulator sense input - used for sensing the output voltage for power good and under-voltage and to set the output voltage
6	DRV	Output of regulator - drives the gate of an N-channel MOSFET to maintain V_{OUT} set by R1 and R2

Block Diagram



Applications Information

Theory Of Operation

The SC339 linear FET controller provides a simple way to drive an N-channel MOSFET to produce tightly regulated output voltages from an available, higher, supply voltage. It takes its power from the 5V system supply, drawing 130µA (typ) while operating.

It contains an internal bandgap reference which is compared to the output voltage via a resistor divider. The resistor divider is external and user selectable. The drive pin (DRV) can pull up to a guaranteed minimum of 4.7V. Thus, the device can be used to regulate a large range of output voltages by careful selection of the external MOSFETs (see Component Selection on this page).

The SC339 includes an active high enable control (EN). If this pin is pulled low, the drive pin is pulled low, turning off the N-channel MOSFET. If the pin is pulled up to 2.8V $\leq V_{EN} \leq V_{IN}$, the drive pin is enabled. This pin should not be allowed to float.

The SC339 has a power good output (PGD) which is an open drain output that pulls low if the related output is below the power good threshold (-12% of the programmed output voltage typical). The power good circuitry is active if the device is enabled, regardless of the state of the over-current latch.

An over-current protection circuit monitors the output voltage. If the output voltage drops below 50% (typical) of nominal, as would occur during an over-current or short condition, the device will pull the drive pin low and latch off. Toggle the power supply or enable pin to reset the latch condition.

Drive Output

The drive output is source and sink capable. The drivers both source and sink 20mA of current typically at 5V IN.

Soft-Start and Power Good Timing

At start-up, the internal reference is switched from its normal 0.5VDC to a 1ms (typical) linear ramp. The output voltage tracks the ramp until 0.5V is reached. The PWRGD signal is held low until the output has been in regulation approximately 500µsec to allow the output voltage to stabilize. The power-up is very smooth and monotonic.

OCP and Power Supply Sequencing

The SC339 has output under-voltage protection that looks at the output to see if it is: **a)** less than 50% (typical) of its nominal value and, **b)** V_{DRV} for that output is within 350mV (typical) of maximum. If both of these criteria are met, there is a 1ms (typical) delay and then the output is shut down. This provides inherent immunity to UV shutdown at start-up (which may occur while the output capacitors are being charged).

At start-up, it is necessary to ensure the power supplies and enable are sequenced correctly to avoid erroneous latch-off. For UV latch-off not to occur at start-up due to sequencing issues, the voltage supplied to the MOSFET drain should be greater than the output under-voltage threshold when that output is enabled. This assumes that the drop through the pass MOSFET is negligible. If not, then this drop needs to be taken into account also since:

$$V_{OUT} = V_{DRAIN} - (I_{OUT} \times R_{DS(ON)})$$

If the supply to the SC339 IN pin comes up before the supply to the MOSFET drain, then that output should be enabled after the supply to the MOSFET drain is applied - the power good signal for this rail would be ideal. If the power supply to the MOSFET drain comes up before the power supply to the SC339 IN pin, then the output can either be enabled with the supply to the IN pin or afterwards.

Please note the following example:

SC339 powered from 5V, the MOSFET (V_{DRAIN}) powered from 1.8V, set for $1.5V_{OUT}$. Worst-case: under-voltage threshold is 60% (over temperature) of 1.5V, or 0.9V. The typical enable threshold is ~2.4V, see Figure 1 on Page 7.

Component Selection

Output Capacitors: low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps are recommended for bulk capacitance, with ceramic bypass capacitors for decoupling high frequency transients. Ceramic output capacitors may be used; however, use of ceramic output capacitors requires compensation on the DRV output.

Applications Information (Cont.)

Input Capacitors: placement of low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps at the input to the MOSFET (V_{DRAIN}) will help to hold up the power supply during fast load changes, thus improving overall transient response. If V_{DRAIN} is located at the bulk capacitors for the upstream voltage regulator, additional capacitance may not be required. In this case a 0.1µF ceramic capacitor will suffice. The 5V bias supply to the SC339 should be bypassed with a 0.1µF ceramic capacitor.

MOSFETs: very low or low threshold N-channel MOSFETs are required. Select FETs rated for V_{GS} of 2.7V or lower. For the device to work under all operating conditions, a maximum $R_{DS(ON)}$ must be met to ensure that the output will never go into dropout:

$$R_{DSON(MAX)} = \frac{V_{IN(MIN)} - V_{OUT(MAX)}}{I_{OUT(MAX)}} \Omega$$

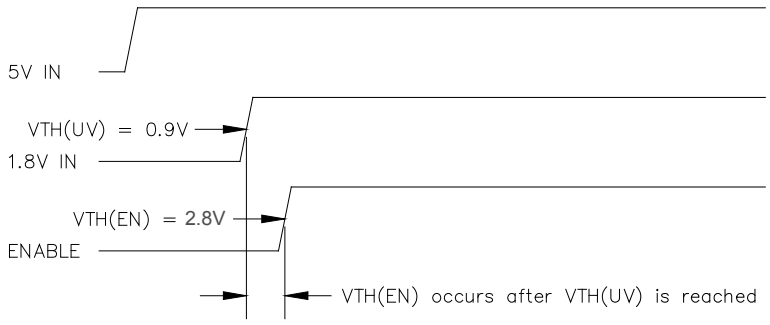
Note: $R_{DS(ON)}$ must be met at all temperatures and at the minimum V_{GS} condition.

Setting The Output Voltage: the adjust pin connects directly to the inverting input of the error amplifier, and the output voltage is set using external resistors (please refer to the Typical Application Circuit on Page 1).

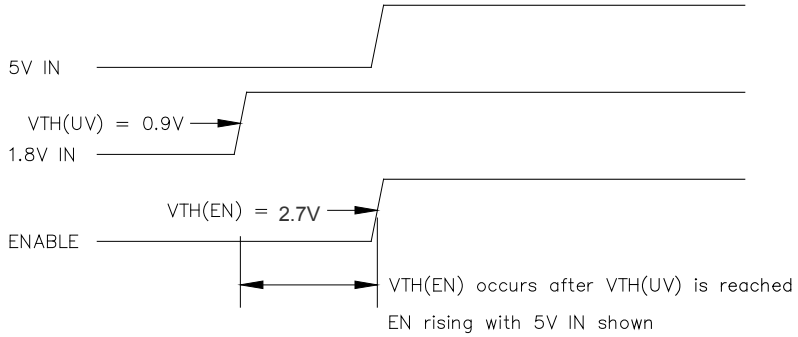
Using output 1 as an example, the output voltage can be calculated as follows:

$$V_{OUT} = 0.5 \bullet \left(1 + \frac{R1}{R2} \right)$$

The input bias current for the adjust pin is so low that it can be safely ignored. To avoid picking up noise, it is recommended that the total resistance of the feedback chain be less than 100kΩ. With ceramic capacitors, a recommended divider current of >100µA is recommended to keep the FET conducting during light load conditions to improve transient response.



SC339 Supply Comes Up Before MOSFET Drain Supply



MOSFET Drain Supply Comes Up Before SC339 Supply

Power Supply Sequencing

Applications Information (Cont.)

Table 1 lists recommended resistor values for some standard output voltages. All resistors are 1%, 1/10W.

The maximum output voltage that can be obtained from each output is determined by the input supply voltage and the $R_{DS(ON)}$ and gate threshold voltage of the external MOSFET. Assuming that the MOSFET gate threshold voltage is sufficiently low for the output voltage chosen and the worst-case drive voltage, $V_{OUT(MAX)}$ is given by:

$$V_{OUT\ (MAX)} = V_{DRAIN(MIN)} - I_{OUT(MAX)} \bullet R_{DSON(MAX)}$$

V_{OUT} (V)	R1 or R3 (kΩ)	R2 or R4 (kΩ)
1.05	11.0	10.0
1.2	14.0	10.0
1.5	20.0	10.0
2.5	45.3	11.3
3.3	63.4	11.3

Recommended Resistor Values For SC339

Design Example

Goal: 1.05V±5% @ up to 2.5A from 1.2V±5% and 5V±5%

Solution 1: No Passive Droop

Total window for DC error, ripple and transient is ±52.5mV.

Since this device is linear and assuming that it has been designed to not ever enter dropout, there is negligible ripple on the output.

The DC error for this output is the sum of:

V_{ADJ} accuracy = ±1% = ±10.5mV

Feedback chain tolerance = ±1% = ±10.5mV

Load regulation = ±0.25% = ±2.6mV

Resistors per Table 1 should be 11.0kΩ (top) and 10.0kΩ (bottom).

Total DC error = ±2.25% = 23.6mV

This leaves ±2.75% = 28.875mV for the load transient ESR spike, therefore:

$$R_{ESR(MAX)} = \frac{28.875mV}{2.5A} = 11.55m\Omega$$

Bulk capacitance required is given by:

$$C_{BULK(MIN)} = \frac{dI \bullet \tau}{dV} = \mu F$$

Where dI is the maximum load current step, t is the maximum regulator response time and dV is the allowable voltage droop. Therefore with dI = 2.5A, t = 1µs, and dV = 28.875mV:

$$C_{BULK(MIN)} = \frac{2.5 \bullet 1 \bullet 10^{-6}}{28.875 \bullet 10^{-3}} = 87\mu F$$

So if we use 1% V_{OUT} set resistors we would select 100µF, 12mΩ POSCAP for output capacitance (which assumes that local ceramic bypass capacitors will absorb the balance of the (12 - 11.55)mΩ ESR requirement - otherwise 10mΩ capacitors should be used).
If we use 0.1% set resistors, then the total DC error becomes ±1.35% = ±15.75mV, leaving ±3.65% = 38.33mV for the ESR spike. In this case:

$$R_{ESR(MAX)} = \frac{38.33mV}{2.5A} = 15.33m\Omega \quad \text{and,}$$

$$C_{BULK(MIN)} = \frac{2.5 \bullet 1 \bullet 10^{-6}}{38.33 \bullet 10^{-3}} = 65\mu F$$

So for 0.1% resistors we could use 1 x 100µF, 15mΩ POSCAP for output capacitance.

Applications Information (Cont.)

This is a very severe example, since the output voltage is so low, therefore the allowable window is very small. See Solution 2 for an alternate circuit. For higher output voltages the components required will be less stringent.

The input capacitance needs to be large enough to stop the input supply from collapsing below -5% (i.e., the design minimum) during output load steps. If the input to the pass MOSFET is not local to the supply bulk capacitance then additional bulk capacitance may be required.

MOSFET selection: since the input voltage to the SC339 is 5V±5%, the minimum available gate drive is:

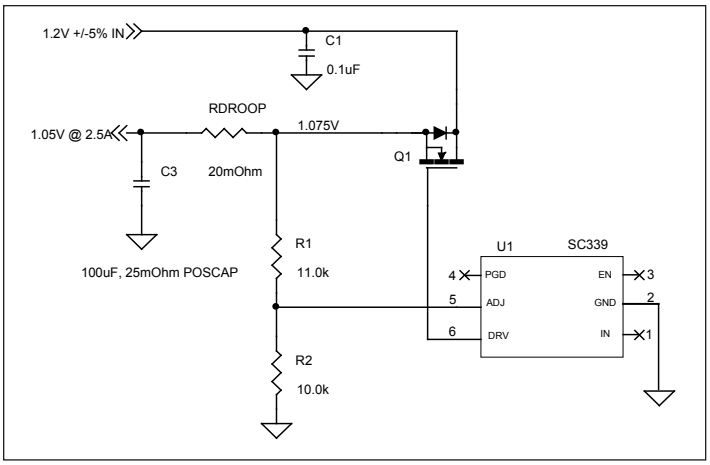
$$V_{GS} = (4.4 - 1.1025) = 3.3V$$

So a MOSFET rated for V_{GS} = 2.7V will be required, with an $R_{DS(ON)(MAX)}$ (over-temperature) given by:

$$R_{DSON(MAX)} = \frac{(V_{IN(MIN)} - V_{OUT})}{I_{OUT(MAX)}} = \frac{(1.14 - 1.05)}{2.5} = 36m\Omega$$

MOSFET SELECTION			
SO-8 Footprint			
	Vgs	Rds-on	Imax
FDS6682	1.7V	9mΩ	14A
IRF7456	1.5V	6.5mΩ	16A
1206 Footprint			
	Vgs	Rds-on	Imax
Si5406DC	0.6V	20mΩ	9.5A
NTHS5404	0.6V	25mΩ	7.2A
SOT-23 Footprint			
	Vgs	Rds-on	Imax
IRLMS2002	1V	30mΩ	5.2A
FDN337N (when Input is > 1.2V for 1.05V output)	0.7V	65mΩ	2.2A

Solution 2: Using Passive Droop



Passive droop allows us to use almost the full output tolerance window for transients, therefore making the output capacitor selection simpler and less expensive. The trade-offs are the cost of the droop resistor versus the reduction in output capacitor cost, and the reduction in headroom which impacts MOSFET selection. The top of the feedback chain connects to the input side of R_{DROOP}, and the output is set for 1.075V. Thus at no load, V_{OUT} will be 1.075V (or 1.05V + 2.4%) and at I_{OUT} = 2.5A, V_{OUT} will be 1.025V (or 1.05V - 2.4%).

If 1% set resistors are used, the total DC error will be ±2.25% = 24mV. Thus, at no load, the minimum output voltage will be given by:

$$V_{OUT(MIN\_NO\_LOAD)} = 1.075 - 0.024 = 1.051V$$

This leaves 53.5mV for transient response, giving:

$$R_{ESR(MAX)} = \frac{53.5mV}{2.5A} = 21.4m\Omega \quad \text{and,}$$

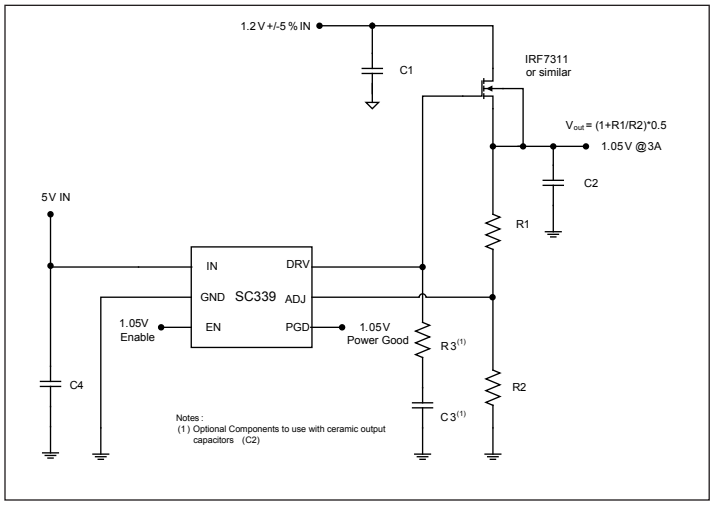
$$C_{BULK(MIN)} = \frac{2.5 \cdot 1 \cdot 10^{-6}}{53.5 \cdot 10^{-3}} = 47\mu F$$

Instead of 2 x 100µF, 12mΩ capacitors, we can use 1 x 47µF, 15mΩ capacitor.

Applications Information (Cont.)

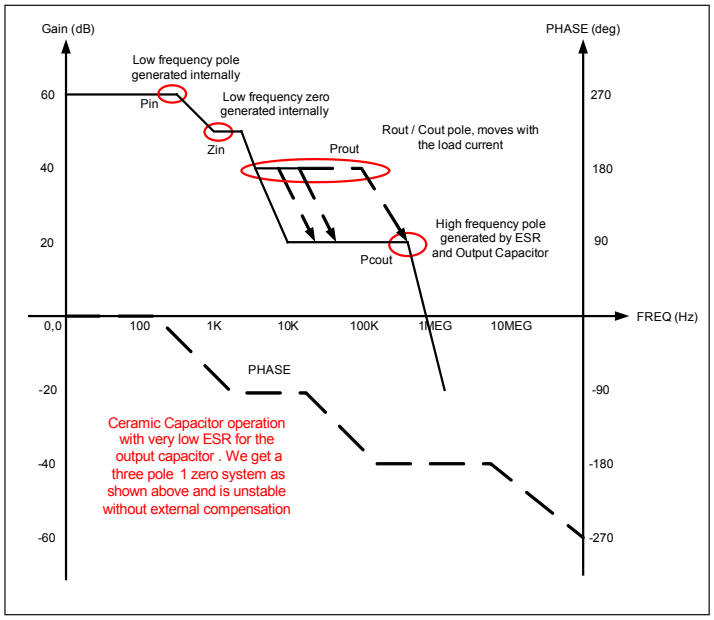
Using Ceramic Capacitors

SC339 is capable of operation using an all-ceramic solution, needing only an external R-C compensation. The Typical Application schematic (R3, C3) from page 1 is reproduced here:



Typical Applications Circuit

Typical Frequency Response without Compensation and Ceramic Output Capacitors:

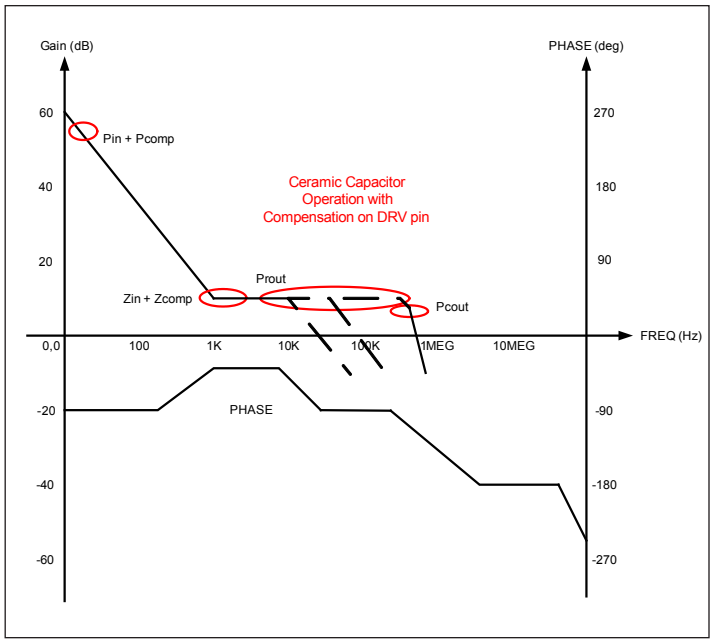


SC339 Frequency Response with Ceramic Output Capacitors and no Compensation

From this response we see that the system is not stable as it has a phase margin of approximately 0 degrees.

For stable operation we introduce a low frequency pole and a zero. The low frequency pole is used to roll off the gain quicker and the zero is used to increase the bandwidth of the system.

The Pole-Zero location:



SC339 Frequency Response with Ceramic Output Capacitors and R-C Compensation

From the above figure we can see that the overall response of the system is stable with a decent phase margin

It is important to select the external compensation zero to be between 1 kHz and 5 kHz for optimum bandwidth and phase margin. In this example we have selected zero at approximately 3 kHz.

The compensation values are calculated by the following empirical equation:

$$\frac{1}{2} \cdot \pi \cdot R3 \cdot C3 = 3kHz$$

We chose a low R3 compensation value to roll off gain.

R3 = 100 Ω.

Applications Information (Cont.)

Now,

$$C3 = ½ \cdot \pi \cdot R3 \cdot 3kHz = 530nF$$

We choose C3 = 470nF as the standard value.

Soft-Start Behavior

At start-up, V_{OUT} first ramps linearly from ground at the rate of ~0.5V/ms (+/- 25%) for about 800us. The linear ramping is followed by a phase of smooth settling for about 700us at the end of which the output has fully settled (to better than 1%).

The total start-up time of about 1.5ms is kept within 1ms - 2ms window, and **this is regardless of the loading and of the external components connected to the device.**

SC339 Start-Up Response

Layout Guidelines

The advantages of using the SC339 to drive external MOSFETs are:

a) that the bandgap reference and control circuitry are in a die that does not contain high power dissipating devices

and,

b) that the device itself does not need to be located right next to the power devices. Thus very accurate output voltages can be obtained since changes due to heating effects will be minimal.

The 0.1µF bypass capacitor should be located close to the supply (IN) and GND pins, and connected directly to the ground plane.

The feedback resistors should be located at the device, with the sense line from the output routed from the load (or top end of the droop resistor if passive droop is being used) directly to the feedback chain. If passive droop is being used, the droop resistor should be located next to the load to avoid adding additional unplanned droop. Sense and drive lines should be routed away from noisy traces or components.

For very low input to output voltage differentials, the input to output/load path should be as wide and short as possible. Where greater headroom is available, wide traces may suffice.

Power dissipation within the device is practically negligible, thus requiring no special consideration during layout. The MOSFET pass devices should be laid out according to the manufacturer's guidelines for the power being dissipated within them.

Performance Characteristics

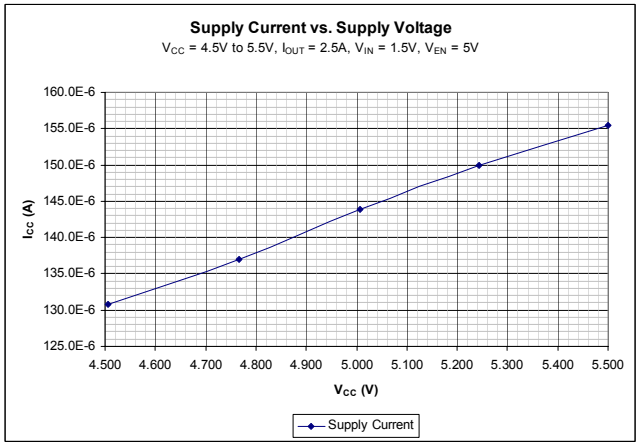


Figure 1: Supply Current v/s Supply Voltage

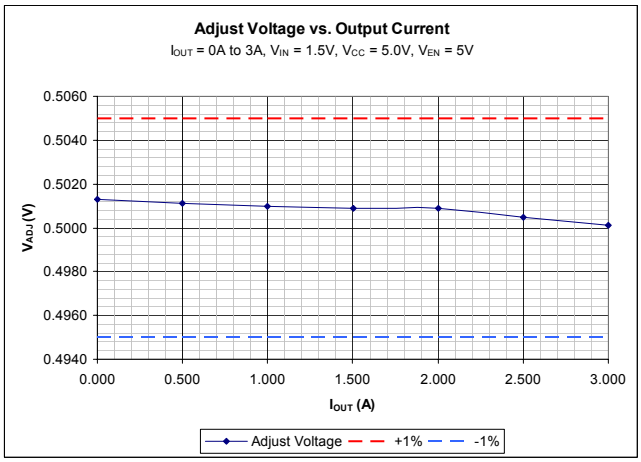


Figure 2: Adjust Voltage v/s Output Current (1% accurate)

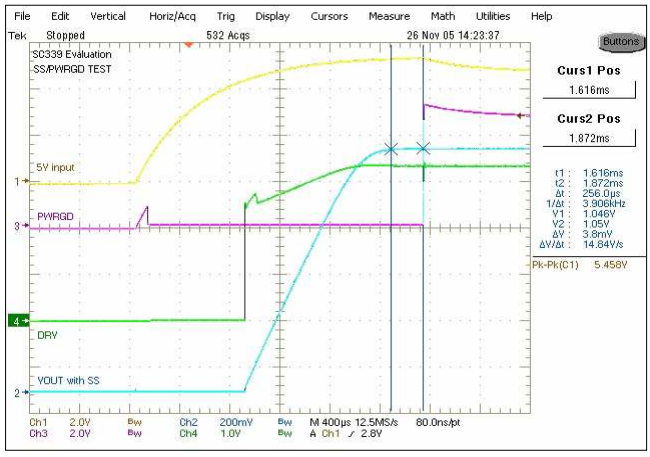


Figure 3: Soft Start waveform shows the PWRGD delay

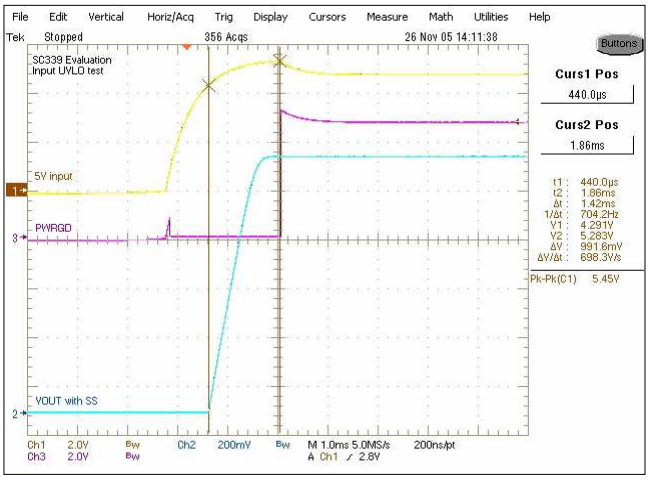


Figure 4: Input UVLO Test (Rising)

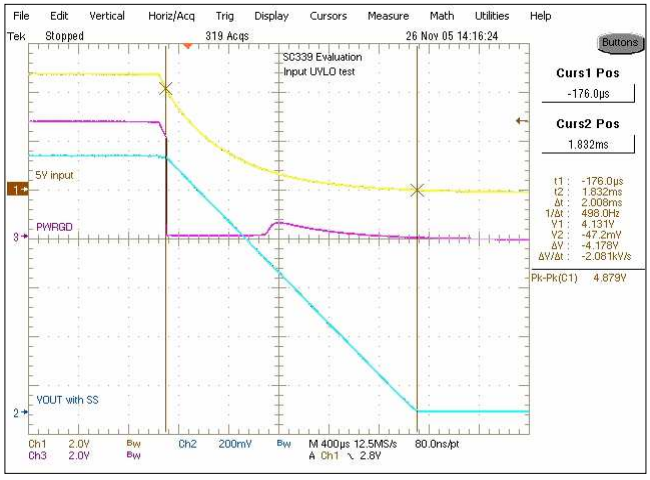


Figure 5: Input UVLO Test (Falling)

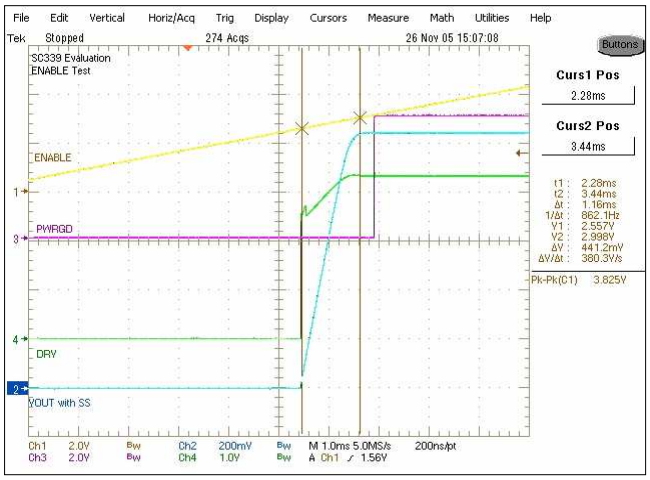


Figure 6: Enable threshold detect (Rising)

Performance Characteristics

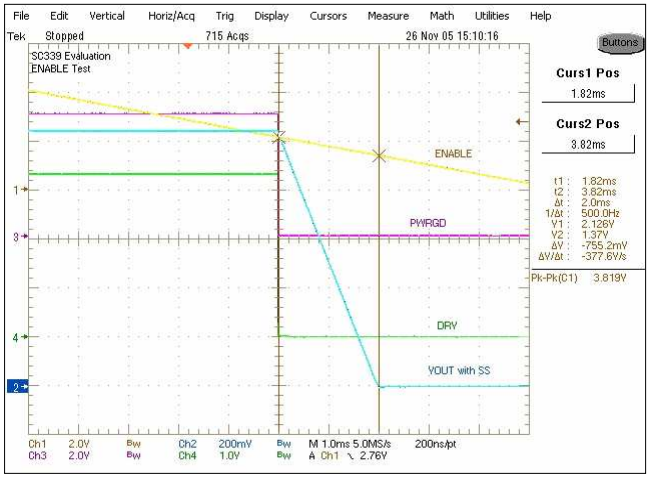


Figure 7: Enable threshold detect (Falling)

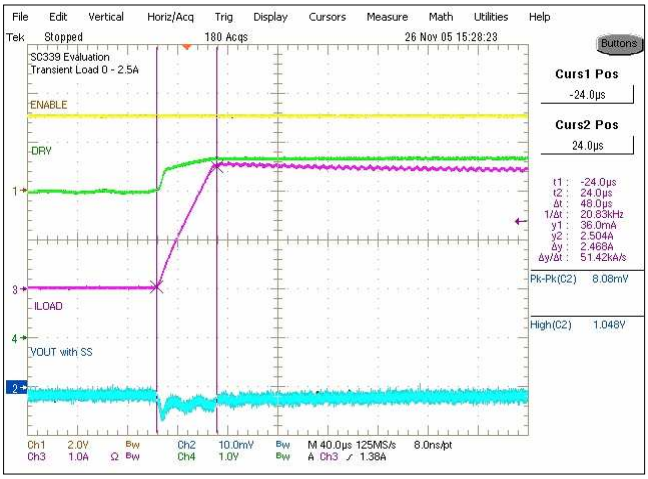
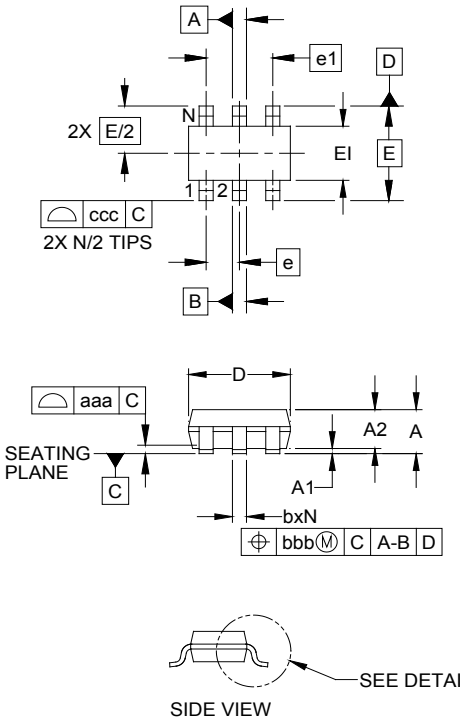


Figure 8: Transient load rising edge

Figure 9: Transient load falling edge

Outline Drawing - SOT-23 6

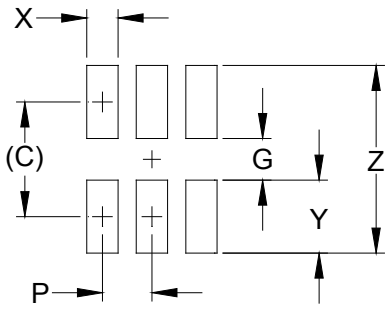


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.118	2.80	2.90	3.00
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT-23 6



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com