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SC4524
Programmable Frequency, 2A Output 30V Step-Down Switching Regulator

Description

The SC4524 is an adjustable frequency peak current-mode step-down switching regulator with an integrated 2.3A, 30V switch. The SC4524 can be programmed up to 1.5MHz. This allows the use of small inductor and ceramic capacitors, resulting in very compact power supplies. The SC4524 is suitable for next generation XDSL modems, set-top boxes and point of load applications.

The SC4524 uses peak current-mode PWM control for ease of compensation. Cycle-by-cycle current limit and hiccup overload protection reduce power dissipation during overload. Combined soft start and enable pin not only eliminates output start up overshoot but also allows power sequencing.

The SC4524 is available in SOIC-8 EDP package.

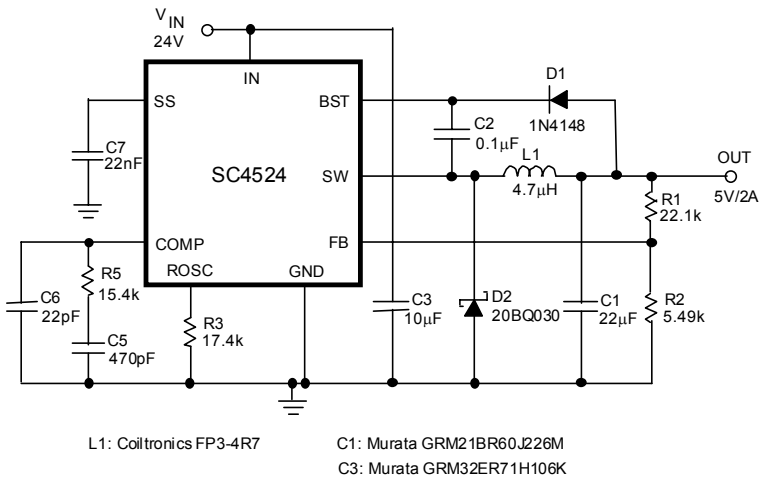
Features

- Up to 1.5 MHz Programmable Switching Frequency
- 2.3A Integrated Switch
- Wide Input Voltage Range 2.8V to 30V
- Peak Current-Mode Control with Cycle-by-Cycle Current Limiting
- Hiccup Overload Protection
- Soft-Start and Enable
- Thermal Shutdown
- Thermally Enhanced 8-Pin SOIC Package
- Fully WEEE and RoHS Compliant

Applications

- XDSL and Cable Modems
- Set-top Boxes
- Point of Load Applications
- CPE Equipment
- DSP Power Supplies
- Disk Drives

Typical Application Circuit



L1: Coiltronics FP3-4R7 C1: Murata GRM21BR60J226M
C3: Murata GRM32ER71H106K

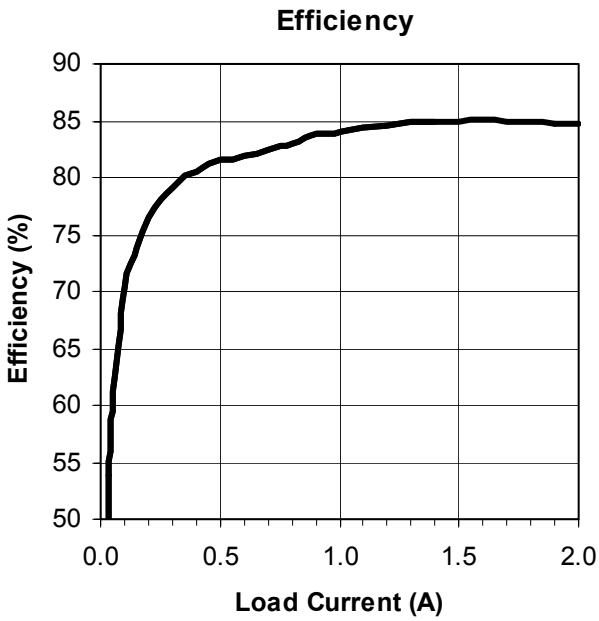


Figure 1. 1MHz 24V to 5V/2A Step-down Converter.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
Input Voltage	V_{IN}	-0.3 to 32	V
BST Pin	V_{BST}	42	V
BST Pin Above SW	V_{BST}-V_{SW}	24	V
SS Pin	V_{SS}	3	V
FB Pin	V_{FB}	-0.3 to V_{IN}	V
SW Voltage	V_{SW}	-0.6 to V_{IN}	V
SW Transient Spikes (<10ns Duration)	V_{SW}	V_{IN}+1.5	V
		-2.5	
Operating Ambient Temperature Range	T_A	-40 to 85	°C
Thermal Resistance Junction to Ambient	θ_{JA}	36	°C/W
Thermal Resistance Junction to Case	θ_{JC}	5.5	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering)10 sec	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	1500	V

Notes: This device is ESD sensitive. ESD handling precaution is required.

Electrical Characteristics

Unless specified: -40°C < T_A < 85°C, -40°C < T_J < 105°C, R_{OSC} = 12.1kΩ, V_{IN} = 5V, V_{BST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
Maximum Operating V_{IN}				30	V
V_{IN} Start Voltage		2.45	2.62	2.78	V
V_{IN} Start Hysteresis			75		mV
V_{IN} Quiescent Current	Not switching		3.5	5	mA
V_{IN} Quiescent Current in Shutdown	V_{SS} = 0V		40	60	µA
Feedback Voltage		0.980	1.000	1.020	V
Feedback Voltage Line Regulation	V_{IN} = 3V to 30V		0.005		%/V
FB Pin Input Bias Current	V_{FB} = 1V, V_{COMP} = 1.5V		-15	-30	nA
Error Amplifier Transconductance			280		$\mu\Omega^{-1}$

Electrical Characteristics (Cont.)

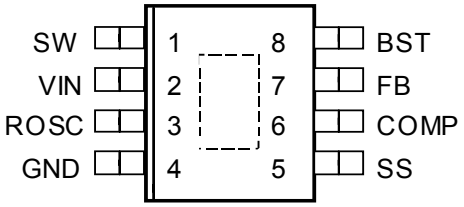
Unless specified: -40°C < T_A < 85°C, -40°C < T_J < 105°C, R_{OSC} = 12.1kΩ, V_{IN} = 5V, V_{BST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
Error Amplifier Open-Loop Gain			53		dB
COMP Source Current	V_{FB} = 0.8V, V_{COMP} = 1.5V		20		µA
COMP Sink Current	V_{FB} = 1.2V, V_{COMP} = 1.5V		20		µA
COMP Pin to Switch Current Gain			8		A/V
COMP Switching Threshold		0.7	1.1	1.3	V
COMP Maximum Voltage	V_{FB} = 0.9V		2.2		V
Switching Frequency		1.2	1.4	1.6	MHz
Maximum Duty Cycle	(Note 2)	80	90		%
Switch Current Limit	(Note 1)	2.3	3.2		A
Switch Saturation Voltage	I_{SW} = -2A		0.3		V
Switch Leakage Current				10	µA
Minimum BST Voltage	I_{SW} = -2A		1.8	2.5	V
BST Pin Current	I_{SW} = -0.5A		20		mA
	I_{SW} = -2A		60		mA
Minimum Soft-Start Voltage to Exit Shutdown		0.2	0.4	0.7	V
Soft-start Charging Current	V_{SS} = 0V		2		µA
	V_{SS} = 1.5V		1.8		µA
Soft-start Discharging Current	V_{SS} = 1.5V		0.8		µA
Minimum Soft-start Voltage to Enable Overload Shutoff	V_{SS} Rising		2		V
FB Overload Threshold	V_{SS} = 2.3V, V_{FB} Falling		0.7		V
Soft-start Voltage to Restart Switching After Overload Shutoff	V_{SS} Falling	0.7	1	1.3	V
Thermal Shutdown Temperature			155		°C
Thermal Shutdown Hysteresis			10		°C

Notes: (1) Guaranteed by design, not tested in production.
(2) The maximum duty cycle specified corresponds to 1.4MHz switching frequency. Duty cycles higher than those specified can be achieved by lowering the operating frequency.

Pin Configuration

TOP VIEW



(8 Pin SOIC-EDP)

Underside metal must be soldered to ground.

Ordering Information

Part Number	Package
SC4524SETRT(1)(2)	SOIC-8 EDP
SC4524EVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

SO-8EDP	Pin Name	Pin Function
1	SW	The emitter of the internal NPN power transistor. Connect this pin to the inductor and the freewheeling diode.
2	VIN	Power supply to the SC4524. It is also connected to the collector of the internal NPN power transistor. It must be bypassed with a ceramic capacitor to ground.
3	ROSC	Frequency setting pin. An external resistor from his pin to the ground sets the oscillator frequency.
4	GND	Ground pin.
5	SS	Soft start and enable pin. (1). A capacitor from SS pin to the ground provides soft-start and overload hiccup functions. Soft start is recommended for all applications. (2). Pulling SS pin below 0.4V shuts off the regulator and reduces the input supply current to 40uA at 5V.
6	COMP	Compensation pin. It is also the output of the internal error amplifier. (1). A RC network at this pin compensates the control loop. (2). The voltage at this pin controls the peak current of the internal switch.
7	FB	The output voltage feedback pin. It is also the inverting input of the error amplifier.
8	BST	Supply pin to the power transistor driver. Tie to external bootstrap circuit to generate a local supply voltage higher than the input voltage in order to fully turn on the internal power transistor.
Metal Pad		The exposed pad at the bottom of the package is electrically connected to the ground pin of the SC4524. It also provides a thermal contact to the circuit board. It has to be soldered to the analog ground of the PC board.

Block Diagrams

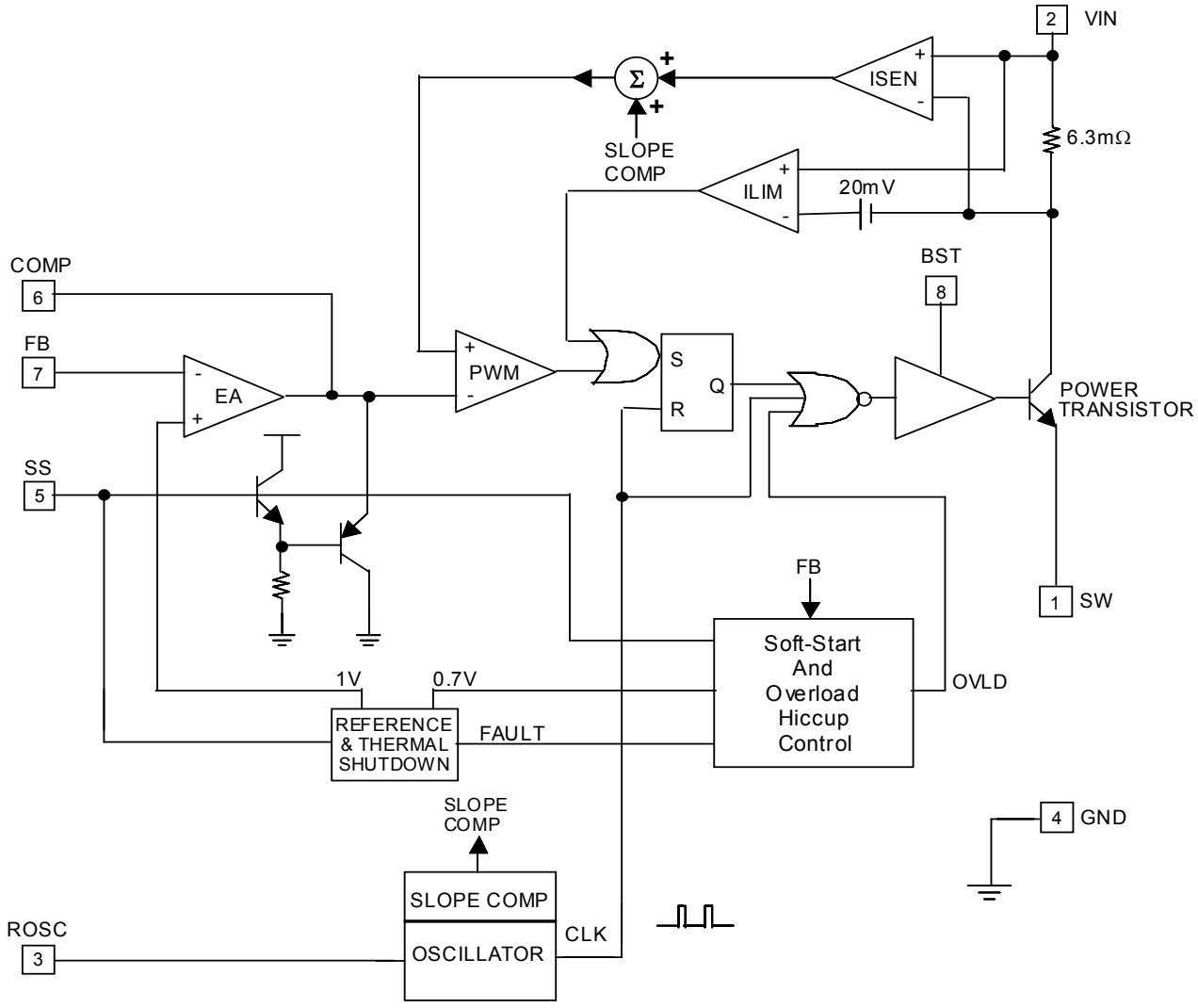


Figure 2. SC4524 Functional Diagram

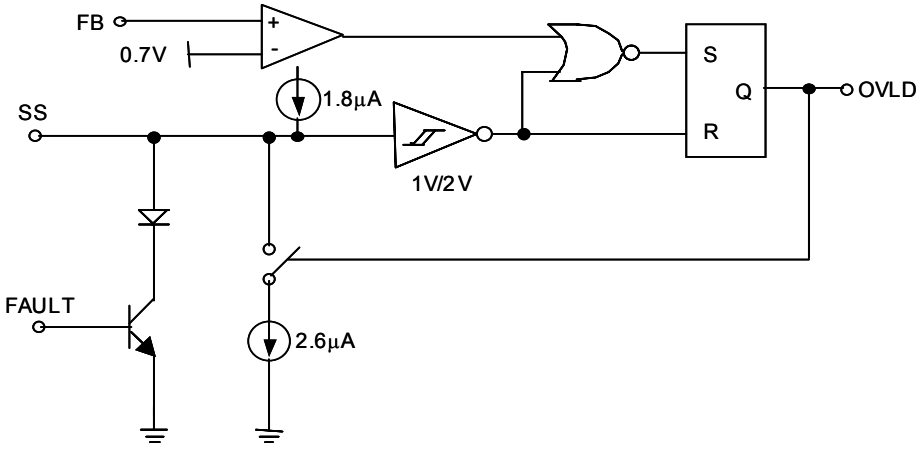
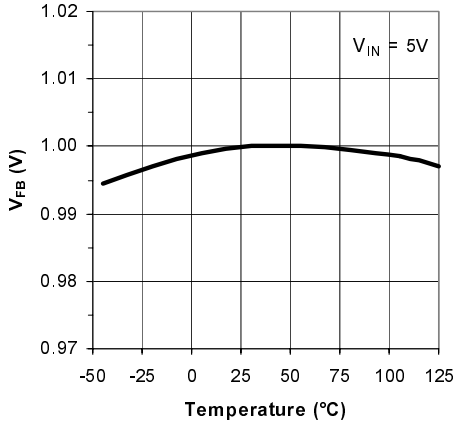


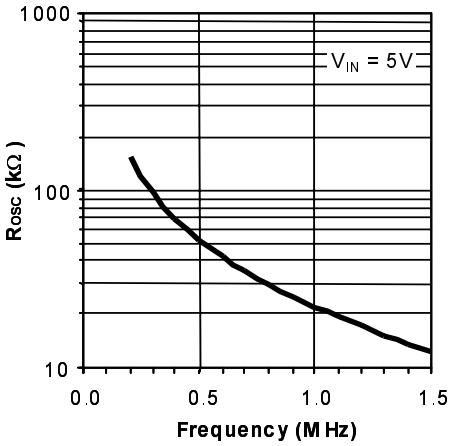
Figure 3. Details of the Soft-Start and Overload Hiccup Control Circuit

Typical Characteristics

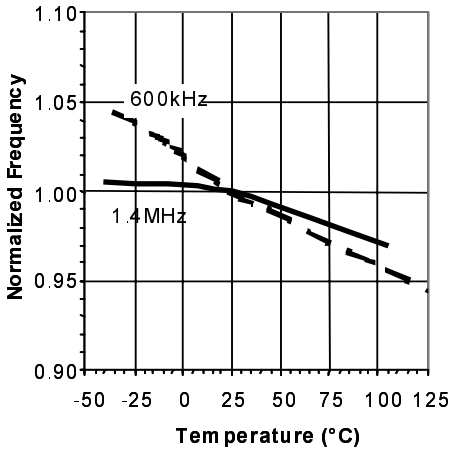
Feedback Voltage vs Temperature



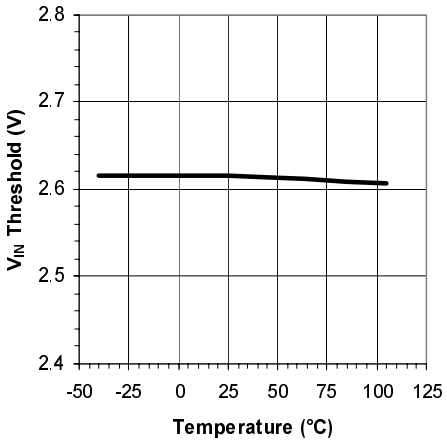
Frequency Setting Resistor vs Frequency



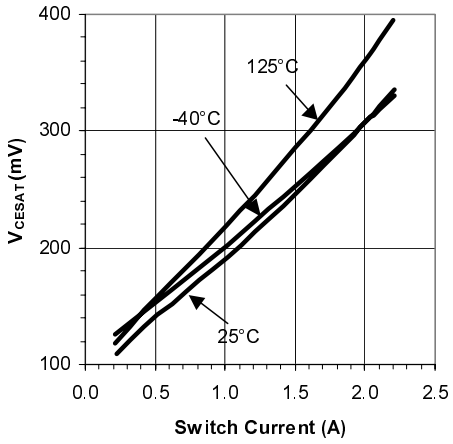
Normalized Frequency vs Temperature



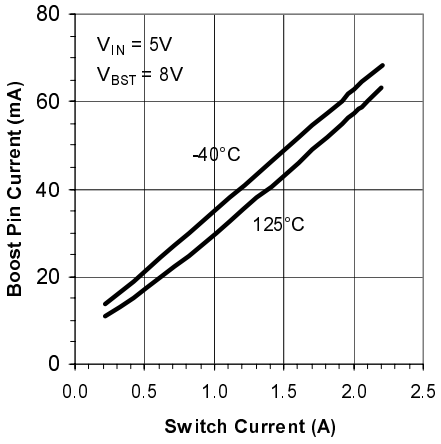
V_{IN} Start Threshold vs Temperature



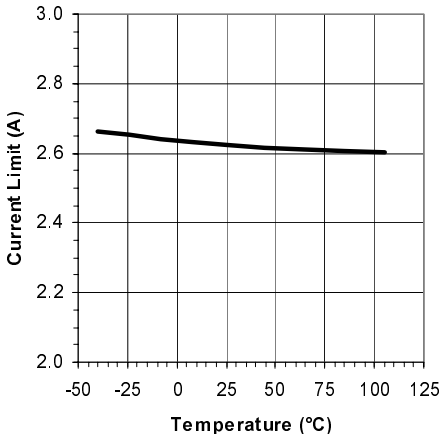
Switch Saturation Voltage vs Switch Current



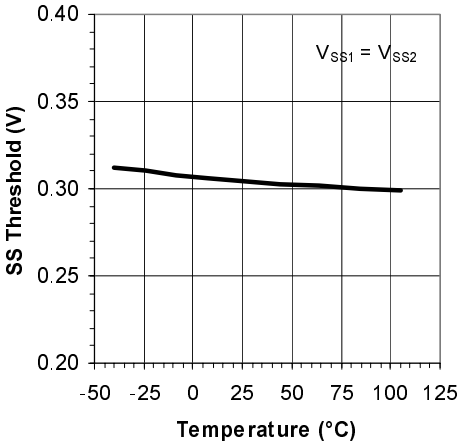
Boost Pin Current vs Switch Current



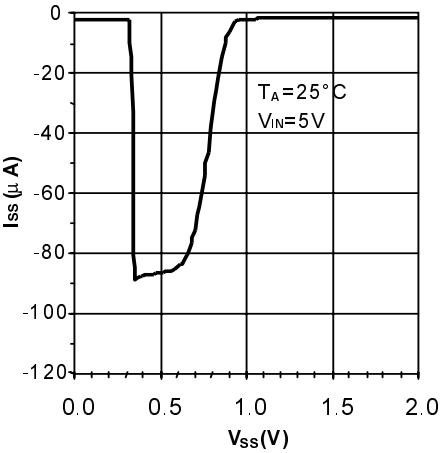
Switch Current Limit vs Temperature



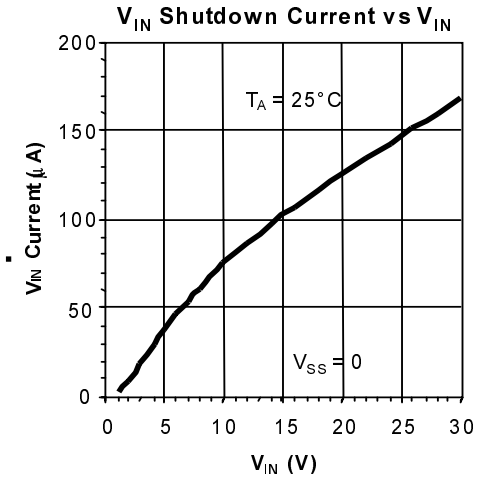
SS Shutdown Threshold vs Temperature

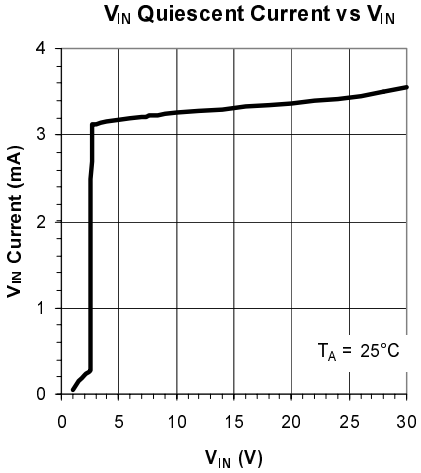


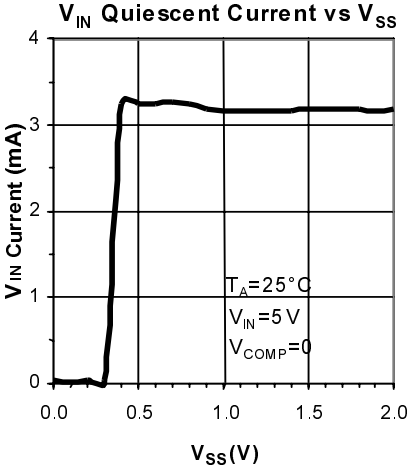
Soft-Start Pin Current vs Soft-Start Voltage

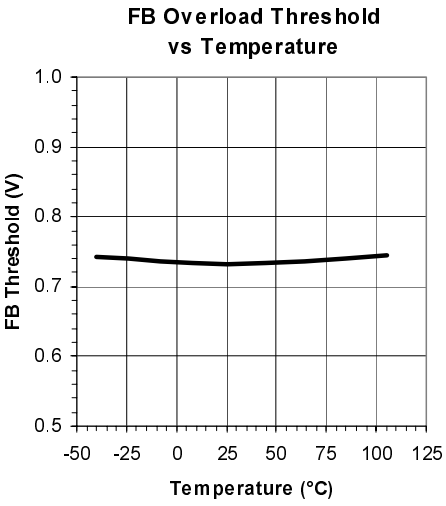


Typical Characteristics









Operation

The SC4524 is a 30V constant-frequency peak current-mode step-down switching regulator with an integrated 2.3A power transistor. The switching frequency can be programmed with an external resistor from the ROSC pin to ground. Frequency adjustability makes switching regulator design flexible.

Peak current mode control is utilized for the SC4524. The double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop, easing loop compensation. Fast transient response can be achieved with a simple Type-2 compensation network. Switch collector current is sensed with an integrated 6.3mΩ sense resistor. The sensed current is summed with slope-compensating ramp before it is compared with the transconductance error amplifier output. The PWM comparator trip point determines the switch turn-on pulse width (Figure 2). The current-limit comparator ILIM turns off the power switch when the sensed-signal exceeds the 20mV current-limit threshold. ILIM therefore provides cycle-by-cycle limit. Current-limit does not vary with duty-cycle.

Driving the base of the power transistor above the input power supply rail minimizes the power transistor turn-on voltage and maximizes efficiency. An external charge pump (or bootstrap circuit) generates a voltage higher than the input rail at the BST pin. The bootstrapped voltage generated becomes the supply voltage for the power transistor driver.

The SS pin is a multiple-function pin. An external capacitor connected from the SS pin to ground together with the internal 1.8µA and 2.6µA current sources set the soft-start and overload shutoff times of the regulator (Figure 3). The SS pin can also be used to shut off the regulator. When the SS pin is pulled below 0.8V, the regulator is turned off. If the SS pin is pulled below 0.2V, then the SC4524 will undergo overall shutdown. The current drawn from the input power supply reduces to 40µA. When the SS pin is released, the soft-start capacitor is charged with a 2µA current source (not shown in Figure 3). As the SS voltage exceeds 0.4V, the internal bias circuit of the SC4524 is enabled. The SC4524 draws 3.5mA from V_{IN}. An internal fast charge circuit quickly charges the soft-start capacitor to 1V. At this juncture, the fast charge circuit turns off and the 1.8µA current source slowly charges the soft-start capacitor. The output of the error amplifier is forced to track the slow soft-start ramp at the SS pin. When the COMP voltage exceeds 1.1V, the switching regulator starts to switch. During soft-start, the current limit of the converter is gradually increased until the converter output comes into regulation.

Hiccup overload protection is utilized in the SC4524. Overload shutdown is disabled during soft-start (V_{SS} < 2V). In Figure 3 the reset input of the overload latch will remain high if the SS voltage is below 2V. Once the soft-start capacitor is charged above 2V, the overload shutdown latch is enabled. As the load draws more current from the regulator, the current-limit comparator will limit the peak inductor current. This is cycle-by-cycle current limiting. Further increase in load current will cause the output voltage to decrease. If the output voltage falls below 70% of its set point, then the overload latch will be set and the soft-start capacitor will be discharged with a net current of 0.8µA. The switching regulator is shut off until the soft-start capacitor is discharged below 1V. At this moment, the overload latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start. The regulator will go through soft-start, overload shutdown and restart until it is no longer overloaded.

Applications Information

Setting the Output Voltage

The regulator output voltage is set with an external resistive divider (Figure 4) with its center tap tied to the FB pin.

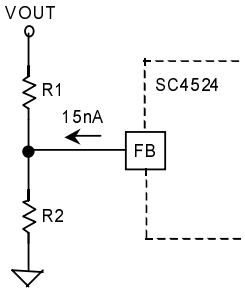


Figure 4. V_{OUT} is set with a Resistive Divider

$$R_1 = R_2(V_{OUT} - 1) \quad (1)$$

The percentage error due the input bias current of the error amplifier is

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (R_1 || R_2)}{1V}.$$

Example: Determine the output voltage error of a $V_{OUT} = 5V$ converter with $R_2 = 51.1k\Omega$.

From (1),

$$R_1 = 51.1k\Omega \cdot (5 - 1) = 205k\Omega$$

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (51.1k || 205k)}{1V} = -0.061\%.$$

This error is at least an order of magnitude lower than the ratio tolerance resulting from the use of 1% resistors in the divider string.

Setting the Switching Frequency

The switching frequency of the SC4524 is set with an external resistor from the ROSC pin to ground. A graph of switching frequency against R_{OSC} is shown in "Typical Performance Characteristics". The switching frequency is programmable up to 1.5MHz.

The switching frequency is limited by the minimum controllable on time at low duty cycles. For V_{IN} > 20V, setting switching frequency below 500kHz makes converter output short circuit operation more robust. These will be described in more details later.

Minimum On Time Consideration

The operating duty cycle of a non-synchronous step-down switching regulator in continuous-conduction mode (CCM) is given by

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{CESAT}} \quad (2)$$

where V_{CESAT} is the switch saturation voltage and V_D is voltage drop across the rectifying diode.

Duty cycle decreases with increasing $\frac{V_{IN}}{V_{OUT}}$ ratio. In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum controllable switch on time ($T_{ON(MIN)}$). Closed-loop measurement of the SC4524 with low $\frac{V_{OUT}}{V_{IN}}$ ratios

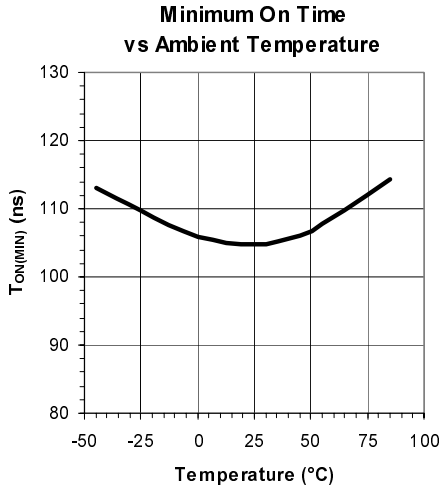


Figure 5. Variation of Minimum On Time with Ambient Temperature.

Applications Information

shows that the minimum on time is about 105ns at room temperature (Figure 5). The power switch in the SC4524 is either not turned on at all or for at least $T_{ON(MIN)}$. If the required switch on time ($=\frac{D}{f}$) is shorter than the minimum on time, the regulator will either skip cycles or it will jitter.

Example: Determine the maximum operating frequency of a 24V to 1.2V switching regulator using the SC4524.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 26.4V (10% high line), the duty ratio can be calculated using (2).

$$D = \frac{1.2 + 0.45}{26.4 + 0.45 - 0.25} = 0.062$$

To allow for transient headroom, the minimum operating switch on time should be at least 30% higher than the worst-case minimum on time exhibited in Figure 5. Designing for a switch on time of 150ns at $V_{IN} = 26.4V$, the maximum operating frequency is $\frac{D}{150ns} = 410KHz$.

Minimum Off Time Limitation

The PWM latch in Figure 2 is reset every period by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. The measured minimum off time is 120ns. For a step-down converter, D increases with increasing $\frac{V_{OUT}}{V_{IN}}$ ratio. If the required duty cycle is higher than the attainable maximum, then the output voltage will not be able to reach its set value in continuous-conduction mode.

Example: Determine the maximum operating frequency of a 5V to 4V switching regulator using the SC4524.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 4.5V (10% low line), the duty ratio can be calculated using (2).

$$D = \frac{4 + 0.45}{4.5 + 0.45 - 0.25} = 0.95.$$

The maximum operating channel frequency of the converter is therefore $\frac{1 - D}{120ns} = 410KHz$.

Transient headroom requires that channel frequency be lower than 410kHz.

Inductor Selection

The inductor ripple current ΔI_L for a non-synchronous step-down converter in continuous-conduction mode is

$$\Delta I_L = \frac{(V_{OUT} + V_D)(1 - D)}{fL} = \frac{(V_{OUT} + V_D)(V_{IN} - V_{OUT} - V_{CESAT})}{(V_{IN} + V_D - V_{CESAT})fL} \quad (3)$$

where f is the switching frequency and L is the inductance.

In current-mode control, the slope of the modulating (sensed switch current) ramp should be steep enough to lessen jittery tendency but not so steep that large flux swing decreases efficiency. Inductor ripple current ΔI_L between 25-40% of the peak inductor current limit is a good compromise. Inductors so chosen are optimized in size and DCR. Setting $\Delta I_L = 0.3(2.3) = 0.69A$, $V_D = 0.45V$ and $V_{CESAT} = 0.25V$ in (3),

$$L = \frac{(V_{OUT} + 0.45)(V_{In} - V_{OUT} - 0.25)}{(V_{IN} + 0.2)(0.69)f} \quad (4)$$

where L is in µH and f is in MHz.

Equation (3) shows that for a given V_{OUT}, ΔI_L increases as D decreases. If V_{IN} varies over a wide range, then choose L based on the nominal input voltage. Always verify converter operation at the input voltage extremes.

The peak current limits of both SC4524 power transistors are internally set at 3.2A. The peak current limits are

duty-cycle invariant and are guaranteed higher than 2.3A. The maximum load current is therefore conservatively

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = 2.3A - \frac{\Delta I_L}{2} \quad (5)$$

If $\Delta I_L = 0.3 \cdot I_{LM}$, then

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = I_{LM} - \frac{0.3 I_{LM}}{2} = 0.85 \cdot I_{LM}.$$

The saturation current of the inductor should be 20-30% higher than the peak current limit (2.3A). Low-cost powder iron cores are not suitable for high-frequency switching power supplies due to their high core losses. Inductors with ferrite cores should be used.

Power Line Input Capacitor

A buck converter draws pulse current with peak-to-peak amplitude equal to its output current I_{OUT} from its input supply. An input capacitor placed between the supply and the buck converter filters the AC current and keeps the current drawn from the supply to a DC constant. The input capacitance C_{IN} should be high enough to filter the pulse input current. Its equivalent series resistance (ESR) should be low so that power dissipated in the capacitor does not result in significant temperature rise and degrade reliability. For a buck converter, the RMS ripple current in the input capacitor is

$$I_{RMS_{(CIN)}} = I_{OUT}\sqrt{D(1-D)}. \quad (6)$$

Power dissipated in the input capacitor is $I^2_{RMS_{(CIN)}} \cdot (ESR)$.

Equation (6) has a maximum value of $\frac{I_{OUT}}{2}$ (at $D = \frac{1}{2}$), corresponding to the worst-case power dissipation $\frac{I^2_{OUT} \cdot ESR}{4}$ in C_{IN}.

Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple current, are the ideal choice for input filtering. A single 4.7µF or 10µF X5R ceramic capacitor is adequate. For high voltage applications, a small ceramic (1µF or 2.2µF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

Output Capacitor

The output ripple voltage ΔV_{OUT} of a buck converter can be expressed as

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 f C_{OUT}} \right) \quad (7)$$

where C_{OUT} is the output capacitance.

Inductor ripple current ΔI_L increases as D decreases (Equation (3)). The output ripple voltage is therefore the highest when V_{IN} is at its maximum. The first term in (7) results from the ESR of the output capacitor while the second term is due to the charging and discharging of C_{OUT} by the inductor ripple current. Substituting ΔI_L = 0.69A, f = 500kHz and C_{OUT} = 22µF ceramic with ESR = 2mΩ in (7),

$$\Delta V_{OUT} = 0.69A \cdot (2m\Omega + 11.4m\Omega)$$
$$= 1.4mV + 7.8mV = 9.2mV$$

Depending on operating frequency and the type of capacitor, ripple voltage resulting from charging and discharging of C_{OUT} may be higer than that due to ESR. A 10µF to 47µF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds C_{OUT}, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and high voltage coefficients.

Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery input current spikes, easing high-side current sensing in the SC4524. These diodes should have an average forward current rating between 1A and 2A and a reverse blocking voltage of at least a few volts higher than the input voltage. For switching regulators operating at low duty cycles (i.e. low

Applications Information

output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher average current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The freewheeling diodes should be placed close to the SW pins of the SC4524 to minimize ringing due to trace inductance. 10BQ015, 20BQ030 (International Rectifier), MBRM120LT3 (ON Semi), UPS120 and UPS140 (Micro-Semi) are all suitable.

Bootstrapping the Power Transistors

To maximize efficiency, the turn-on voltage across the internal power NPN transistor should be minimized. If the transistor is to be driven into saturation, then its base will have to be driven from a power supply higher in voltage than V_{IN}. The required driver supply voltage (at least 2.5V higher than the SW voltage over the industrial temperature range) is generated with a bootstrap circuit (the diode D_{BST} and the capacitor C_{BST} in Figure 7). The bootstrapped output (the common node between D_{BST} and C_{BST}) is connected to the BST pin of the SC4524. The power transistor in the SC4524 is first switched on to build up current in the inductor. When the transistor is switched off, the inductor current pulls the SW node low, allowing C_{BST} to be charged through D_{BST}. When the power switch is again turned on, the SW voltage goes high. This brings the BST voltage to $V_{SW} + V_{C_{BST}}$, thus back-biasing D_{BST}. C_{BST} voltage increases with each subsequent switching cycle, as does the bootstrapped voltage at the BST pin. After a number of switching cycles, C_{BST} will be fully charged to a voltage approximately equal to that applied to the anode of D_{BST}. Figure 6 shows the typical minimum BST to SW voltage required to fully saturate the power transistor. This differential voltage ($= V_{C_{BST}}$) must be at least 1.8V at room temperature. This is also specified in the "Electrical Characteristics" as "Minimum Bootstrap Voltage". The minimum required V_{CBST} increases as temperature decreases. The bootstrap circuit reaches equilibrium when the base charge drawn from C_{BST} during transistor on time is equal to the charge replenished during the off interval.

The switch base current $= \frac{I_{SW}}{\beta + 1} \approx \frac{I_{SW}}{\beta}$, where I_{SW} and β are the switch emitter current and current gain respectively, is drawn from the bootstrap capacitor C_{BST}. Charge $\frac{I_{SW} T_{ON}}{\beta}$ is drawn from C_{BST} during the switch on time, resulting in a voltage droop of $\frac{I_{SW} T_{ON}}{\beta C_{BST}}$. If I_{SW} = 2A, T_{ON} = 1µs, β = 35 and C_{BST} = 0.1µF, then the $V_{C_{BST}}$ droop will be 0.57V. C_{BST} is refreshed to $V_A - V_{D_{BST}} + V_{D_{RECT}}$ every cycle, where V_A is the applied D_{BST} anode voltage. Switch base current discharges the bootstrap capacitor to $V_A - V_{D_{BST}} + V_{D_{RECT}} - \frac{I_{SW} T_{ON}}{\beta C_{BST}}$ at the end of conduction. This voltage must be higher than the minimum shown in Figure 6 to ensure full switch enhancement. D_{BST} can be tied either to the input or to the output of the DC/DC converter.

If D_{BST} is tied to the input, then the charge drawn from the input power supply will be $\frac{I_{SW} T_{ON}}{\beta}$ (the base charge of the switch). The energy loss due to base charge per

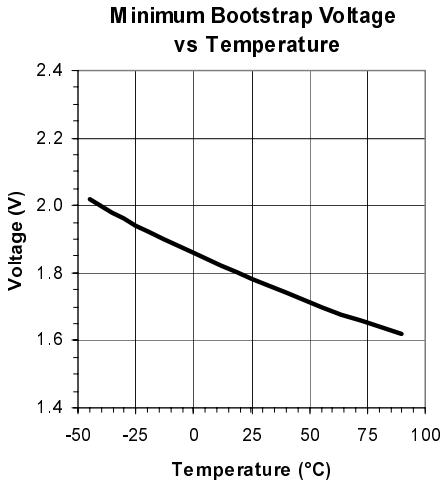


Figure 6. Typical Minimum Bootstrap Voltage Required to Maintain Saturation at I_{SW} = 2A.

cycle is $\frac{I_{SW} V_{IN} T_{ON}}{\beta}$ for a power loss of $\frac{DI_{SW} V_{IN}}{\beta} \approx \frac{I_{SW} V_{OUT}}{\beta}$. loss of $\frac{DI_{SW} V_{OUT}}{\beta}$.

If D_{BST} is tied to the output, then the charge drawn from the output capacitor will still be $\frac{I_{SW} T_{ON}}{\beta}$. The energy loss due to base charge per cycle is $\frac{I_{SW} V_{OUT} T_{ON}}{\beta}$ for a power

Since $V_{OUT} < V_{IN}$, D_{BST} should always be tied to V_{OUT} (if >2.5V) to maximize efficiency. In general efficiency penalty increases as D decreases.

Figure 7 summarizes various ways of bootstrapping the SC4524. A fast switching PN diode (such as 1N4148 or

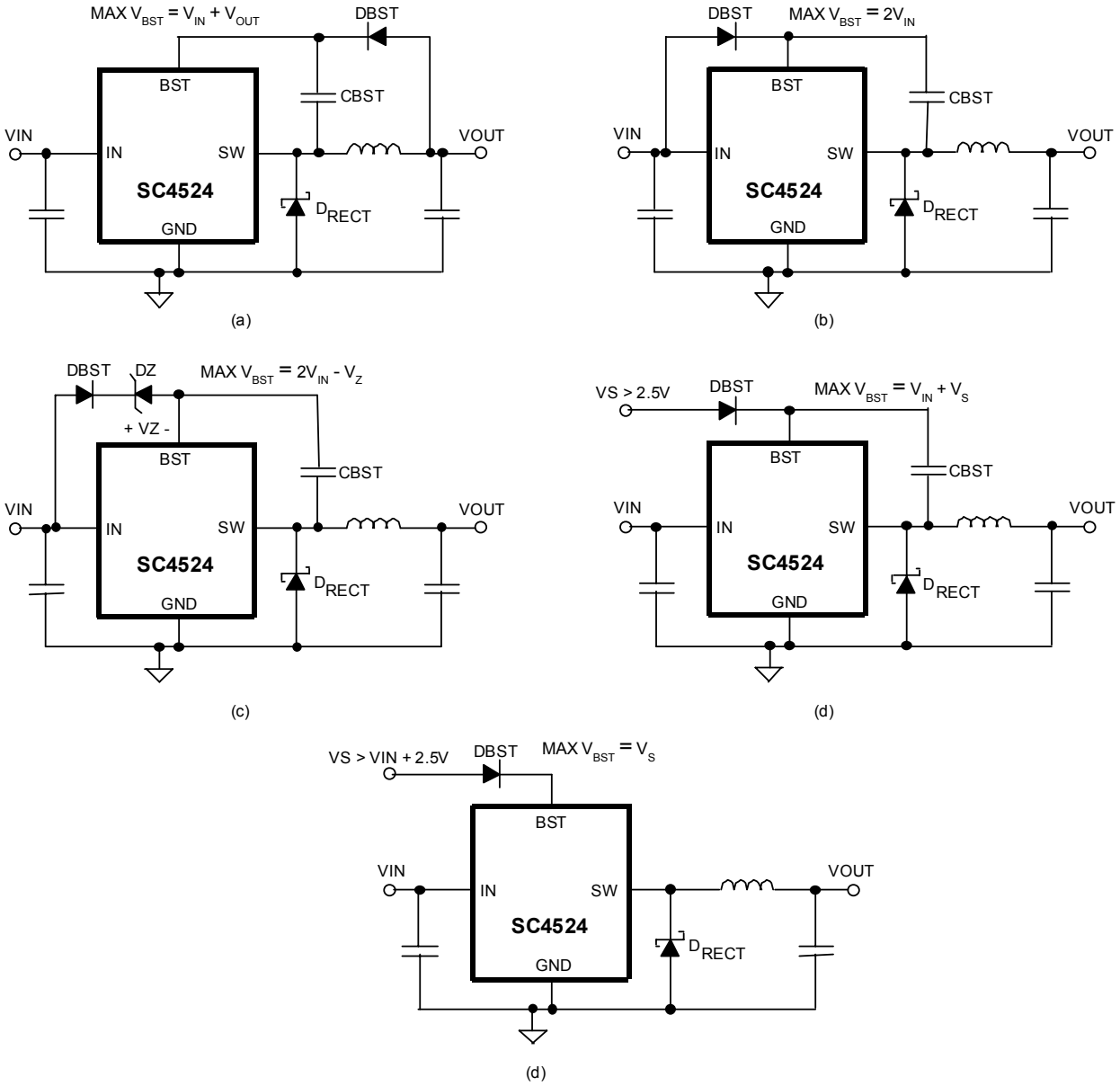


Figure 7. Methods of Bootstrapping the SC4524.

Applications Information

1N914) and a small (0.1µF – 0.47µF) ceramic capacitor can be used. In Figure 7(a) the power switch is bootstrapped from the output. This is the most efficient configuration and it also results in the least voltage stress at the BST pin. The maximum BST pin voltage is about $V_{IN}+V_{OUT}$. If the output is below 2.8V, then D_{BST} will preferably be a small Schottky diode (such as BAT-54) to maximize bootstrap voltage. A 0.33-0.47µF bootstrap capacitor may be needed to reduce droop. Bench measurement shows that using Schottky bootstrapping diode has no noticeable efficiency benefit.

The SC4524 can also be bootstrapped from the input (Figure 7(b)). This configuration is not as efficient as Figure 7(a). However this may be only option if the output voltage is less than 2.5V and there is no other supply with voltage higher than 2.5V. Voltage stress at the BST pin can be somewhat higher than $2V_{IN}$. The Zener diode in Figure 7(c) reduces the maximum BST pin voltage. The BST pin voltage should not exceed its absolute maximum rating of 42V.

Figures 7(d) and (e) show how to bootstrap the SC4524 from a second power supply V_S with voltage > 2.5V.

Since the inductor current charges C_{BST}, the bootstrap circuit requires some minimum load current to get going. Figures 8(a) and 8(b) show the dependence of the minimum input voltage required to properly bootstrap a 5V and a 3.3V converters on the load current. Once started the bootstrap circuit is able to sustain itself down to zero load.

Shutdown and Soft-Start

Pulling the soft-start pin below 0.8V with an open-collector NPN or an open-drain NMOS transistor turns off the regulator. In "Typical Characteristics", the soft-start pin current is plotted against the soft-start voltage with V_{IN} = 5V. When the soft-start pin is pulled below 1V, 105µA current flows out of the pin. Pulling the soft-start pin below 0.2V shuts off the internal bias circuit of the SC4524. The total V_{IN} current decreases to 40µA. In shutdown the SS pin sources only 2µA. A fast charging circuit (enabled by the internal bias circuit), which charges the soft-start capacitor below 1V, causes the difference in the soft-start pin currents.

If the SS pin is released in shutdown, the internal current source pulls up on the SS pin. When this SS voltage reaches 0.4V, the SC4524 turns on and the V_{IN} quiescent current increases to 3.5mA. The fast charging circuit quickly pulls the released soft-start capacitor to 1V (slightly below the switching threshold). The fast charging circuit is then disabled. A 1.8µA current source continues to charge the soft-start capacitor (Figure 3). The soft-

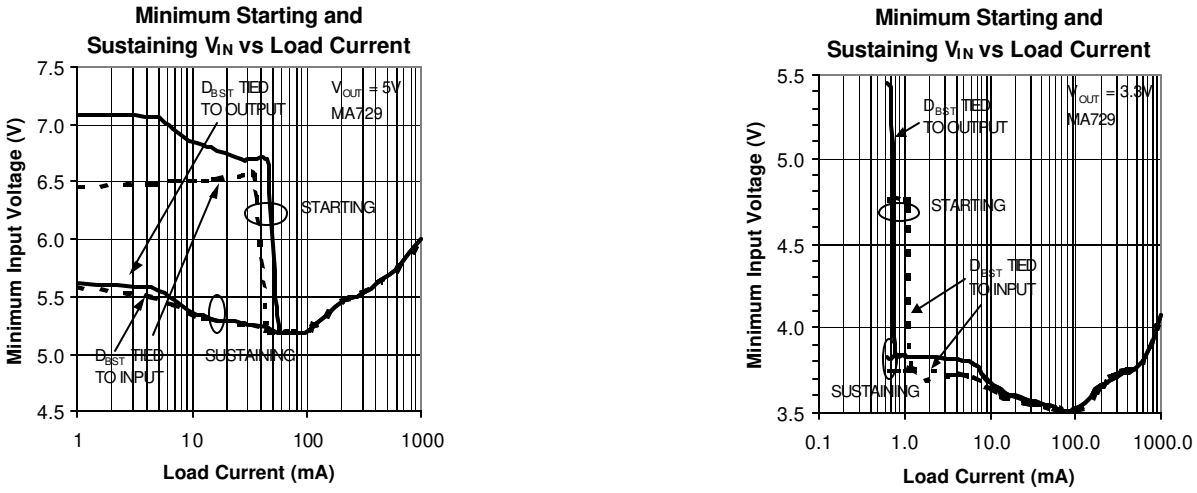


Figure 8. Minimum Input Voltage Required to Start and to Maintain Bootstrap.(T_A = 25°C).

start voltage ramp at the SS pin clamps the error amplifier output (Figure 2). During regulator start-up, COMP voltage follows the SS voltage. The converter starts to switch when its COMP voltage exceeds 1.1V. The peak inductor current gradually increases until the converter output comes into regulation. Proper soft-start prevents output overshoot during start-up. Current drawn from the input supply is also well controlled. Notice that the inductor current, not the converter output voltage, is ramped during soft-start.

The soft-start capacitor is charged to a final voltage of about 2.4V.

Overload / Short-Circuit Protection

The current limit comparator in the SC4524 limits the peak inductor current to 3.2A (typical). The regulator output voltage will fall if the load is increased above the current limit. If overload is detected (the output voltage falls below 70% of the set voltage), then the regulator will be shut off. An internal 0.8µA current sink starts to discharge the soft-start capacitor. As the soft-start capacitor is discharged below 1V, the discharge current source turns off and the soft-start capacitor is recharged with a 1.8µA current source. The regulator undergoes soft-start. During soft-start ($1V < V_{SS} < 2V$), the overload shutdown latch in Figure 3 cannot be set. When V_{SS} exceeds 2V, the set input of the overload latch is no

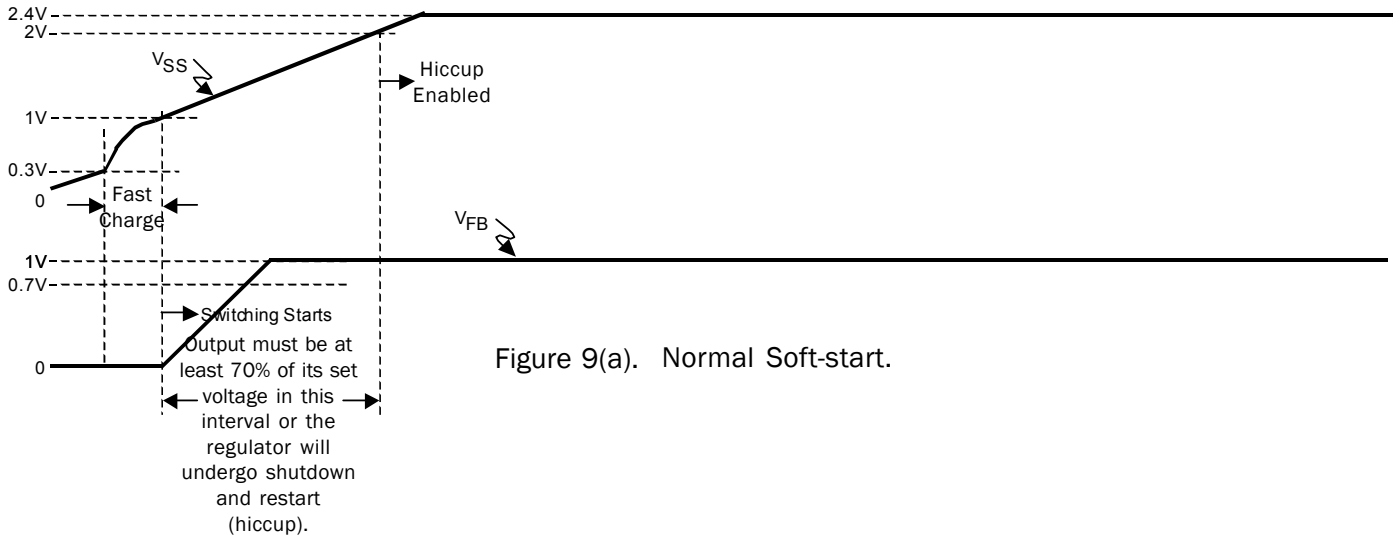


Figure 9(a). Normal Soft-start.

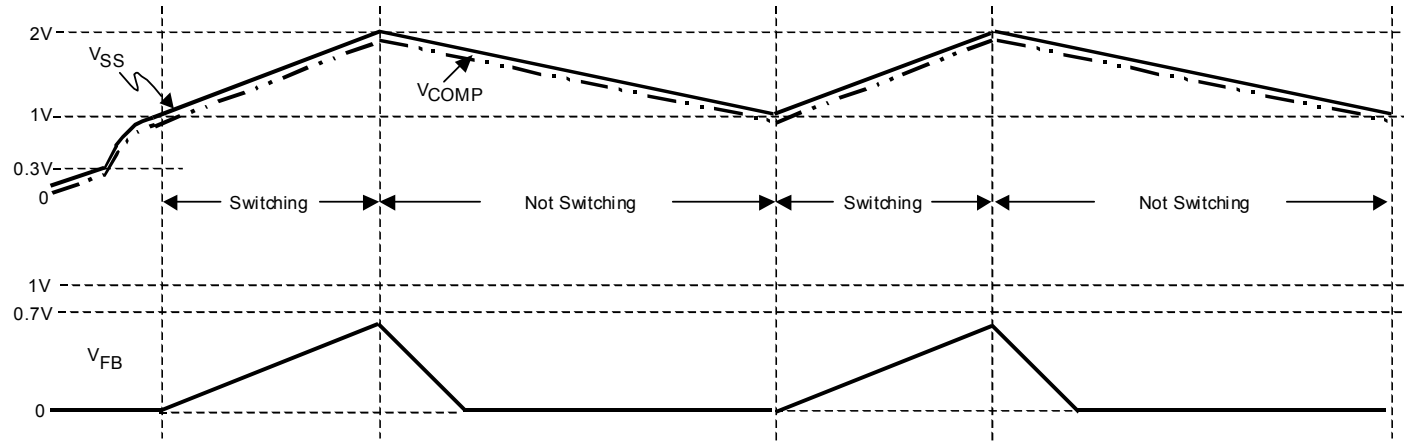


Figure 9(b). Start-up Fails due to (i) Short Soft-start Duration or (ii) Output Overload or (iii) Output Short-circuited.

longer blanked. If V_{FB} is still below 0.7V, then the regulator will undergo shutdown and restart. The soft-start process should allow the output voltage to reach 70% of its final value before C_{SS} is charged above 2V. Figures 9(a) and 9(b) show the timing diagrams of successful and failed start-up waveforms respectively. The soft-start interval should also be made sufficiently long so that the output voltage rises monotonically and it does not overshoot its final voltage by more than 5%.

During normal soft-start, both the COMP voltage and the switch current limit gradually increase until the converter becomes regulated. If the regulator output is shorted to ground, then the COMP voltage will continue to rise to its 2.4V upper limit. The SC4524 will reach its cycle-by-cycle current limit sometime during the soft-start charging phase. As described previously, the switches in the SC4524 either do not turn on at all or for at least 105ns. With the output shorted, the error amplifier will command the regulator to operate at full duty cycle. The current limit comparator will turn off the switch if the switch current exceeds 3.2A. However, this happens only after the switch is turned on for 105ns. During switch off time, the inductor current ramps down at a slow rate determined by the forward voltage of the freewheeling diode and the resistance of the short. If the resulting reverse volt-second is insufficient to reset the inductor before the start of the next cycle, then the inductor current will keep increasing until the diode forward voltage becomes high enough to achieve volt-second balance. This makes the current limit comparator ineffective. Setting the switching frequency below 500kHz at high V_{IN} (> 20V) will make the off time sufficiently long to keep the inductor current within bounds under short circuit condition.Shortening the soft-start interval from the onset of switching to hiccup enable also makes short circuit operation more robust. A 22-47nF soft-start capacitor is found adequate for most applications.

Loop Compensation

Figure 10 shows a simplified equivalent circuit of a step-down converter. The power stage, which consists of the current-mode PWM comparator, the power switch, the freewheeling diode and the inductor, feeds the output network. The power stage can be modeled as a voltage-controlled current source, producing an output current proportional to its controlling input V_{COMP}. Its transconductance G_{MP} is $8\Omega^{-1}$. With the current loop closed, the control-to-output transfer function $\frac{v_{OUT}}{v_{COMP}}$ has a dominant-pole p_2 located at a frequency slightly higher than that of the output filter pole.

$$\omega_{p2} \approx -\frac{nI_{OUT}}{V_{OUT}C_1} = -\frac{n}{R_{OUT}C_1} \quad (8)$$

where C_1 is the output capacitor, R_{OUT} is the equivalent load resistance and n (depending on duty ratio, slope compensation, frequency and passive components) is usually between 1 and 2.

If C_1 is ceramic, then its ESR zero can be neglected as it situates well beyond half the switching frequency. The low frequency gain of the control-to-output transfer function is simply the product of power stage transconductance and the equivalent load resistance (Figure 11).

The transfer functions of the feedback network and the error amplifier are:

$$\frac{v_{FB}}{v_{OUT}} = \left(\frac{R_2}{R_1+R_2}\right)\left[\frac{1+sC_{11}R_1}{1+s(R_1||R_2)C_{11}}\right] \quad (9)$$

and

$$\frac{v_{COMP}}{v_{FB}} \approx \frac{G_{MA}R_O(1+sC_5R_5)}{(1+sC_5R_O)\cdot(1+sC_6R_5)} \quad (10)$$

provided that $C_5 >> C_6$ and $R_O >> R_5$.

In Equation (10), C_5 forms a low frequency pole p_1 with the output resistance R_O of the error amplifier and C_6 forms a high frequency pole p_3 with R_5:

$$R_O = \frac{\text{Amplifier Open Loop Gain}}{\text{Transconductance}} = \frac{53\text{dB}}{280\mu\Omega^{-1}} = 1.6\text{M}\Omega$$

$$\omega_{p1} = -\frac{1}{R_OC_5}$$

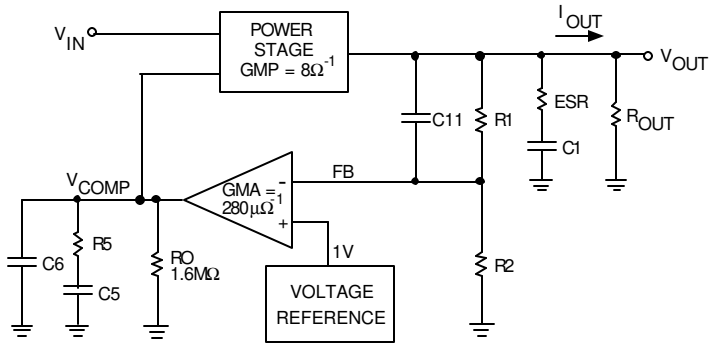


Figure 10. Simplified Control Loop Equivalent Circuit

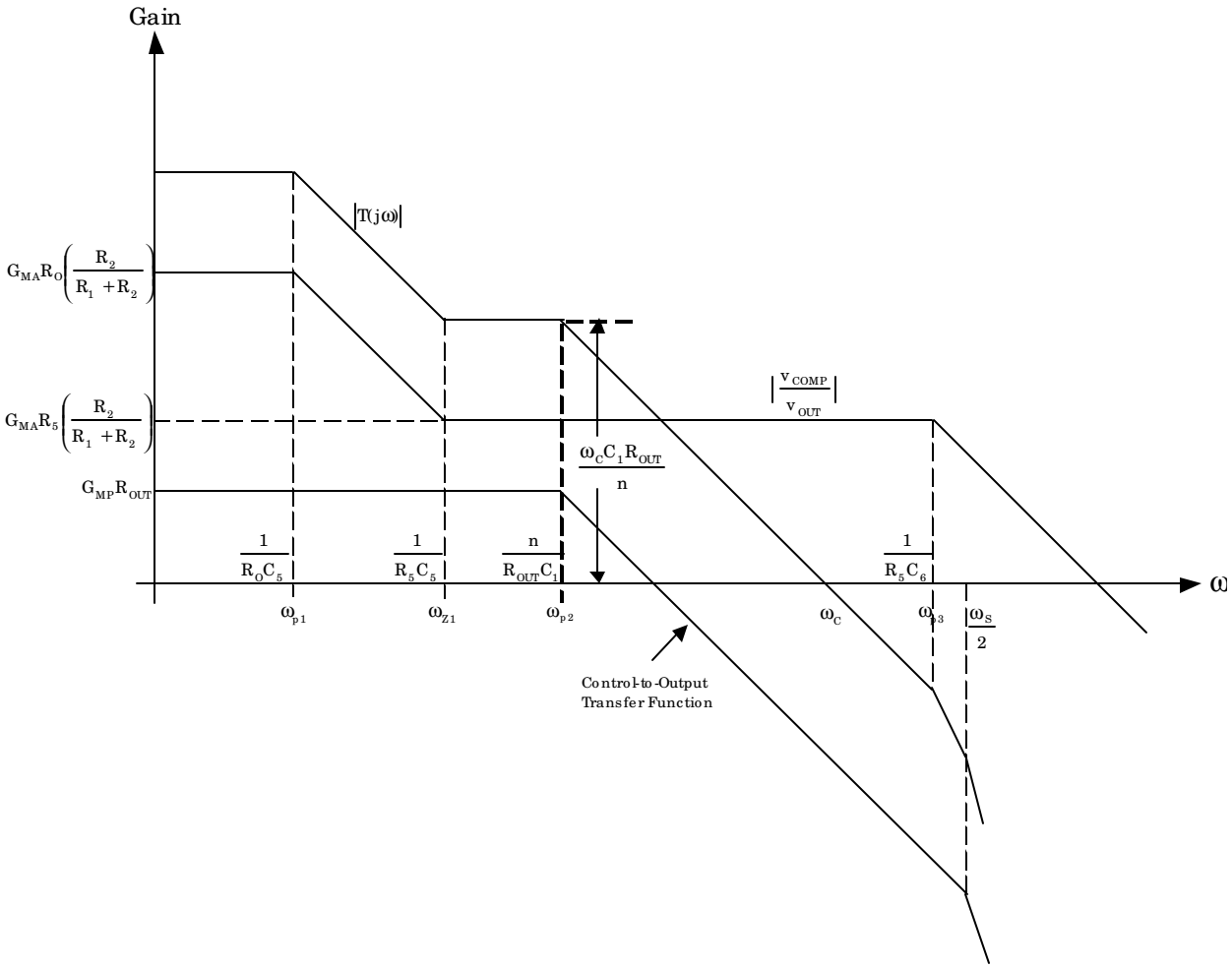


Figure 11. Bode Plots of Control-to-Ouput, Output-to-Control and the Overall Loop Gain. Control-to-output transfer function is shown with two poles near half the switching frequency ω_S.

$$\omega_{p3} = -\frac{1}{R_5 C_6}$$

In addition C_5 and R_5 form a zero with angular frequency:

$$\omega_{Z1} = -\frac{1}{R_5 C_5}$$

The output-to-control transfer function $\frac{V_{COMP}}{V_{OUT}} = \frac{V_{COMP}}{V_{FB}} \cdot \frac{V_{FB}}{V_{OUT}}$ is also shown in Figure 11. Its mid-band gain (between z_1 and p_3) is $G_{MA} R_5 \left(\frac{R_2}{R_1 + R_2} \right)$. The overall loop gain T(s) is the product of the control-to-output and the output-to-control transfer functions. To simplify $|T(j\omega)|$ Bode plot, the feedback network is assumed to be resistive. If the overall loop gain is to cross 0dB at one tenth of the switching frequency ($\omega_C = \frac{\omega_S}{10} = \frac{\pi f}{5}$) at –20dB/decade, then its mid-band gain (between z_1 and p_2) will be

$$\frac{\omega_C}{\omega_{p2}} = \frac{\frac{\omega_S}{10}}{\frac{n}{C_1 R_{OUT}}} = \frac{\omega_S C_1 R_{OUT}}{10n}$$

This is also equal to $G_{MP} R_{OUT} G_{MA} R_5 \left(\frac{R_2}{R_1 + R_2} \right)$. Therefore

$$G_{MP} R_{OUT} G_{MA} R_5 \left(\frac{R_2}{R_1 + R_2} \right) = \frac{\omega_S C_1 R_{OUT}}{10n}.$$

Re-arranging,

$$R_5 = \left(1 + \frac{R_1}{R_2} \right) \frac{\omega_S C_1}{10 n G_{MP} G_{MA}} \qquad (11)$$

ω_{z1} is shown to be less than ω_{p2} in Figure 11. Making $\omega_{z1} = \frac{\omega_C}{6} = \frac{\omega_S}{60}$ gives a first-order estimate of C_5:

$$C_5 \approx \frac{60}{\omega_S R_5} \qquad (12)$$

Notice that R_5 determines the mid-band loop gain of the converter. Increasing R_5 increases the mid-band gain and the crossover frequency. However it reduces the phase margin. C_6 is a small ceramic capacitor to roll off the loop gain at high frequency. Placing p_3 at about $\frac{\omega_S}{2}$ gives:

$$C_6 \approx \frac{1}{\pi f R_5} \qquad (13)$$

Computed R_5, C_5 and C_6 can indeed result in near optimal load transient responses in over half of the applications. However in other cases empirically determined compensation networks based on optimized load transient responses may differ from those calculated by a factor of 3. Therefore checking the transient response of the converter is imperative. Starting with calculated R_5, C_5 and C_6 (using n=1 in Equations (11)-(13)), apply the largest expected load step to the converter at the maximum operating V_{IN}. Observe the load transient response of the converter while adjusting R_5, C_5 and C_6. Choose the largest R_5, the smallest C_5 and C_6 so that the inductor current waveform does not show excessive ringing or overshoot.

Feedforward capacitor C_{11} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{11} will be more effective if $R_1 >> R_1 || R_2$.

Example: Determine the compensation components for the 550kHz 12V to 3.3V converter in Figure 13(a).

For the converter, $\omega_S = 3.5 \text{Mrads}^{-1}$, $I_{OUT(MAX)} = 2\text{A}$ and $C_1 = 22\mu\text{F}$. n is assumed to be 1 in (11) and (12).

$$R_5 = \left(1 + \frac{30.1k}{13k}\right)\frac{3.5\times10^{6}\cdot22\times10^{-6}}{10\cdot(1)\cdot(8)\cdot(2.8\times10^{-4})}$$
$$= 11.3k\Omega$$

$$C_5 \approx \frac{60}{11.3k\cdot2\pi\cdot5.5\times10^{5}} = 1.5nF$$

$$C_6 \approx \frac{1}{\pi\cdot(550\times10^{3})\cdot(11.3\times10^{3})} \approx 47pF$$

Bench measurement shows that compensation components computed from our simplified linear model give very good load transient response for the converter.

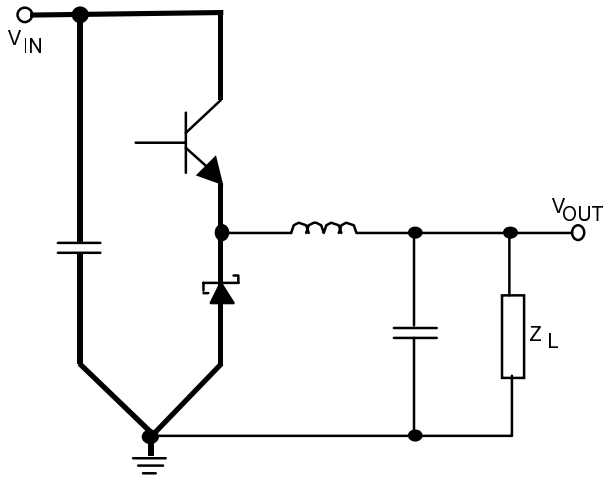


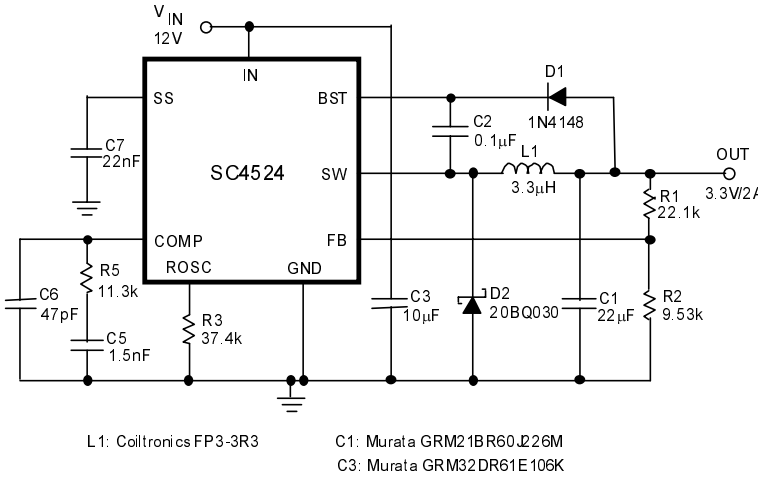
Figure 12. Fast Switching Current Paths in a Buck Regulator. Minimize the size of this loop to reduce parasitic trace inductance.

Board Layout Considerations

In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry discontinuous currents with high $\frac{di}{dt}$ (Figure 12). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switches are already integrated within the SC4524, connecting the anodes of both freewheeling diodes close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitors should be placed close to the VIN pin. Shortening the traces of the SW and BST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

The exposed pad should be soldered to a large analog ground plane as the analog ground copper acts as a heat sink for the device. To ensure proper adhesion to the ground plane, avoid using vias directly under the device.

Typical Application Circuit



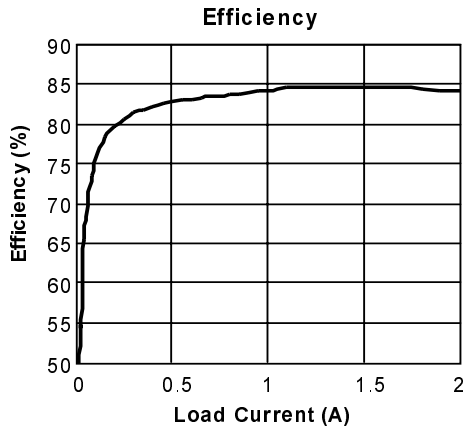


Figure 13(a). 550kHz 12V to 3.3V/2A step down converter.

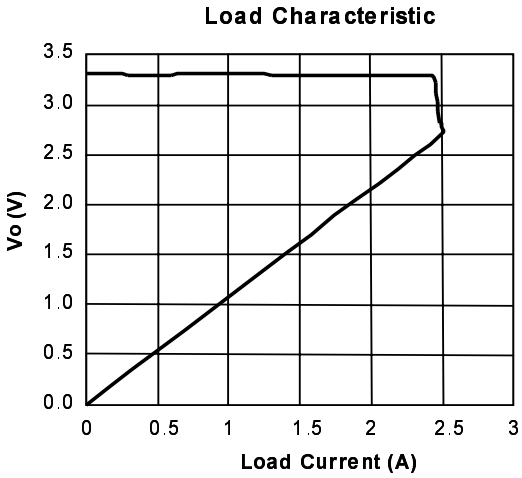


Figure 13(b). Load characteristic.

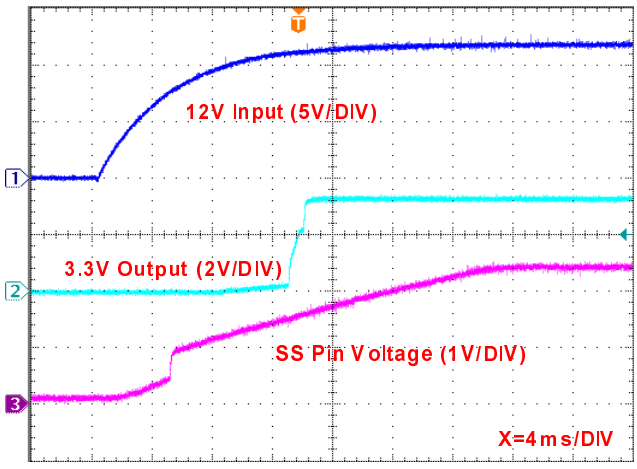


Figure 13(c). 12VIN start-up transient at 2A load.

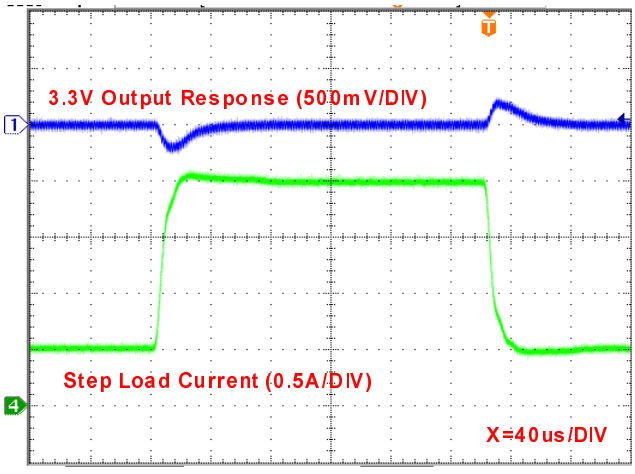
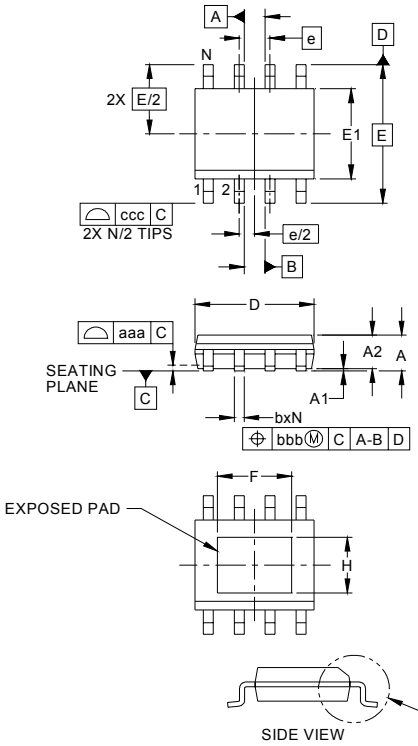


Figure 13(d). 0.5A to 2A step load transient response.

Outline Drawing - SOIC-8 EDP

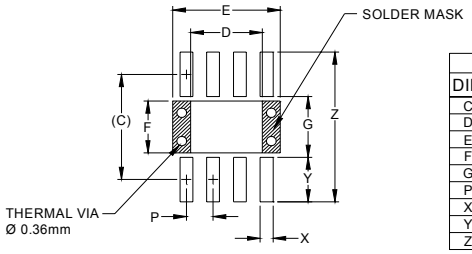


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.116	.120	.130	2.95	3.05	3.30
H	.085	.095	.099	2.15	2.41	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

Land Pattern - SOIC-8 EDP



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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