



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### POWER MANAGEMENT

#### Description

The SC4806 is a double ended, high speed, highly integrated PWM controller optimized for applications requiring minimum space. The device is easily configurable for current mode or voltage mode operation and contains all the control circuitry required for isolated applications, where a secondary side error amplifier is used.

Designed for simplicity, the SC4806 is fully featured and requires only a few external components. It features a programmable frequency up to 1MHz, external programmable soft start, pulse-by-pulse current limit and over current protection for both voltage and current modes, as well as a line monitoring input with hysteresis to reduce stress on the power components. A ramp pin allows for slope compensation to be programmed by external resistors for current mode. This also allows for operation in voltage mode with voltage feed forward.

A unique oscillator is utilized which allows two SC4806 to be synchronized together and work out-of-phase. This feature minimizes the input and output ripples, and reduces stress and size on input/output filter components. The outputs are configured for push-pull format, dead time between the 2 outputs is programmable depending on the size of the timing components.

The SC4806 features a turn on threshold of 8 volts . The device is available at a MLP-12 package.

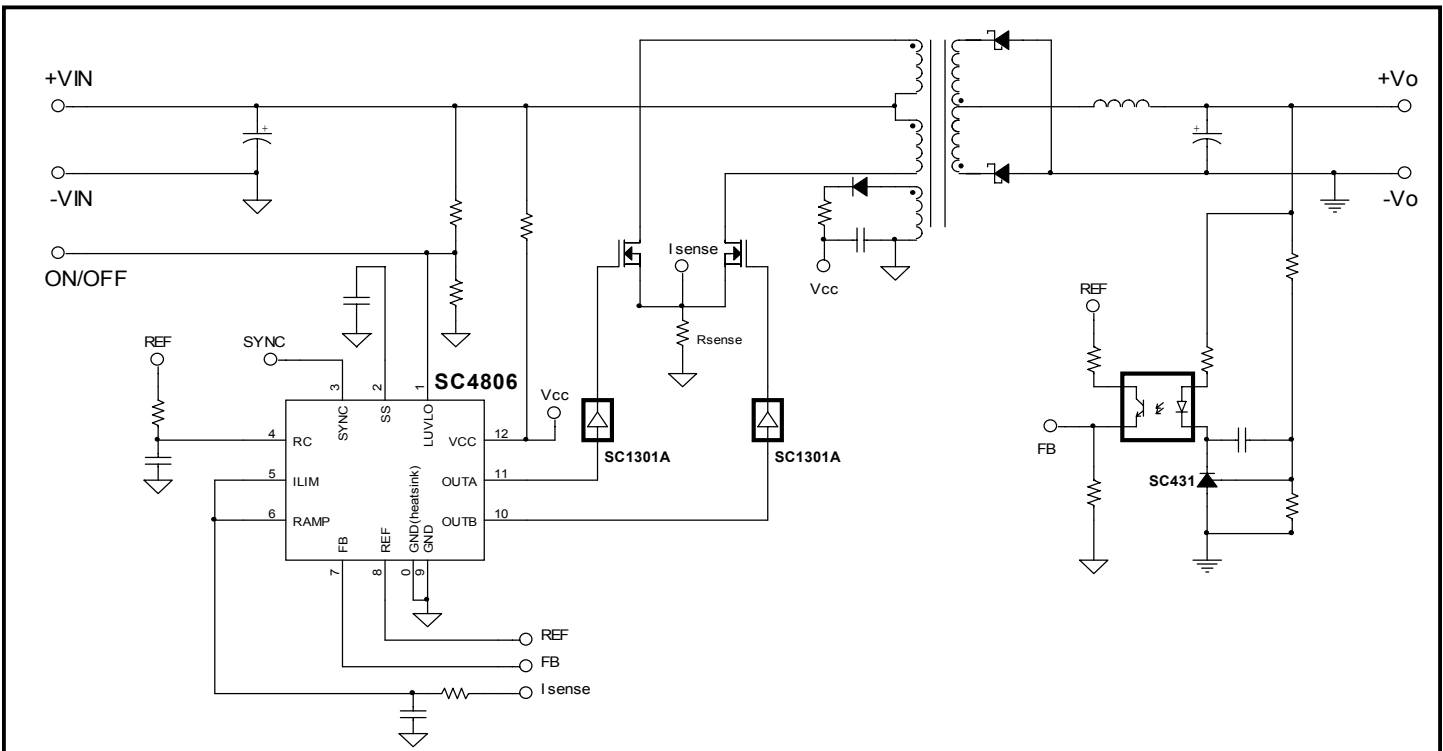
#### Features

- ◆ 90  $\mu$ A starting current
- ◆ Pulse-by-pulse current limit for both voltage/current modes
- ◆ Programmable operating frequency up to 1MHz
- ◆ Programmable external soft start
- ◆ Programmable line undervoltage lockout
- ◆ Programmable external slope compensation
- ◆ Over current shutdown with separate pin
- ◆ Dual output drive stages on push-pull configuration
- ◆ Programmable mode of operation (peak current mode or voltage mode)
- ◆ External frequency synchronization
- ◆ Bi-phase mode of operation
- ◆ Lead free MLP-12 package, WEEE and RoHS compliant
- ◆ -40 to 105  $^{\circ}$ C operating temperature

#### Applications

- ◆ Telecom equipment and power supplies
- ◆ Networking power supplies
- ◆ Industrial power supplies
- ◆ Push-pull converter
- ◆ Half bridge converter
- ◆ Full bridge converter
- ◆ Isolated VRMs

#### Typical Application Circuit



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter                                 | Symbol        | Maximum                     | Units |
|---|---------------|-----------------------------|-------|
| Supply Voltage                            | $V_{CC}$      | -0.5 to 18                  | V     |
| Supply Current                            | $I_{CC}$      | 20                          | mA    |
| SYNC, RC,RAMP, LUVLO, REF, ILM, SS to GND |               | -0.5 to 7                   | V     |
| FB to GND                                 | $V_{FB}$      | -0.5 to ( $V_{REF} + 0.5$ ) | V     |
| REF Current                               | $I_{REF}$     | 10                          | mA    |
| OUTA/OUTB to GND                          | $V_{OUTA/B}$  | -0.5 to 18                  | V     |
| OUTA/OUTB Source Current (peak)           | $I_{source}$  | -250                        | mA    |
| OUTA/OUTB Sink Current (peak)             | $I_{sink}$    | 250                         | mA    |
| Thermal Resistance, Junction to Ambient   | $\theta_{JA}$ | 32                          | °C/W  |
| Thermal Resistance, Junction to Case      | $\theta_{JC}$ | 3                           | °C/W  |
| Junction Temperature                      | $T_J$         | -55 to 150                  | °C    |
| Storage Temperature Range                 | $T_{STG}$     | -65 to 150                  | °C    |
| Peak IR Reflow Temperature 10 - 40s       | $T_{PKG}$     | 260                         | °C    |
| ESD Rating (Human Body Model)             | ESD           | 2                           | kV    |

**Electrical Characteristics**

Unless specified:  $V_{CC} = 12V$ ;  $CL = 100pF$ ;  $T_A = -40^{\circ}C$  to  $105^{\circ}C$

| Parameter                                  | Test Conditions   | Min  | Typ  | Max  | Units   |
|--|---|------|------|------|---------|
| <b>VCC Supply</b>                          |   |      |      |      |         |
| $V_{CC}$ Start Threshold                   |   | 7.4  | 8    | 8.6  | V       |
| Hysteresis                                 |   | 1.17 | 1.5  | 1.83 | V       |
| Startup Current                            | $V_{CC} < \text{start threshold}$                         |      |      | 150  | $\mu A$ |
| Operating Supply Current                   | $FB = 0V, RAMP = 0V$                                      |      |      | 7    | mA      |
| VCC Zener Shunt Voltage                    | $I_{DD} = 10mA$   | 16   |      |      | V       |
| <b>PWM</b>                                 |   |      |      |      |         |
| Maximum Duty Cycle                         | $F_{osc} = 50kHz, FB = 5V,$<br>Measured at OUTA or OUTB   | 48   | 49   | 50   | %       |
| Minimum Duty Cycle                         | $F_{osc} = 50kHz, FB = 1.5V,$<br>Measured at OUTA or OUTB |      |      | 0    | %       |
| <b>Current Sense/Limit</b>                 |   |      |      |      |         |
| ILM Cycle by Cycle Current Limit Threshold |   | 450  | 525  | 600  | mV      |
| ILM to Output Delay                        |   |      | 50   |      | ns      |
| ILM Auto Restart Over Current Threshold    |   | 750  | 850  | 950  | mV      |
| FB to RAMP Offset                          |   | 1.20 | 1.40 | 1.60 | V       |

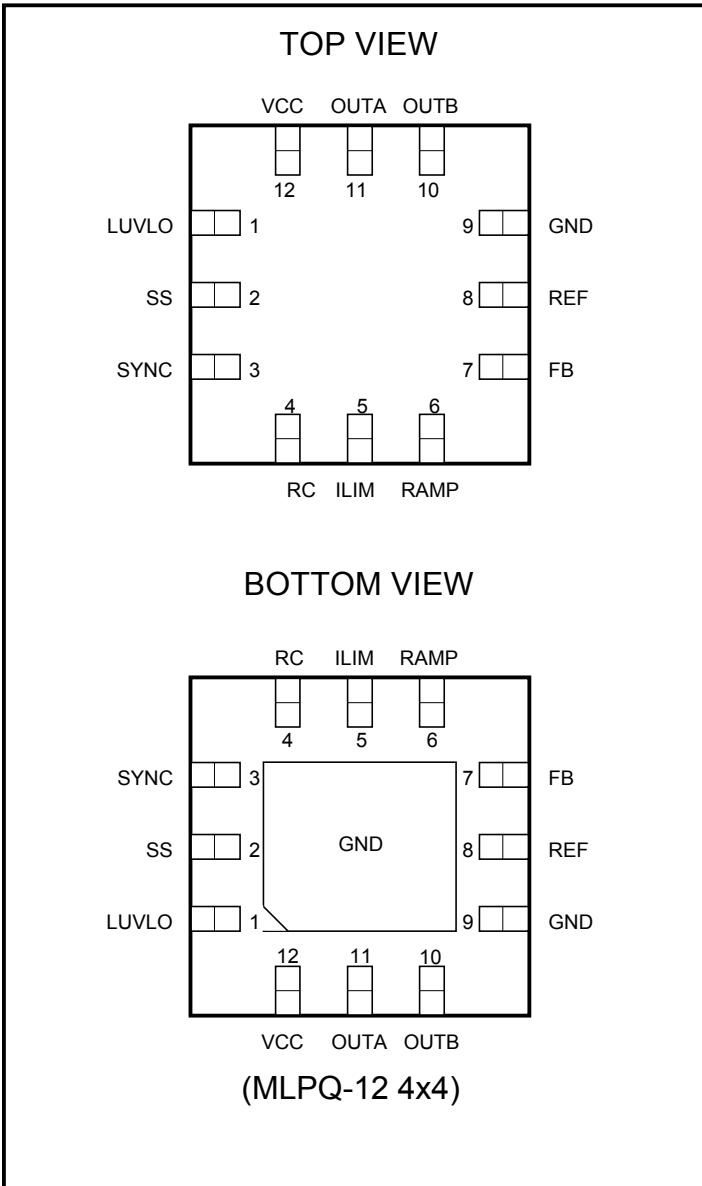
**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified: VCC = 12V; CL = 100pF; T<sub>A</sub> = -40°C to 105°C

| Parameter   | Test Conditions                                   | Min   | Typ          | Max                   | Unit  |
|---|---|-------|--------------|-----------------------|-------|
| <b>Line Under Voltage Lockout</b>                     |   |       |              |                       |       |
| Start Threshold                                       | R <sub>high</sub> = 14kΩ, R <sub>low</sub> = 10kΩ | -3%   | VREF         | +3%                   | V     |
| Hysteresis  | R <sub>high</sub> = 14kΩ, R <sub>low</sub> = 10kΩ |       | 5.5% of VREF |                       | mV    |
| <b>Soft Start</b>                                     |   |       |              |                       |       |
| Internal Soft Start Charge Current (I <sub>SS</sub> ) | V <sub>SS</sub> = 1.5V                            | 25    | 35           | 45                    | μA    |
| Internal Discharge Current                            | V <sub>SS</sub> = 1.5V                            |       | 10           |                       | μA    |
| <b>Oscillator</b>                                     |   |       |              |                       |       |
| Oscillator Frequency                                  | R <sub>osc</sub> = 10kΩ, C <sub>osc</sub> = 200pF | 450   | 500          | 550                   | KHz   |
| Oscillator Ramp                                       |   |       | VREF/2 +0.25 |                       | V     |
| Oscillator Fall Time                                  | Guaranteed by characterization                    |       | 200          | 250                   | ns    |
| RC pin to GND Capacitance                             |   |       | 22           |                       | pF    |
| Oscillator Frequency Range                            | Guaranteed by characterization                    | 50    |              | 1000                  | KHz   |
| <b>Sync/CLOCK</b>                                     |   |       |              |                       |       |
| Clock SYNC Threshold                                  |   |       | 1.75         |                       | V     |
| Sync Frequency Range                                  | Guaranteed by characterization                    |       |              | F <sub>OSC</sub> *1.3 | KHz   |
| <b>Bandgap</b>  |   |       |              |                       |       |
| Reference Voltage                                     |   | 4.75  | 5.0          | 5.25                  | V     |
| Reference Load Regulation                             | I <sub>REF</sub> = 0 - 5mA                        |       | 10           |                       | mV/mA |
| Reference Line Regulation                             | V <sub>CC</sub> = 8.5V to 15V                     |       | 0.3          |                       | mV/V  |
| <b>Output</b>   |   |       |              |                       |       |
| OUT Low Level   |   |       | 0.5          | 0.7                   | V     |
| OUT High Level  | V <sub>CC</sub> = 12V                             | 10.85 | 11.20        |                       | V     |
| Rise Time   | Load 1nF  |       | 35           |                       | ns    |
| Fall Time   | Load 1nF  |       | 35           |                       | ns    |
| Minimal Dead Time                                     |   |       | 200          | 250                   | ns    |
| <b>Thermal Shutdown</b>                               |   |       |              |                       |       |
| Thermal Shutdown Threshold T <sub>SD</sub>            |   |       | 175          |                       | °C    |
| Thermal Shutdown Hysteresis                           |   |       | 15           |                       | °C    |

**POWER MANAGEMENT**

**Pin Configuration**



**Ordering Information**

| DEVICE <sup>(1)</sup>      | PACKAGE | Temp. Range (T <sub>j</sub> ) |
|----------------------------|---------|-------------------------------|
| SC4806MLTRT <sup>(2)</sup> | MLPQ-12 | -40°C to 105°C                |

Notes:

- (1) Only available in tape and reel packaging. A reel contains 3000 devices.
- (2) Lead free product. This product is fully WEEE and RoHS compliant.

**POWER MANAGEMENT**
**Pin Descriptions**
**LUVLO (Pin 1):**

Line undervoltage lockout pin. An external resistive divider from the Input supply will program the undervoltage lockout level. The external divider should be referenced to the quiet analog ground. During the LUVLO, the driver outputs are disabled. This pin can also function as an Enable/Disable.

**SS (Pin 2):**

An internal 35µA current source charges the external capacitor connected to this pin. This pin is connected to one of the inputs of the PWM comparator. When the voltage on this SS pin increases, but less than 1/3 of the feedback voltage  $V_{FB}$ , the pulse width of OUTA and OUTB gradually increases to achieve soft start. As the output voltage increases and feedback loop enters regulation, the PWM modulator is controlled by  $V_{FB}$ . At normal operation, the voltage at SS pin is clamped at Vref.

When the Over Current is tripped, both OUTA and OUTB are pulled low after a typical time delay (Typ. 100ns). At the same time, the SS cap is gradually discharged via an equivalent 10µA internal current source. When the voltage on SS pin is dropped below 0.8V, a new SS cycle is initiated while the SS cap is charged with 35µA again.

The internal thermal protection circuit monitors the die temperature. If the temperature exceeds 175°C, the controller is completely shutdown. When the temperature is dropped below 160°C, defined by the hysteresis, the controller re-starts with soft start process.

**SYNC (Pin 3):**

SYNC is a positive edge triggered input with a threshold set to 1.75V. In a single controller operation, SYNC could be grounded or connected to an external synchronization clock within the SYNC frequency range. In Bi-Phase operation mode SYNC pins could be connected to the Cosc (Timing Capacitors) of the other controller. This will force an out-of-phase operation (see Application Information part).

**RC (Pin 4):**

The oscillator programming pin. The oscillator should be referenced to a stable reference voltage for an accurate and stable frequency. Only two components are required to program the oscillator, a resistor (tied to Vref and RC), and a capacitor (tied to the RC and GND). The following formula can be used for a close approximation of the oscillator frequency.

$$F_{OSC} \cong \frac{1}{R_{OSC} C_{TOT}}$$

where:

$$C_{TOT} = C_{OSC} + C_{SC4806} + C_{Circuit}$$

$$C_{SC4806} \cong 22\text{pF}$$

The recommended range of timing resistors is between 10kohm and 200kohm and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10kohm should be avoided.

Refer to layout guidelines in Application Information section to achieve best results.

**ILim (Pin 5):**

The current signal from a sense resistor is applied to peak current and overcurrent comparators through ILM pin.

Under normal operation condition, the comparators are not triggered. When the current signal sensed at ILM pin exceeds the first threshold – pulse-by-pulse current limit, the corresponding on-time is terminated for the remainder of the switching cycle. In this case, the circuit output voltage loses regulation even though it continues to provide full load current.

When the load current continuously increases and the sensed signal at ILM pin reaches the second threshold - over current limit, the controller turns off both OUTA and OUTB. At the same time, the SS cap is discharged with equivalent 10uA current source. When the voltage at SS pin is below 0.5V, the controller initiates re-start. The pins Ramp and ILM are discharged by the internal FETs at the end of each switching cycle.

**POWER MANAGEMENT****Pin Descriptions (Cont.)****Ramp (Pin 6):**

The signal at this pin will be used as the PWM ramp signal that will be compared to the FB to achieve regulation. The modes of operation can be programmed depending on how this pin is configured (For more details see Application section).

For voltage mode control, the PWM ramp is generated via external RC circuit connected from a voltage source to the Ramp pin. Connection to a fixed voltage source (REF) will provide a constant peak ramp with a frequency set by the internal oscillator frequency programmed at the RC pin. Connection to a variable source such as the VIN will provide the added benefit of the feed forward function enhancing the converter static and dynamic performance.

For Current mode control the current information from the ILim pin can be directly connected to the Ramp pin without the need for the external RC circuit at the Ramp pin.

If current mode of operation with slope compensation is required, an external resistor connected from the ILim pin to the Ramp pin will provide the slope compensation. The percentage of the slope compensation will be inversely proportional to the value of the resistor (the higher resistor lower slope compensation, the lower resistor higher slope compensation). 1/3 of external feedback signal to FB pin by an internal 3 to 1 resistor divider compares to the combined current signal to generate PWM control signal.

**FB (Pin 7):**

The inverting input to the PWM comparator through an internal 3 to 1 resistor divider. Stray inductances and parasitic capacitance should be minimized by utilizing ground planes and correct layout guidelines.

**REF (Pin 8):**

Bandgap reference output. It is recommended by placing a minimum 2.2uF low ESR capacitor right at the pin.

**GND (Pin 9):**

Device power and analog ground. The exposed paddle area on the back of the package must be connected to the GND (pin9). Careful attention should be paid to the layout of the ground planes.

**OUTB (Pin 10) and OUTA (Pin 11):**

Out of phase gate drive stages. The driver's peak source and sink current drive capability of 100mA, enables the use of an external MOSFET driver or a NPN/PNP transistor totem pole driver.

The oscillator RC network programs the oscillator frequency, which is twice the OUTA/OUTB frequency. To insure that the outputs do not overlap, a dead time can be generated between the two outputs by sizing the oscillator timing capacitor (see Application Information section).

**VCC (Pin 12):**

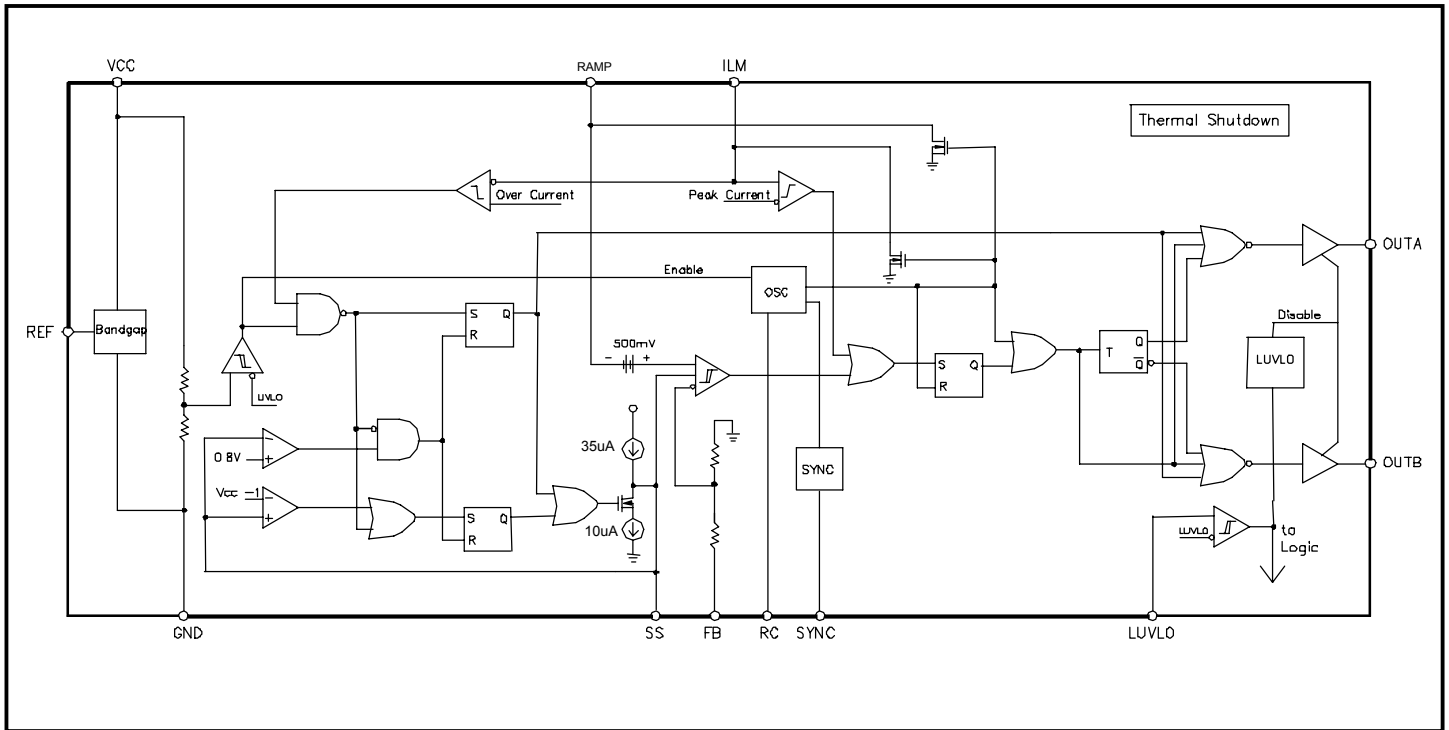
The supply input for the device. Once VCC has exceeded the UVLO limit, the internal reference, oscillator, drivers and logic are powered up. A low ESR capacitor, should be placed right at the pin to minimize noise problems. It is recommended that the  $V_{CC}$  rising rate during start-up be smaller than 10V/mS.

**THERMAL PAD:**

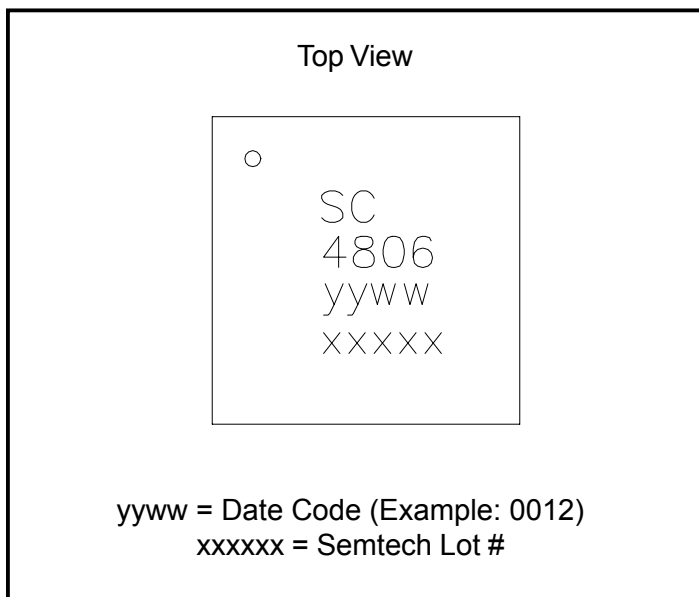
Pad for heatsinking purposes. Connect to ground plane using multiple thermal vias. Not connected internally.

**POWER MANAGEMENT**

**Block Diagram**



**Marking Information**





**POWER MANAGEMENT****Application Information**

SC4806 is a versatile double ended, high speed, low power, pulse width modulator optimized for applications requiring minimum space.

The device contains all of control and drive circuitry required for isolated or non isolated power supplies where an external error amplifier is used. A fixed oscillator frequency (up to 1MHz) can be programmed by an external RC network.

SC4806 is a peak current or voltage mode controller, depending on the amount of slope compensation, programmable with only one external resistor. The cycle by cycle peak current limit prevents core saturation when a transformer is used for isolation while the auto-restart over-current circuitry initiates the soft-start cycle.

SC4806 dual output drive stages are arranged for double ended configurations. Both outputs switch at half the oscillator frequency using a toggle flip flop. The dead time between the two outputs is programmable depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

SC4806 also provides flexibility with programmable LUVLO thresholds, with built-in hysteresis.

**POWER SUPPLY**

A single supply, VCC is used to provide the bias for the internal reference, oscillator, drivers, and logic circuitry of SC4806.

**PWM CONTROLLER**

SC4806 is a double ended PWM controller that can be used in voltage or current mode applications. The oscillator frequency is programmed by a resistor and a capacitor network connected to an external reference provided by the SC4806. The two outputs, OUTA and OUTB, are 180 degrees out-of-phase and run at half of the oscillator frequency.

An external error amplifier will provide the error signal to the FB pin of the SC4806. The current limit input and external slope compensation are provided separately via the ILIM and RAMP pins. The current limit signal from a sense resistor or a current sense transformer is used for the peak current and auto-restart overcurrent comparators.

To generate PWM control signal, 1/3 of external feedback signal to FB pin by an internal 3 to 1 resistor divider compares to the combined current signal if an external resistor is connected from ILIM to RAMP. The value of the resistor will determine the level of slope compensation. The slope signal to RAMP is generated from either input voltage or VREF with external RC. Voltage mode of operation can be achieved if the slope signal is only used.

Two levels of undervoltage lockout are also available. The LUVLO (line under voltage lockout) pin via an external resistive divider programs input voltage turn-on level. During the LUVLO, the driver outputs are disabled and the soft-start is reset.

The VCC UVLO (under voltage lockout) determines VCC voltage turn-on level. Once VCC exceeds the UVLO limit, the internal reference, oscillator, drivers and logic are powered up.

SYNC is a positive edge triggered input with a threshold set to 1.75V. By connecting an external control signal to the SYNC pin, the internal oscillator frequency will be synchronized to the positive edge of the external control signal. In a single controller operation, SYNC should be grounded or connected to an external synchronization clock within the SYNC frequency range. In the Bi-phase operation mode, a very unique oscillator is utilized to allow two SC4806s to be synchronized together and work out of phase. This feature is set up by simple connection of the SYNC input of one part to the RC pin of the other. The master oscillator forces the two PWMs to operate out of phase. This feature minimizes the input and output ripples, and may reduce input and output capacitors.

**VCC UNDER VOLTAGE LOCK OUT**

Depending on the application and the voltages available, the SC4806 (UVLO = 8V) can be used to provide the VCC undervoltage lock out function to ensure the converters controlled start up.

Before the VCC UVLO has been reached, the internal reference, oscillator, OUTA/OUTB drivers, and logic are disabled.

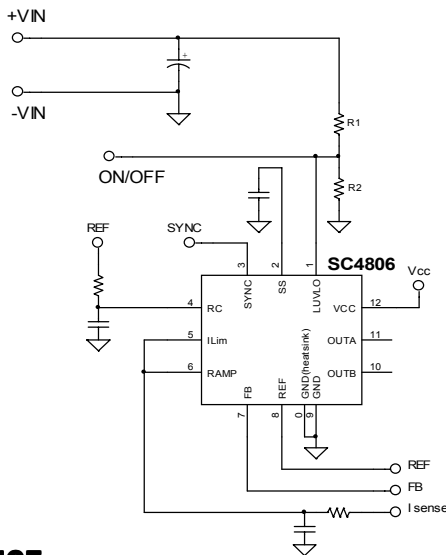
**LINE UNDER VOLTAGE LOCK OUT**

The SC4806 also provides a line undervoltage (LUVLO = Vref) function. The LUVLO pin is programmed via an ex-

**POWER MANAGEMENT**
**Application Information (Cont.)**

ternal resistor divider connected as shown below. The actual start-up voltage can be calculated by using the equation below:

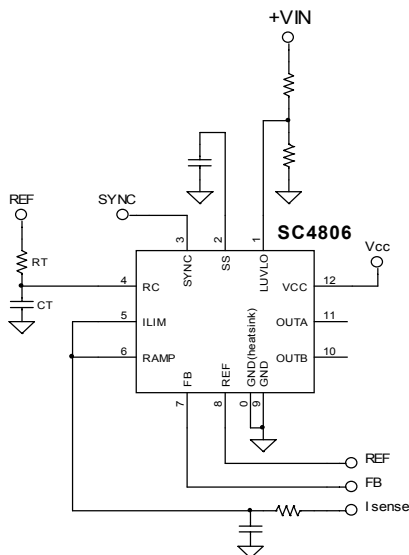
$$V_{\text{Startup}} = V_{\text{REF}} \times \left(1 + \frac{R1}{R2}\right)$$


**REFERENCE**

A 5V reference voltage is available that can be used to source a typical current of 5mA to the external circuitry. The Vref can be used to provide the oscillator RC network with a regulated bias.

**OSCILLATOR**

The oscillator frequency is set by connecting a RC network as shown below.



The oscillator has a ramp voltage of about Vref/2. The oscillator frequency is twice the frequency of the OUTA and OUTB gate drive controls.

The oscillator capacitor CT is charged from the Vref through RT. Once the RC pin reaches about Vref/2, the capacitor is discharged internally by the SC4806. It should be noted that larger capacitor values will result in a longer dead time during the down slope of the ramp. The following equation can be used as an approximation of the oscillator frequency and the Dead time:

$$F_{\text{OSC}} \cong \frac{1}{R_{\text{OSC}} C_{\text{TOT}}}$$

where:

$$C_{\text{TOT}} = C_{\text{OSC}} + C_{\text{SC4806}} + C_{\text{Circuit}}$$

$$C_{\text{SC4806}} \cong 22\text{pF}$$

$$T_{\text{deadtime}} \cong \frac{C_{\text{OSC}} \times V_{\text{REF}} \times 0.5}{3 \cdot 10^{-3}}$$

The recommended range of timing resistors is between 10 kohm and 200kohm, range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10 kohm should be avoided.

**SYNC/BI-Phase operation**

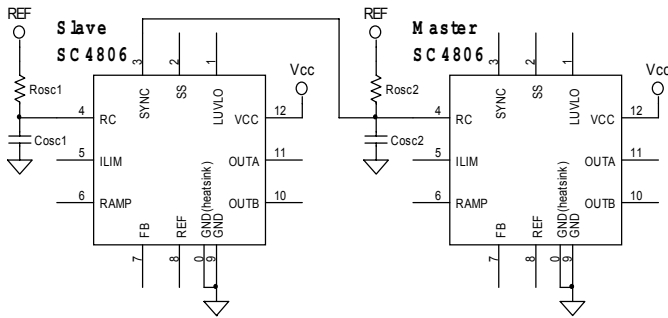
In noise sensitive applications where synchronization of the oscillator frequency to a reference frequency may be required, the SYNC pin can accept the external clock. By connecting an external control signal to the SYNC pin, the internal oscillator frequency will be synchronized to the positive edge of the external control signal. SYNC is a positive edge triggered input with a threshold set to 1.75V.

In a single controller operation, SYNC should be grounded or connected to an external synchronization clock within the SYNC frequency range.

In the Bi-phase operation mode a very unique oscillator is utilized to allow two SC4806's to be synchronized together and work out of phase. This feature is set up by a simple connection of the SYNC input to the RC pin of the other part. The master oscillator forces two PWMs to operate out of phase. This feature minimizes the input and output ripples, and may reduce input and output capacitors.

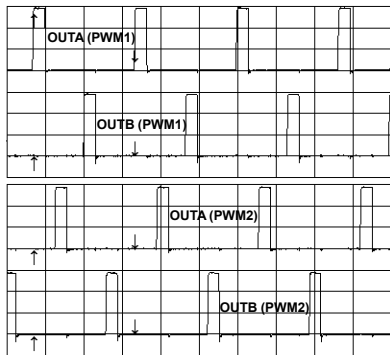
**POWER MANAGEMENT**

**Application Information (Cont.)**



The signal at the FB pin is then compared to the 3X signal from the current sense/ slope compensation RAMP pin. Matched out of phase signals are generated to control the OUTA and OUTB gate drives of the two phases. A single ramp signal is used to generate the control signals for both phases, hence achieving a tightly matched per phase operation.

Voltages below 1.5V at the FB pin, will produce a 0% duty cycle at the OUTA/OUTB gate drives. This offset is to provide enough head room for the opto coupler used in isolated applications.



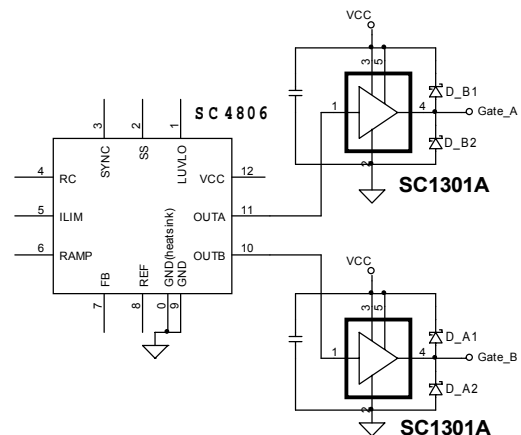
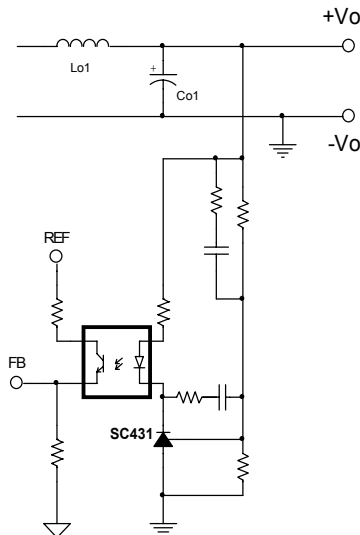
**GATE DRIVERS**

OUTA and OUTB are out of phase bipolar gate drive output stages, that are supplied from VCC and provide a peak source/sink current of about 100mA. Both stages are capable of driving the logic input of external MOSFET drivers or a NPN/PNP transistor buffer. The output stages switch at half the oscillator frequency. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This “dead time” between the two outputs, along with a slower output rise and fall time, insures that the two outputs can not be on at the same time. The dead time is programmable and depends upon the timing capacitor.

**FEED BACK**

The error signal from output of an external error amplifier such as SC431 or SC4431 is applied to the inverting input of the PWM comparator at the FB pin either directly or via an opto-coupler for the isolated applications. For best stability, keep the FB trace length as short as possible.

It should be noted that if high speed/high current drivers such as the SC1301 are used, careful layout guide lines must be followed in order to minimize stray inductance, which might cause negative voltages at the output of the drivers. This negative voltage can be clamped to a reasonable level by placing a small Schottky diode directly at the output of the driver as shown below:



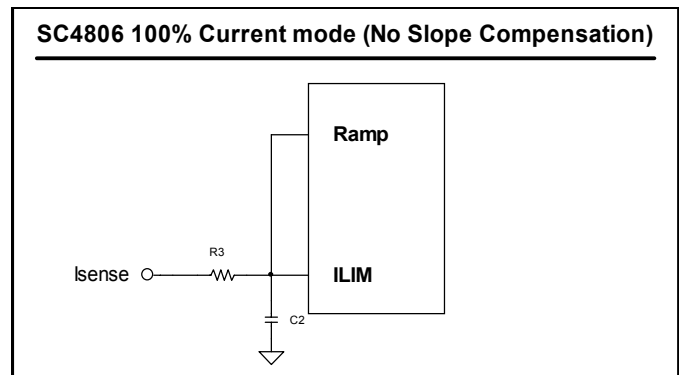
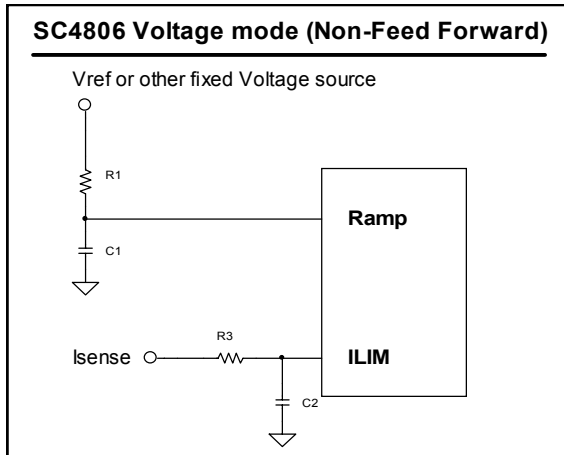
**POWER MANAGEMENT**

**Application Information (Cont.)**

**OPERATION MODE**

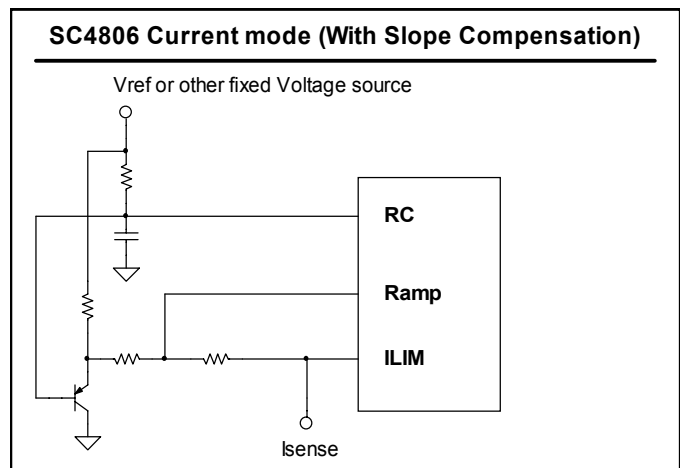
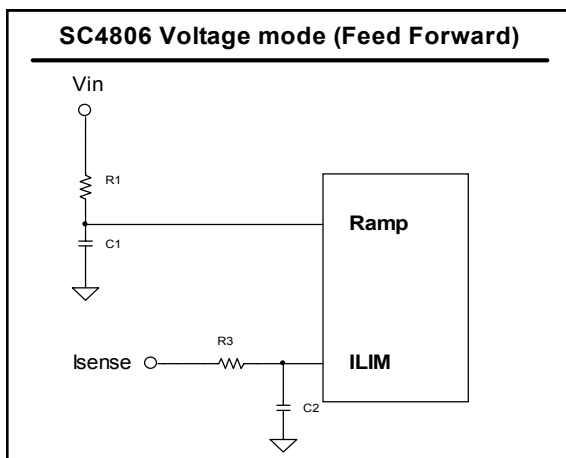
SC4806 can be configured in either voltage mode or current mode. In voltage mode, a ramp is externally generated by RC network. The R can be connected to Vref or other fixed voltage source as shown below. By comparing control signal to the ramp, PWM duty cycle is derived.

In current mode control, the ramp voltage is not derived artificially from a ramp generator. It is instead provided from a power converter inductor current by a current sensing transformer or resistor. Thus a second, inner control loop is formed by comparing the inductor current ramp to control voltage from outer voltage loop. Now the control voltage programs the inductor current via the inner loop and no longer controls the duty cycle directly. The current mode control corrects most of problems with direct duty cycle control in voltage mode. The chief advantage of the methods its inherent feed-forward characteristics and simplified loop dynamics. An added benefit is the reduction or elimination of transformer saturation problems in full-bridge or push-pull isolated converters. The current mode configuration with SC4806 is as shown below:



Voltage mode with feed-forward operation is implemented if the R is connected to input voltage as shown below. With this implementation, the ramp amplitude varies directly with input voltage. If control signal to FB is constant, the duty cycle varies inversely with input voltage. Thus the volt-second product,  $V_{in} * D$ , remains constant without any control change. Open loop line regulation better than direct duty cycle control as shown above. Good dynamic response is achieved with less closed loop gain required.

The current mode control limiting the peak inductor current results in circuit instability whenever the steady state duty cycle is greater than 0.5. An artificial slope has to be added to avoid such problem. Power transformer magnetizing current riding on the reflected inductor current acts to provide some slope compensation, but the amount is rather variable and indeterminate. The current mode with slope compensation is as shown below:



**POWER MANAGEMENT****Application Information (Cont.)****SOFT START**

During start up of the converter, the discharged output capacitor and the load current have large supply current requirements. To avoid this a soft start scheme is usually implemented where the duty cycle of the regulator is gradually increased from 0% until the soft start duration is elapsed.

SC4806 has soft start circuit with an external capacitor that limits the duty cycle for a duration approximated by the formula below. Also the soft start circuitry is activated if an over current condition occurs. After an over current condition, OUTA and OUTB are disabled and kept low. After the delay, the OUTA and OUTB are enabled while the soft start limits the duty cycle. If the over current condition persists, the soft start cycle repeats indefinitely.

**START UP SEQUENCE**

Initially during the power up, the SC4806 is in under voltage lock out condition. As the Vcc supply exceeds the UVLO limit of the SC4806, the internal reference, oscillator, and logic circuitry are powered up.

The OUTA and OUTB drivers are not enabled until the line under voltage lock out limit is reached. At that point, once the FB pin is above 1.5V, soft start circuitry starts the output drivers, and gradually increases the duty cycle from 0%.

As the output voltage starts to increase, the error signal from the error amplifier starts to decrease. If isolation is required, the error amplifier output can drive the LED of the opto isolator. The output of the opto is connected in a common emitter configuration with a pull-up resistor to a reference voltage connected to the FB pin of the SC4806. The voltage level at the FB pin provides the duty cycle necessary to achieve regulation.

If an over current condition occurs, the outputs are disabled and after a soft start delay time of about 100 $\mu$ s, the soft-start sequence mentioned above is repeated.

**LAYOUT GUIDELINES**

Careful attention to layout requirements are necessary for successful implementation of the SC4806 PWM controller.

High current switching is present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1) The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, such as the input capacitor and FET ground.

2) In the loop formed by the Input Capacitor(s) (Cin), the FET must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3) The connection between FETs and the Transformer should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) A SC4806 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin FET loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the VCC supply capacitor(s). Under no circumstances should GND be returned to a ground inside the Cin, Q1, Q2 loop. Avoid making a star connection be-

**POWER MANAGEMENT****Application Information (Cont.)**

tween the quiet GND planes that the SC4806 will be connected to and the noisy high current GND planes connected to the FETs.

6) The feed back connection between the error amplifier and the FB pin should be kept as short as possible. The GND connections should be connected to the quiet GND used for the SC4806.

7) If an Opto isolator is used for isolation, quiet primary and secondary ground planes should be used. The same precautions should be followed for the primary GND plane as mentioned in item 5 mentioned above. For the secondary GND plane, the GND plane method mentioned in item 4 should be followed.

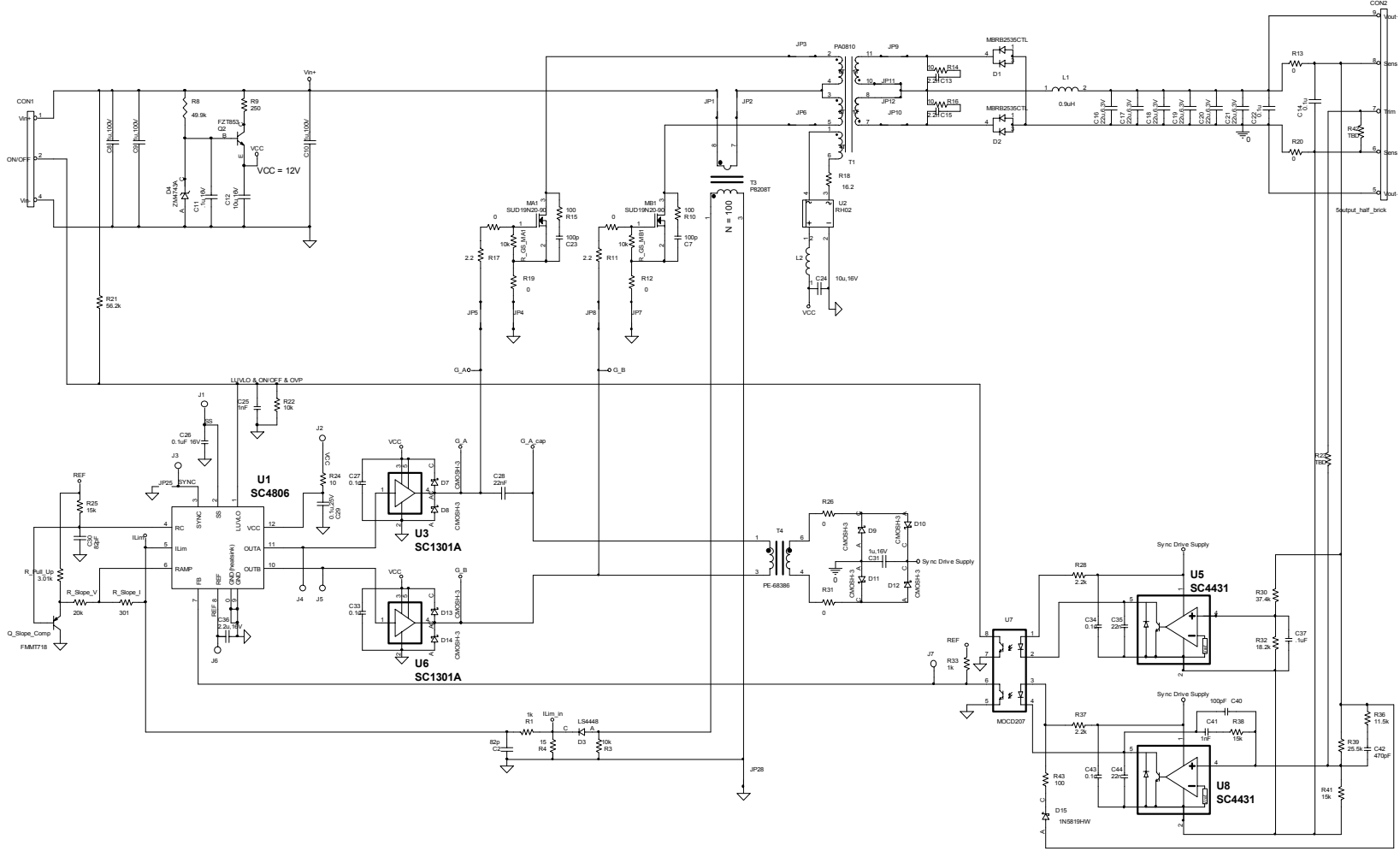
8) All the noise sensitive components such as LUVLO resistive divider, reference by pass capacitor, Vcc bypass capacitor, current sensing circuitry, feedback circuitry, and the oscillator resistor/capacitor network should be connected as close as possible to the SC4806. The GND return should be connected to the quiet SC4806 GND plane.

9) The connection from the OUTA and OUTB of the SC4806 should be minimized to avoid any stray inductance. If the layout can not be optimized due to constraints, a small Schottky diode may be connected from the OUTA/B pins to the ground directly at the IC. This will clamp excessive negative voltages at the IC. If drivers are used, the Schottky diodes should be connected directly at the IC from the output of the driver to the driver ground.

10) If the SYNC function is not used, the SYNC pin should be grounded at the SC4806 GND to avoid noise pick up.



## POWER MANAGEMENT Push Pull Evaluation Board Sch



**POWER MANAGEMENT**

**Evaluation Board Bill of Materials**

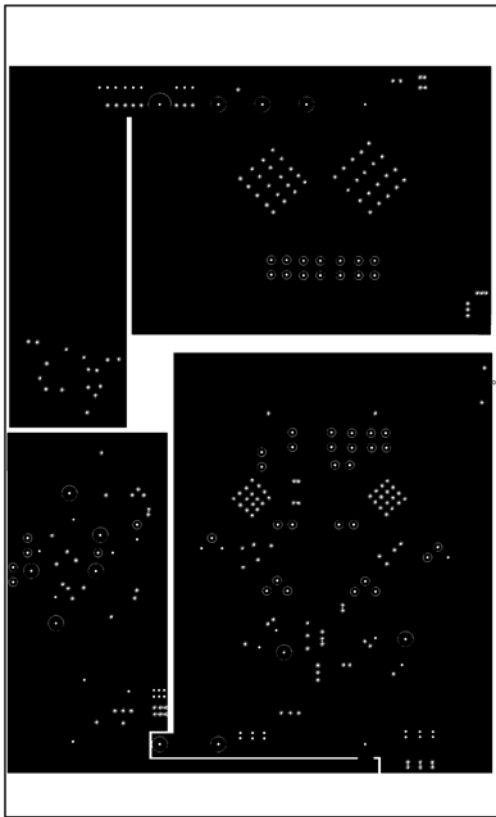
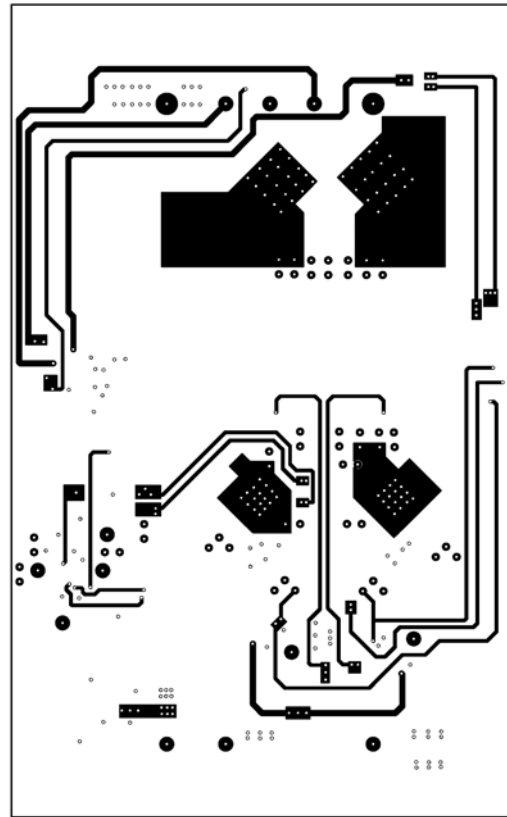
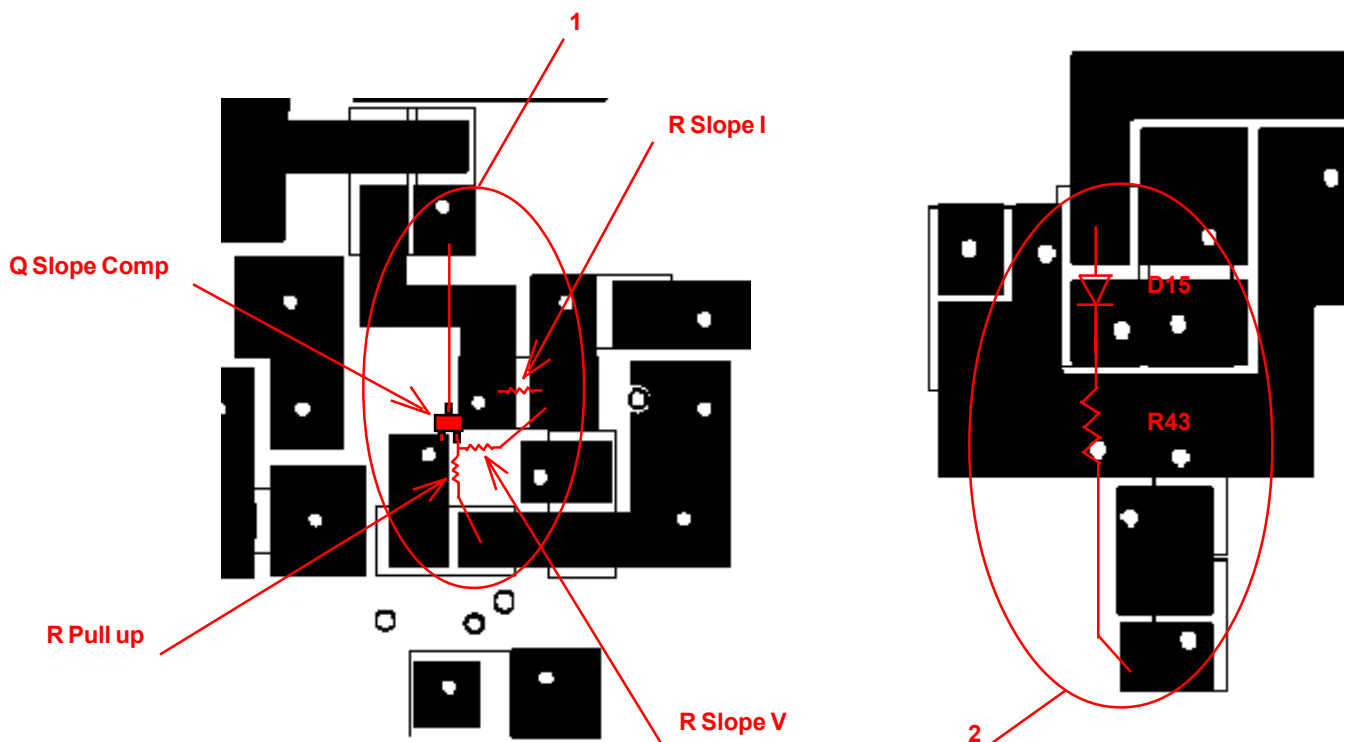
SC4806 Slope Compensation Current Mode Push Pull 3.3V 35W non Synchronous  
 SC4806EVB\_non\_sync Revision: 1.1

Bill Of Materials March 30,2005 11:27:17

| Item | Quantity | Reference  | Part               | Manufacturer #                  | Foot Print             |
|------|----------|--|--------------------|---------------------------------|------------------------|
| 1    | 1        | CON1   | 3input_half_brick  |                                 | CON\3INPUT_HALF_BRICK  |
| 2    | 1        | CON2   | 5output_half_brick |                                 | CON\5OUTPUT_HALF_BRICK |
| 3    | 1        | C2   | 82p                |                                 | SM/C_0805              |
| 4    | 2        | C23,C7   | 100p               |                                 | SM/C_1206              |
| 5    | 3        | C8,C9,C10  | 1u,100V            | GRM44-1X7R105K250AL(muRata)     | SM/C_2220              |
| 6    | 1        | C11  | .1u,16V            |                                 | SM/C_0805              |
| 7    | 2        | C24,C12  | 10u,16V            | GRM32DR61C106KA01(muRata)       | SM/C_1210_GRM          |
| 8    | 2        | C13,C15  | 2.2n               |                                 | SM/C_1206              |
| 9    | 6        | C14,C22,C27,C33,C34,C43  | 0.1u               |                                 | SM/C_0805              |
| 10   | 6        | C16,C17,C18,C19,C20,C21  | 22u,6.3V           | GRM32DR60J226KA01(muRata)       | SM/C_1210_GRM          |
| 11   | 2        | C41,C25  | 1nF                |                                 | SM/C_0805              |
| 12   | 1        | C26  | 0.1uF 16V          |                                 | SM/C_0603              |
| 13   | 1        | C28  | 22nF               |                                 | SM/C_1206              |
| 14   | 1        | C29  | 0.1u,25V           |                                 | SM/C_1206              |
| 15   | 1        | C30  | 82pF               |                                 | SM/C_0805              |
| 16   | 1        | C31  | 1u,16V             | GRM32RR71H105KA01(muRata)       | SM/C_1210_GRM          |
| 17   | 2        | C44,C35  | 22n                |                                 | SM/C_0805              |
| 18   | 1        | C36  | 2.2u,16V           |                                 | SM/C_1206              |
| 19   | 1        | C37  | .1uF               |                                 | SM/C_0805              |
| 20   | 1        | C40  | 100pF              |                                 | SM/C_0805              |
| 21   | 1        | C42  | 470pF              |                                 | SM/C_0805              |
| 22   | 2        | D2,D1  | MBRB2535CTL        |                                 | DIODE_D2PAK            |
| 23   | 1        | D3   | LS4448             |                                 | SM/DO213AC             |
| 24   | 1        | D4   | ZM4743A            |                                 | SMB/DO214              |
| 25   | 8        | D5,D6,R12,R13,R19,R20,<br>R26,R31                                    | 0                  |                                 | SM/R_0805              |
| 26   | 8        | D7,D8,D9,D10,D11,D12,D13,<br>D14                                     | CMOSH-3            | CMOSH-3 (Central Semiconductor) | SOD523                 |
| 27   | 1        | D15  | 1N5819HW           |                                 | SOD123                 |
| 28   | 14       | JP1,JP2,JP3,JP4,JP5,JP6,<br>JP7,JP8,JP9,JP10,JP11,<br>JP12,JP25,JP28 | short              |                                 | VIA\2P                 |
| 29   | 1        | J1   | SS                 |                                 | ED5052                 |
| 30   | 1        | J2   | Vcc                |                                 | ED5052                 |
| 31   | 1        | J3   | SYNC               |                                 | ED5052                 |
| 32   | 1        | J4   | OUTA               |                                 | ED5052                 |
| 33   | 1        | J5   | OUTB               |                                 | ED5052                 |
| 34   | 1        | J6   | REF                |                                 | ED5052                 |
| 35   | 1        | J7   | FB                 |                                 | ED5052                 |
| 36   | 1        | L1   | 0.9uH              | PG0006.102(Pulse)               | PG0006                 |
| 37   | 1        | L2   | LQH43MN102K011     | LQH43MN102K01L(muRata)          | SDIP0302               |
| 38   | 2        | MB1,MA1  | SUD19N20-90        | SUD19N20-90(vishay)             | DPAKFET                |
| 39   | 1        | Q_Slope_Comp   | FMMT718            | FMMT718 (Zetex)                 | SM/SOT23_BEC           |
| 40   | 1        | Q2   | FZT853             | FZT853 (Zetex)                  | SM/SOT223_BCEC         |
| 41   | 3        | R_GS_MB1,R_GS_MA1,R3   | 10k                |                                 | SM/R_0805              |
| 42   | 1        | R_Pull_Up  | 3.01k              |                                 | SM/R_0805              |
| 43   | 1        | R_Slope_I  | 301                |                                 | SM/R_0805              |
| 44   | 1        | R_Slope_V  | 20k                |                                 | SM/R_0805              |
| 45   | 2        | R1,R33   | 1k                 |                                 | SM/R_0805              |
| 46   | 1        | R4   | 15                 |                                 | SM/R_0805              |
| 47   | 1        | R8   | 49.9k              |                                 | SM/R_1206              |
| 48   | 1        | R9   | 250                |                                 | SM/R_1210_MCR          |
| 49   | 2        | R10,R15  | 100                |                                 | SM/R_1206              |
| 50   | 2        | R17,R11  | 2.2                |                                 | SM/R_0805              |
| 51   | 2        | R16,R14  | 10                 |                                 | SM/R_1206              |
| 52   | 1        | R18  | 16.2               |                                 | SM/R_0805              |
| 53   | 1        | R21  | 56.2k              |                                 | SM/R_1206              |
| 54   | 1        | R22  | 10k                |                                 | SM/R_1206              |
| 55   | 2        | R42,R23  | TBD                |                                 | SM/R_0805              |
| 56   | 1        | R24  | 10                 |                                 | SM/R_0805              |
| 57   | 3        | R25,R38,R41  | 15k                |                                 | SM/R_0805              |
| 58   | 2        | R37,R28  | 2.2k               |                                 | SM/R_0805              |
| 59   | 1        | R30  | 37.4k              |                                 | SM/R_0805              |
| 60   | 1        | R32  | 18.2k              |                                 | SM/R_0805              |
| 61   | 1        | R36  | 11.5k              |                                 | SM/R_0805              |
| 62   | 1        | R39  | 25.5k              |                                 | SM/R_0805              |
| 63   | 1        | R43  | 100                |                                 | SM/R_0805              |
| 64   | 1        | T1   | PA0810             | PA0810(Pulse)                   | PA0810                 |
| 65   | 1        | T3   | P8208T             | P8208T(Pulse)                   | P8208T                 |
| 66   | 1        | T4   | PE-68386           | PE-68386(Pulse)                 | PE-68386               |
| 67   | 1        | U1   | SC4806             | SC4806(Semtech)                 | MLPQ-12 (4X4)          |
| 68   | 1        | U2   | RH02               | RH02(Diodes inc.)               | RH02                   |
| 69   | 2        | U6,U3  | SC1301A            | SC1301A(Semtech)                | SOT23_5PIN             |
| 70   | 2        | U5,U8  | SC4431             | SC4431(Semtech)                 | SOT23_5PIN             |
| 71   | 1        | U7   | MOC207             |                                 | SO-8                   |



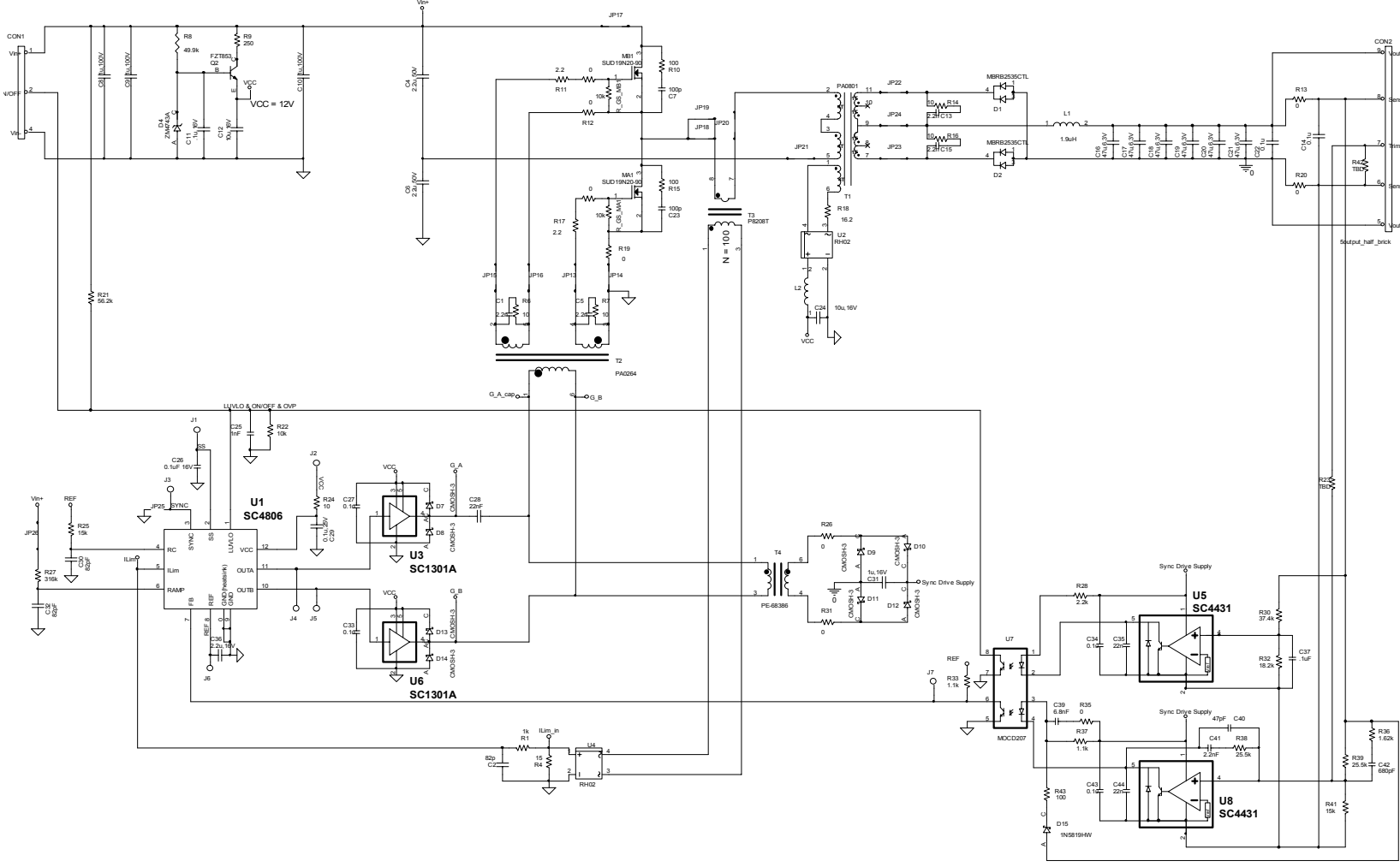


**POWER MANAGEMENT**
**Evaluation Board Gerber Plots (Cont.)**

**Board Layout Inner1**

**Board Layout Inner2**
**Evaluation Board Modifications**

**Board Layout Bottom**



## POWER MANAGEMENT

### HB Evaluation Board Schematics



**POWER MANAGEMENT**

**Evaluation Board Bill of Materials**

SC4806 Feed Forward Half bridge 3.3V 35W non Synchronous  
 SC4806EVB\_\_non\_sync Revision: 1.1

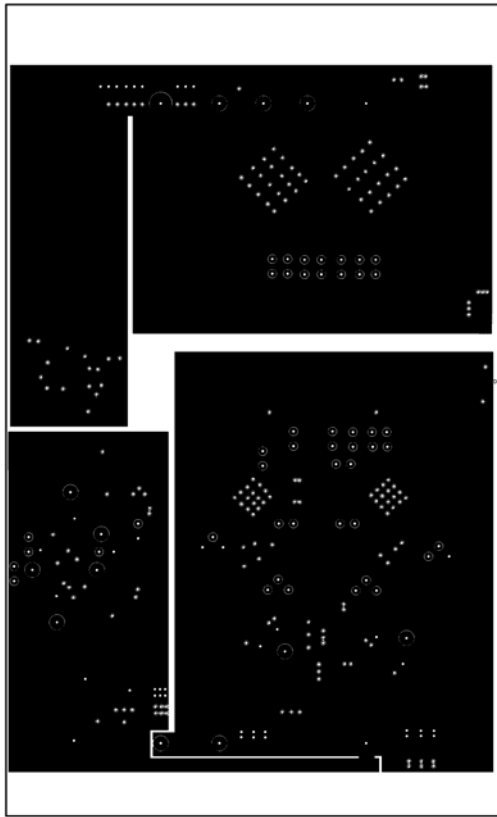
Bill Of Materials March 30,2005 10:47:27

| Item | Quantity | Reference   | Part               | Manufacturer #                  | Foot Print            |
|------|----------|---|--------------------|---------------------------------|-----------------------|
| 1    | 1        | CON1  | 3input_half_brick  |                                 | CON3INPUT_HALF_BRICK  |
| 2    | 1        | CON2  | 5output_half_brick |                                 | CON5OUTPUT_HALF_BRICK |
| 3    | 2        | C1,C5   | 2.2n               |                                 | SM/C_0805             |
| 4    | 1        | C2  | 82p                |                                 | SM/C_0805             |
| 5    | 2        | C4,C6   | 2.2u,50V           |                                 | SM/C_2220             |
| 6    | 2        | C23,C7  | 100p               |                                 | SM/C_1206             |
| 7    | 3        | C8,C9,C10   | 1u,100V            | GRM44-1X7R105K250AL(muRata)     | SM/C_2220             |
| 8    | 1        | C11   | .1u,16V            |                                 | SM/C_0805             |
| 9    | 2        | C12,C24   | 10u,16V            | GRM32DR61C106KA01(muRata)       | SM/C_1210_GRM         |
| 10   | 2        | C15,C13   | 2.2n               |                                 | SM/C_1206             |
| 11   | 6        | C14,C22,C27,C33,C34,C43   | 0.1u               |                                 | SM/C_0805             |
| 12   | 6        | C16,C17,C18,C19,C20,C21   | 47u,6.3V           | GRM43-2X5R476K6.3(muRata)       | SM/C_1210_GRM         |
| 13   | 1        | C25   | 1nF                |                                 | SM/C_0805             |
| 14   | 1        | C26   | 0.1uF 16V          |                                 | SM/C_0603             |
| 15   | 1        | C28   | 22nF               |                                 | SM/C_1206             |
| 16   | 1        | C29   | 0.1u,25V           |                                 | SM/C_1206             |
| 17   | 2        | C32,C30   | 82pF               |                                 | SM/C_0805             |
| 18   | 1        | C31   | 1u,16V             | GRM32RR71H105KA011(muRata)      | SM/C_1210_GRM         |
| 19   | 2        | C44,C35   | 22n                |                                 | SM/C_0805             |
| 20   | 1        | C36   | 2.2u,16V           |                                 | SM/C_1206             |
| 21   | 1        | C37   | .1uF               |                                 | SM/C_0805             |
| 22   | 1        | C39   | 6.8nF              |                                 | SM/C_0603             |
| 23   | 1        | C40   | 47pF               |                                 | SM/C_0805             |
| 24   | 1        | C41   | 2.2nF              |                                 | SM/C_0805             |
| 25   | 1        | C42   | 680pF              |                                 | SM/C_0805             |
| 26   | 2        | D1,D2   | MBRB2535CTL        |                                 | DIODE_D2PAK           |
| 27   | 1        | D4  | ZM4743A            |                                 | SMB/DO214             |
| 28   | 8        | D5,D6,R12,R13,R19,R20,<br>R26,R31   | 0                  |                                 | SM/R_0805             |
| 29   | 8        | D7,D8,D9,D10,D11,D12,D13,<br>D14  | CMOSH-3            | CMOSH-3 (Central Semiconductor) | SOD523                |
| 30   | 1        | D15   | 1N5819HW           |                                 | SOD123                |
| 31   | 14       | JP13,JP14,JP15,JP16,JP17,<br>JP18,JP19,JP20,JP21,JP22,<br>JP23,JP24,JP25,JP26 | short              |                                 | VIA2P                 |
| 32   | 1        | J1  | SS                 |                                 | ED5052                |
| 33   | 1        | J2  | Vcc                |                                 | ED5052                |
| 34   | 1        | J3  | SYNC               |                                 | ED5052                |
| 35   | 1        | J4  | OUTA               |                                 | ED5052                |
| 36   | 1        | J5  | OUTB               |                                 | ED5052                |
| 37   | 1        | J6  | REF                |                                 | ED5052                |
| 38   | 1        | J7  | FB                 |                                 | ED5052                |
| 39   | 1        | L1  | 1.9uH              | PG0006.212(Pulse)               | PG0006                |
| 40   | 1        | L2  | LQH43MN102K011     | LQH43MN102K01L(muRata)          | SDIP0302              |
| 41   | 2        | MB1,MA1   | SUD19N20-90        | SUD19N20-90(vishay)             | DPAKFET               |
| 42   | 1        | Q2  | FZT853             | FZT853 (Zetex)                  | SM/SOT223_BCEC        |
| 43   | 2        | R_GS_MB1,R_GS_MA1   | 10k                |                                 | SM/R_0805             |
| 44   | 1        | R1  | 1k                 |                                 | SM/R_0805             |
| 45   | 1        | R4  | 15                 |                                 | SM/R_0805             |
| 46   | 3        | R6,R7,R24   | 10                 |                                 | SM/R_0805             |
| 47   | 1        | R8  | 49.9k              |                                 | SM/R_1206             |
| 48   | 1        | R9  | 250                |                                 | SM/R_1210_MCR         |
| 49   | 2        | R15,R10   | 100                |                                 | SM/R_1206             |
| 50   | 2        | R17,R11   | 2.2                |                                 | SM/R_0805             |
| 51   | 2        | R16,R14   | 10                 |                                 | SM/R_1206             |
| 52   | 1        | R18   | 16.2               |                                 | SM/R_0805             |
| 53   | 1        | R21   | 56.2k              |                                 | SM/R_1206             |
| 54   | 1        | R22   | 10k                |                                 | SM/R_1206             |
| 55   | 2        | R23,R42   | TBD                |                                 | SM/R_0805             |
| 56   | 2        | R41,R25   | 15k                |                                 | SM/R_0805             |
| 57   | 1        | R27   | 316k               |                                 | SM/R_0805             |
| 58   | 1        | R28   | 2.2k               |                                 | SM/R_0805             |
| 59   | 1        | R30   | 37.4k              |                                 | SM/R_0805             |
| 60   | 1        | R32   | 18.2k              |                                 | SM/R_0805             |
| 61   | 2        | R33,R37   | 1.1k               |                                 | SM/R_0805             |
| 62   | 1        | R35   | 0                  |                                 | SM/R_0603             |
| 63   | 1        | R36   | 1.62k              |                                 | SM/R_0805             |
| 64   | 2        | R39,R38   | 25.5k              |                                 | SM/R_0805             |
| 65   | 1        | R43   | 100                |                                 | SM/R_0805             |
| 66   | 1        | T1  | PA0801             | PA0801(Pulse)                   | PA0805                |
| 67   | 1        | T2  | PA0264             | PA0264 (Pulse)                  | PE-68386              |
| 68   | 1        | T3  | P8208T             | P8208T(Pulse)                   | P8208T                |
| 69   | 1        | T4  | PE-68386           | PE-68386(Pulse)                 | PE-68386              |
| 70   | 1        | U1  | SC4806             | SC4806(Semtech)                 | MLPQ-12 (4X4)         |
| 71   | 2        | U4,U2   | RH02               | RH02(Diodes Inc.)               | RH02                  |
| 72   | 2        | U6,U3   | SC1301A            | SC1301A(Semtech)                | SOT23_5PIN            |
| 73   | 2        | U5,U8   | SC4431             | SC4431(Semtech)                 | SOT23_5PIN            |
| 74   | 1        | U7  | MOCD207            |                                 | SO-8                  |

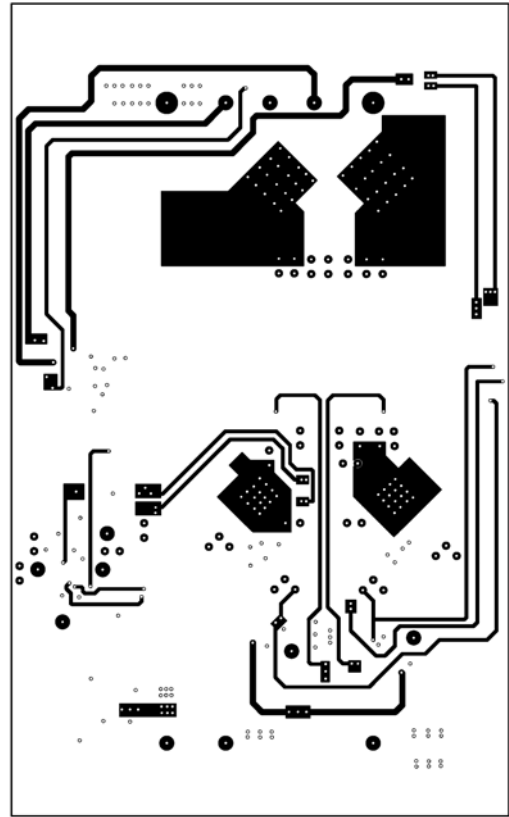


**POWER MANAGEMENT**

**Evaluation Board Gerber Plots (Cont.)**

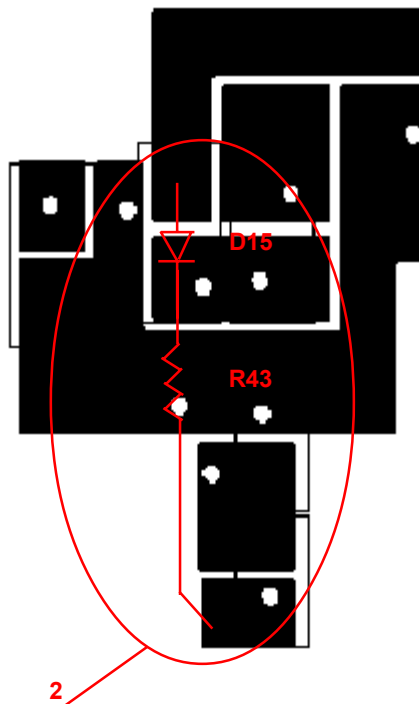


**Board Layout Inner1**



**Board Layout Inner2**

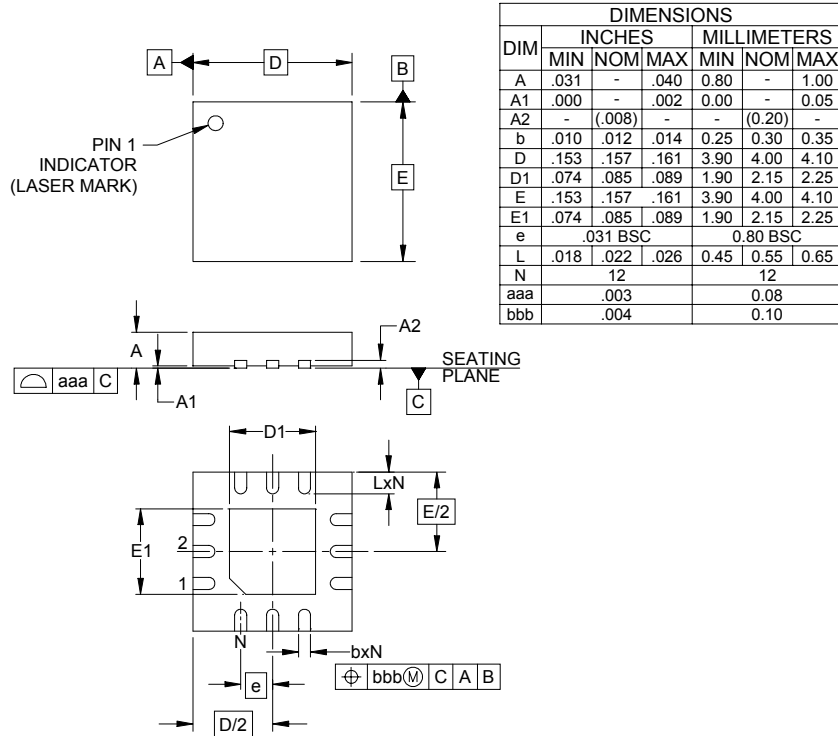
**Evaluation Board Modifications**



**Board Layout Bottom**

**POWER MANAGEMENT**

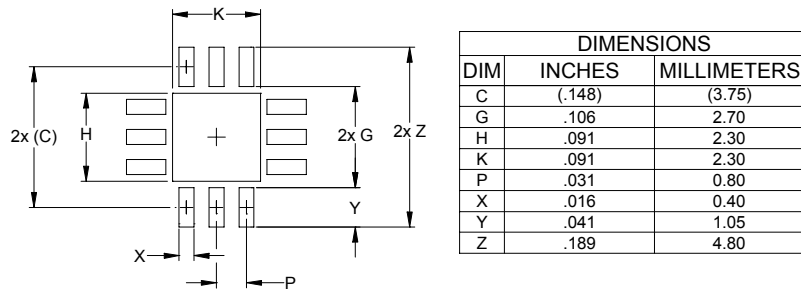
**Outline Drawing - MLPQ-12, 4 x 4**



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**Land Pattern - MLPQ-12, 4 x 4**



NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

**Contact Information**

Semtech Corporation  
 Power Management Products Division  
 200 Flynn Road, Camarillo, CA 93012  
 Phone: (805)498-2111 FAX (805)498-3804