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## POWER MANAGEMENT

### Description

The SC4810B/E is a 16 pin BICMOS primary side PWM controller for use in Isolated DC-DC and off-line switching power supplies. It is a highly integrated solution, requiring few external components. It features a high frequency of operation, accurately programmable maximum duty cycle, current mode control, line voltage monitoring, supply UVLO, low start-up current, and programmable soft start with user accessible reference. It operates in a fixed frequency, highly desirable for Telecom applications. The output for switch is complementary to each other with programmable delay between each transition. The active technique allows single ended converters beyond 50% duty cycle and greater flux swing for the power transformer while reducing voltage stresses on the switches. The separate sync pin simplifies synchronization to an external clock. Feeding the oscillator of one device to the sync of another forces biphased operation which reduces input ripple and filter size.

The SC4810B/E has a turn-on voltage threshold of 7V. In the SC4810B, OUT2 is inverted to drive the N-MOSFET. In the SC4810E, OUT2 is non-inverted to drive the P-MOSFET. These devices are available in a TSSOP-16 or MLPQ-16 lead package.

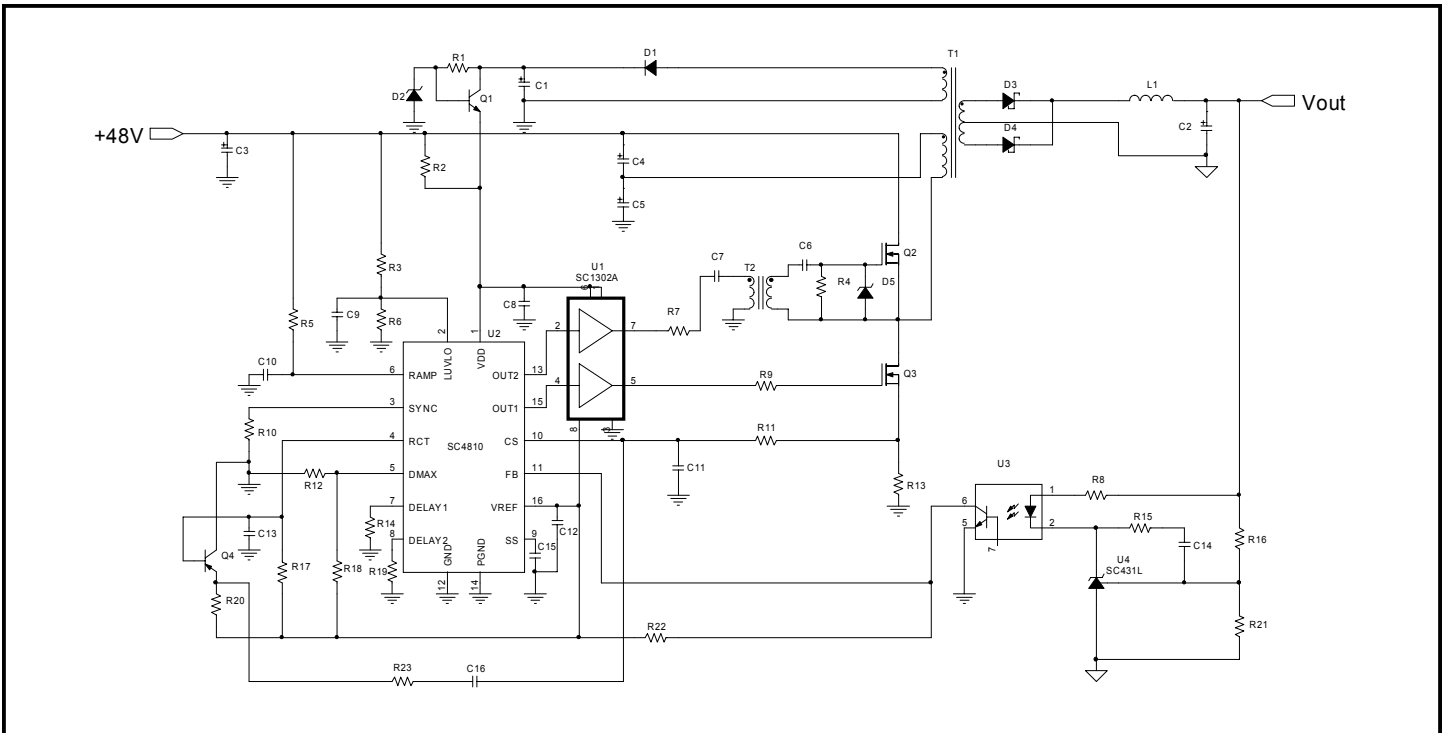
### Features

- ◆ Operation to 1MHz
- ◆ Accurate programmable maximum duty cycle
- ◆ Line voltage monitoring
- ◆ External frequency synchronization
- ◆ **Bi-phase mode of operation for low ripple**
- ◆ Independent programmable delays
- ◆ Hiccup mode current limit
- ◆ Under 250µA start-up current
- ◆ Programmable maximum volt-second clamp
- ◆ Accessible reference voltage
- ◆ VDD undervoltage lockout
- ◆ -40°C to 105°C operating temperature
- ◆ 16 lead TSSOP or MLPQ lead free packages. Both fully WEEE and RoHS compliant

### Applications

- ◆ Telecom equipment and power supplies
- ◆ Networking power supplies
- ◆ Power over LAN applications
- ◆ Industrial power supplies
- ◆ Isolated power supplies
- ◆ VoIP phones

### Typical Application Circuit



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Supply Voltage	$V_{DD}$	19	V
Supply Current	$I_{DD}$	25	mA
LUVLO	$V_{LUVLO}$	10	V
SS, DMAX, RCT, FB, CS, RAMP, SYNC		-0.3V to $V_{REF} + 0.3V$	V
Current VREF	$I_{REF}$	15	mA
Current LUVLO	$I_{LUVLO}$	-1	mA
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Junction Temperature Range	$T_J$	-40 to +150	°C
Lead Temperature (Soldering) 10 Sec.	$T_{LEAD}$	300	°C
Peak IR Reflow Temperature 20 - 40 Sec.	$T_{PKG}$	260	°C

**Electrical Characteristics**

Unless specified:  $V_{DD} = 12V$ ,  $C_{SS} = 1nF$ ,  $F_{OSC} = 420kHz$ ,  $R_T = 10k$ ,  $C_T = 220pF$ ,  $D_{MAX} = 2V$ ,  $R_{DELAY} = 75k\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $105^\circ C$

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Section</b>					
Supply Voltage				15	V
$I_{DD}$	$V_{DD} = 15V$ , No LOAD		3.5	4.5	mA
$I_{DD}$ Shutdown	SS = 0V		100	250	$\mu A$
<b>Ramp Section</b>					
Ramp Clamp Threshold Voltage			3		V
<b>UVLO Section (B/E version)</b>					
Start Threshold		8	8.4	8.8	V
Hysteresis			2		V



**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified:  $V_{DD} = 12V$ ,  $C_{SS} = 1nF$ ,  $F_{OSC} = 420kHz$ ,  $R_T = 10k$ ,  $C_T = 220pF$ ,  $D_{MAX} = 2V$ ,  $R_{DELAY} = 75k\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $105^\circ C$ 

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>VREF Section</b>					
VREF (B/E version)	0 - 5mA	4.85	5	5.15	V
<b>Line Under Voltage Lockout</b>					
Start Threshold		2.91	3	3.09	V
Hysteresis			150		mV
Input Bias Current <sup>(1)</sup>	LUVLO = 3.2V		-100		nA
<b>Comparator Section</b>					
CS Input Current <sup>(1)</sup>			-200		nA
PWM to OUT Propagation Delay (No Load) <sup>(1)</sup>			75		ns
<b>Current Limit Section</b>					
Current Limit Threshold		590	625	660	mV
$I_{LM}$ to OUT Propagation Delay <sup>(1)</sup>			75		ns
<b>Soft Start Section</b>					
$I_{SS}$	$V_{SS} = 0V$	-2.5	-5	-7.5	$\mu A$
Shutdown Threshold		500			mV
<b>Oscillator Section</b>					
Frequency Range <sup>(2)</sup>		50		1100	kHz
RCT Peak Voltage			3.00		V
RCT Valley Voltage			0.05		V
Maximum Duty Cycle	D <sub>MAX</sub> = 2.8V, OUT1		85		%
Maximum Duty Cycle	D <sub>MAX</sub> = 1.25V, OUT1		29		%
Frequency		380	420	460	kHz
<b>Sync/CLOCK</b>					
Clock SYNC Threshold	Positive Edge Triggered	2			V
Minimum Sync Input Pulse Width <sup>(1)</sup>	$F_{SYNC} > F_{OSC}$		50		ns

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless specified:  $V_{DD} = 12V$ ,  $C_{SS} = 1nF$ ,  $F_{OSC} = 420kHz$ ,  $R_T = 10k$ ,  $C_T = 220pF$ ,  $D_{MAX} = 2V$ ,  $R_{DELAY} = 75k\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $105^\circ C$

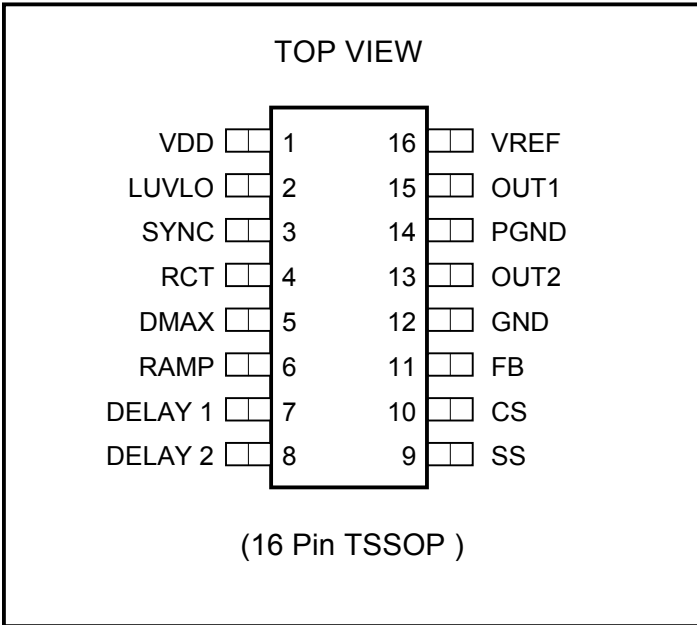
Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Output Section (OUT1 and OUT2)</b>					
Output VSAT Low	$I_{OUT} = 5mA$ sinking			500	mV
Output VSAT High	$I_{OUT} = 5mA$ sourcing	$V_{REF} - 0.6$			V
Rise Time <sup>(1)</sup>	$C_{OUT} = 20pF$		10		ns
Fall Time <sup>(1)</sup>	$C_{OUT} = 20pF$		10		ns
<b>Program Delay Section</b>					
OUT1 Fall to OUT2 Rise (SC4810B)			120		ns
OUT2 Fall to OUT1 Rise (SC4810B)			140		ns
OUT1 Fall to OUT2 Fall (SC4810E)			120		ns
OUT2 Rise to OUT1 Rise (SC4810E)			140		ns

**Notes:**

- (1) Guaranteed by design.
- (2) Guaranteed by characterization.
- (3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

**POWER MANAGEMENT**

**Pin Configurations**

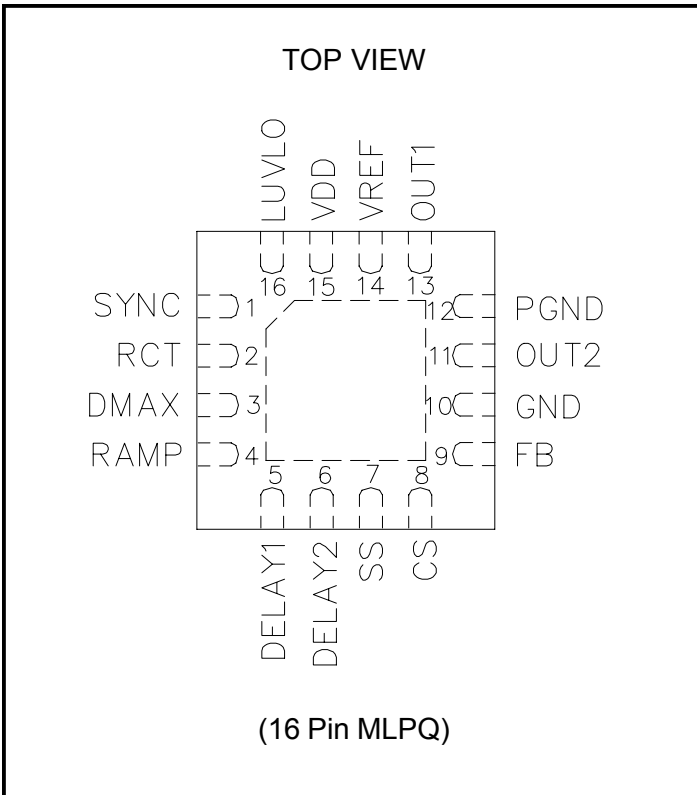


**Ordering Information**

Part Number <sup>(2)</sup>	Package <sup>(1)</sup>	Temp. Range (T <sub>J</sub> )
SC4810BITSTRT	TSSOP-16	-40°C to 105°C
SC4810EITSTRT		
SC4810BIMLTRT	MLPQ-16	
SC4810EIMLTRT		

Notes:

- (1) Only available in tape and reel packaging. A reel contains 2500 devices for TSSOP and 3000 parts for MLP package.
- (2) Lead free product. This product is fully WEEE and RoHS compliant.



**POWER MANAGEMENT**
**Pin Descriptions**

Pin # TSSOP	Pin # MLPQ	Pin Name	Pin Function
1	15	VDD	The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1µF ceramic capacitor.
2	16	LUVLO	Line undervoltage lock out pin. An external resistive divider will program the undervoltage lock out level. During the LUVLO, the Driver OUT1 is disabled and the softstart is reset. OUT2 continues with a fixed on time of DELAY 1 + DELAY2 approximately.
3	1	SYNC	SYNC is a positive edge triggered input with a threshold set to 2.1V. In the Bi-Phase operation mode the SYNC pin should be connected to the CT (Timing Capacitor) of the second controller. This will force a out of phase operation. In a single controller operation, SYNC could be grounded or connected to an external synchronization clock with a frequency higher than the on-board oscillator frequency. The external OSC frequency should be 30% greater for guaranteed SYNC operation.
4	2	RCT	The oscillator frequency is configured by connecting resistor RT from VREF to RCT and capacitor CT from RCT to ground. Using the equation below values for RT and CT can be selected to provide the desired OUT frequency.  $F = \frac{1}{(RT + 1k) \cdot CT \cdot \ln \left( 1 - \frac{V_{P-K}}{V_{REF}} \right)}$ where VP-K = RCT peak voltage
5	3	DMAX	Duty cycle up to 95% can be programmed via R18 and R12 (the resistor divider from Vref in the Application Circuit). When DMAX pin is taken above 3V, 100% duty cycle is achieved.
6	4	RAMP	A resistor from the RAMP to the input voltage and a capacitor from the RAMP to GND forms the ramp signal of maximum allowable volt-second product. The RAMP is discharged to GND when OUT1 is low and allowed to charge when OUT1 is high. A volt-second comparator compares the ramp signal to 3V to limit the maximum allowable volt-second product: Volt-second product clamp = 3 • Rramp • Cramp.
7	5	DELAY 1	A resistor from these pins to GND programs the non-overlap delay time between OUT1 and OUT2.
8	6	DELAY 2	A resistor from these pins to GND programs the non-overlap delay time between OUT2 and OUT1.

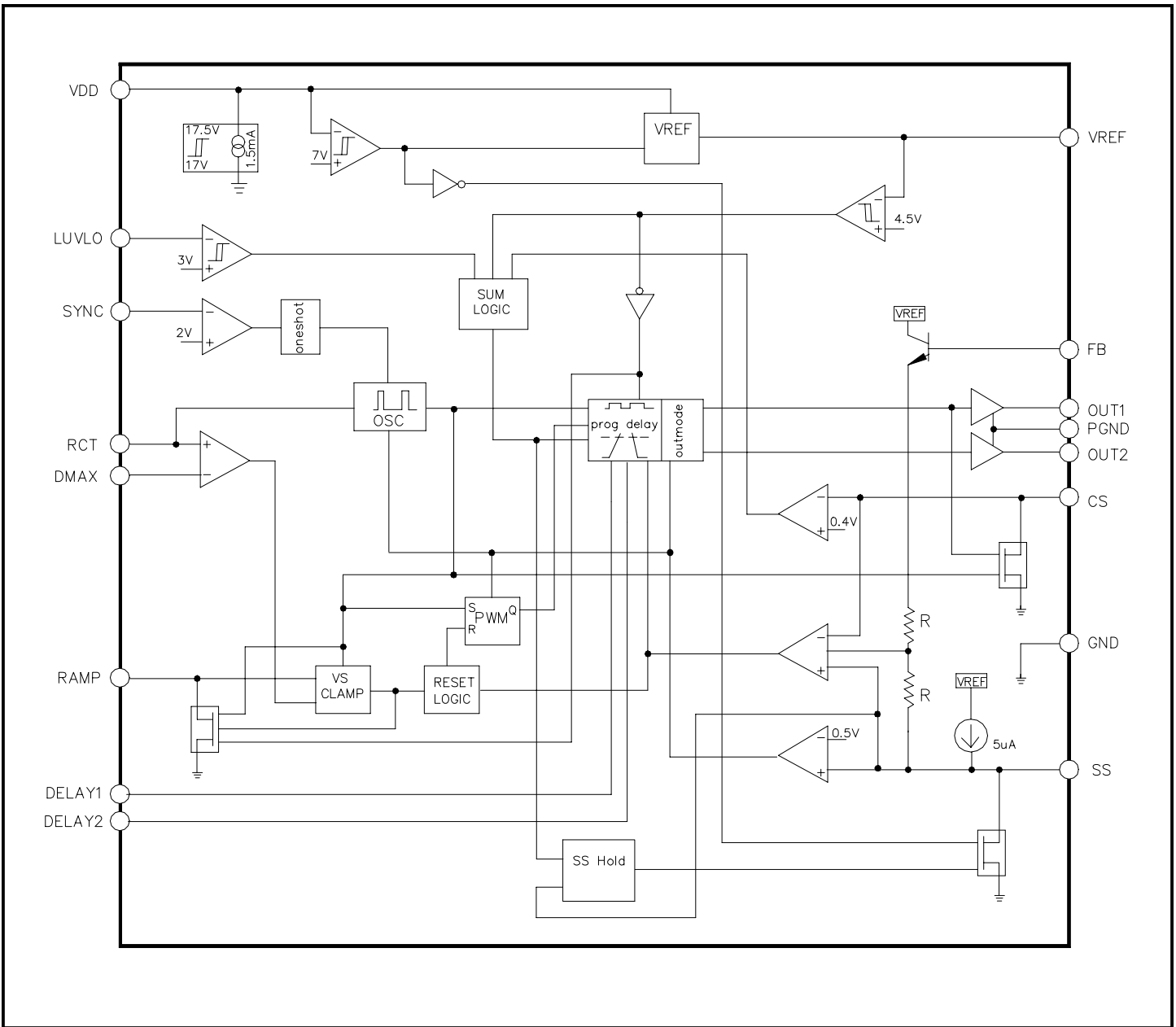
**POWER MANAGEMENT**
**Pin Descriptions (Cont.)**

Pin # TSSOP	Pin # MLPQ	Pin Name	Pin Function
9	7	SS	This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 5 $\mu$ A current source. Under normal soft start SS is discharged to less than 0.65V and then ramps positive to 1V during which time the OUT1 is held low. As SS charges from 1V to 2.5V, soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 4V (A and D) or 5V (B, C and E) voltage reference also goes low and $I_{DD} = 100\mu$ A.
10	8	CS	Current sense input is provided via the CS pin. The current sense input from a sense resistor provides current feedback to the PWM comparator and current limit signal to terminate the PWM pulse. When a pulse peak voltage provided at this pin exceeds 600mV, a soft-restart sequence will follow. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal PNP transistor.
11	9	FB	This pin is used to generate a reset signal when compared to CS for the PWM comparator with an offset voltage of 600mV and 1/2 attenuation. The feedback analog signal from the output of an error amplifier or an opto-coupler will be connected to this pin to provide regulation.
12	10	GND	Signal ground for all functions.
13	11	OUT2	This pin is the logic level drive output to the external MOSFET driver circuit (similar to SC1302) for the complementary switch.
14	12	PGND	Ground connection for the gate drivers. Connect PGND and GND at a single point.
15	13	OUT1	This pin is the logic level drive output to the external MOSFET driver circuit (similar to SC1302) for the main switch.
16	14	VREF	The 5V reference output. This reference is buffered and is available on the VREF pin. VREF should be bypassed with a 0.47 - 1.0 $\mu$ F ceramic capacitor.
N/A		THERMAL PAD	Pad for heatsinking purposes only. Connect to ground plane using multiple vias. Not connected internally.



POWER MANAGEMENT

Block Diagram



**POWER MANAGEMENT**

**Application Information**

**Introduction**

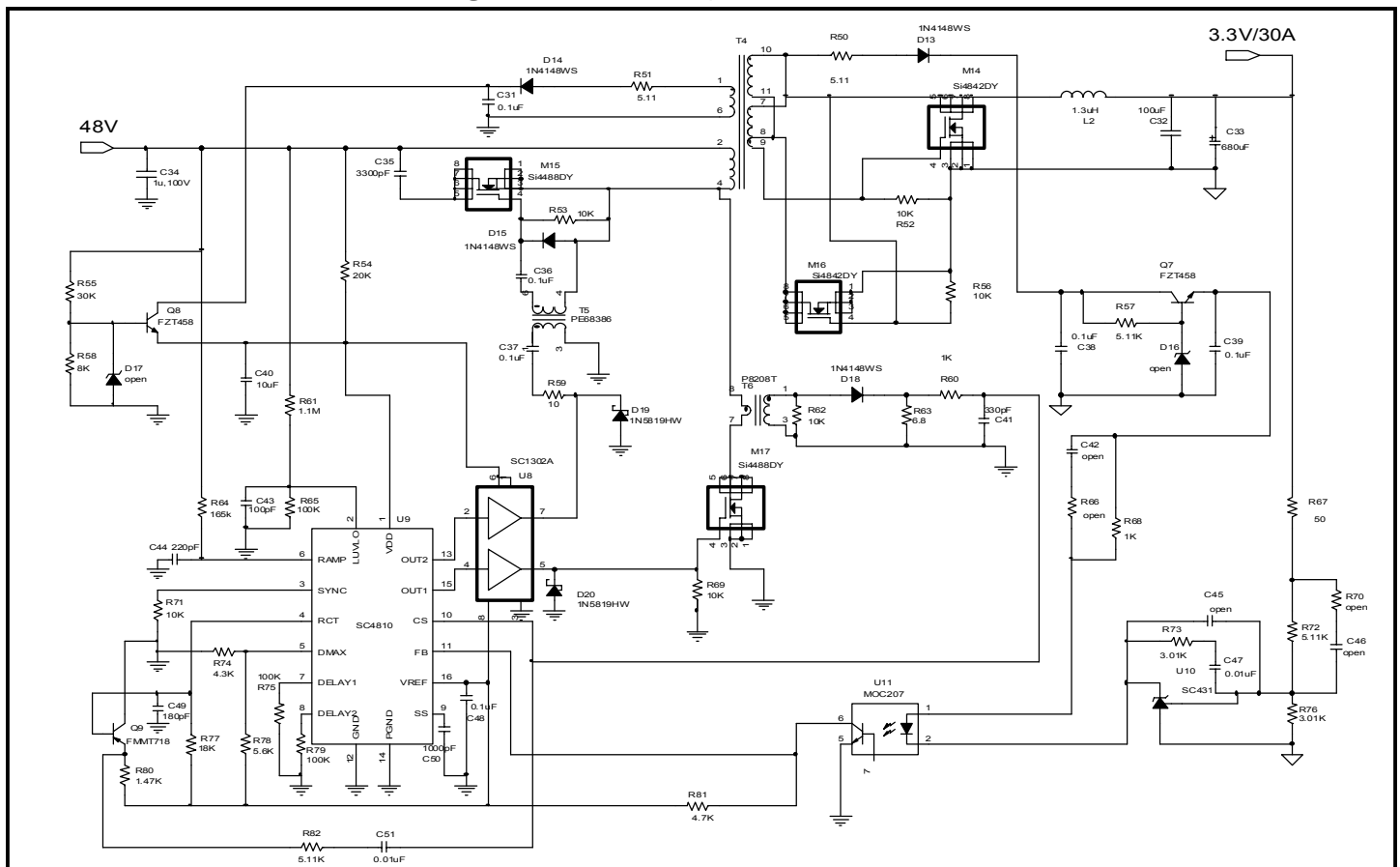
The SC4810B/E is a 16 pin BICMOS peak current mode controlled PWM controller for isolated DC-DC and off-line switching power supplies. It features a high switching frequency of operation, programmable limits for both power transformer voltage-second product and maximum PWM duty cycle, line under-voltage lockout, auxiliary switch activation complementary to main power switch drive, programmable leading-edge delay time between activation of each switch, multiple protection features with programmable cycle-by-cycle current limit and hiccup mode over-current protection plus soft-restart. It operates in a fixed frequency programmed by external components. The separate sync pin simplifies synchronization to an external clock. Feeding the oscillator of one device to the sync of another forces biphas operation which reduces input ripple and input and output filter size.

The SC4810 can be applied in an active clamp forward topology with the input voltage ranging from 36V to 72V. This topology allows the converter to achieve an efficiency of 92.4% at normal input voltage of 48V.

**Circuit Description**

The schematic of the active clamp forward converter is illustrated in Figure. 1 below. T4 is the power transformer. M17 is the N-channel main switching MOSFET and M15 is the auxiliary N-channel MOSFET. C35 is the reset capacitor for resetting the power transformer's core. M14 and M16 construct the synchronous rectification circuit. L2 and C32 and C33 construct the low-pass output filtering circuit. T6 is the current sensing transformer. R62 is the reset resistor for resetting the magnetic core of the current sensing transformer. D18 is the rectifying diode. R63 is the current sensing resistor. R60 and C41 construct the low-pass filtering circuit for the sensed current signal. The primary bias circuit consists of R55, R58, D17, Q8, C40, C31, D14 and R51. R55 and R58 construct a voltage divider, which limits the bias voltage to 6.9V until the line voltage reach 36V. D17 is a zener diode that limits the bias voltage to under 8V. R51, D14 and C31 construct the peak charge circuit. The peak charge circuit will provide bias to the PWM IC U9 (SC4810) and the driver U8 (SC1302A) after the converter starts

Figure 1: Active Clamp Forward Converter



**POWER MANAGEMENT**
**Application Information (Cont.)**

up so that the total power loss is less. D19, R59, C37, T5, C36, D15 and R53 construct the driving circuit for the auxiliary reset switch M15. The secondary side bias circuit composed of R50, D13 and C38 is regulated to about 7.5V via a linear regulator composed of R57, Q7 D16 and C39. The feedback of the converter is composed of U10 (SC431), U11, R73, C47, C45, R72, R76, R70 and C46.

SC4810 is the PWM controller which processes the voltage feedback plus current signal and generates driving signals to drive the main switch and auxiliary reset switch. SC1302A is a dual driver IC which is capable of sourcing 3A peak current. To obtain the best performance, SC1302A is adopted to drive M17 and M15 in the Semtech application circuits. SC4810 features dual complementary driving signals. And SC4810 also provides adjustable leading-edge delay time for the driving signals, which helps to achieve zero-voltage switching in active clamp forward converter. R75 and R79 are the two resistors available to adjust the delay for the complementary driving. C50 is the soft-start capacitor. R61 and R65 construct the voltage divider for the line under voltage lock out protection. R64 and C44 construct the circuit for the programmable power transformer voltage-second production protection limits. This special protection function provide the voltage-second balance for the power transformer under different input line conditions. R78 and R74 also provide an extra maximum duty cycle protection for the power converter.

The clock signal is generated by C49 and R77. When VDD of SC4810 hits the threshold voltage, VREF jumps up to 5.0V. VREF charges C49 via R77. C49 will be discharged via an internal FET whenever the voltage on C49 reaches 3.0V. The selection of C49 and R77 is described in the "Set Clock Frequency" section on the following page. Q9 works as a buffer between the clock signal and the slope compensation signal to minimize the interference on the system clock signal. R80 is a pull-up resistor tied to VREF. Since SYNC function is not utilized, SYNC pin is grounded via R71.

**Power Transformer Design**

A power transformer with the turns ratio of 6 to 1 was designed for this application. With the turns ratio of 6:1, the duty ratio under different input line and load conditions were calculated to verify feasibility.

A self-driven configuration was adopted on the secondary side for driving the synchronous rectification FETs. One extra winding (Pin8~Pin9) was added at the bottom side of the power transformer's secondary side to drive the freewheeling FET. The forward FET was driven directly from the top of the power winding. Primary side auxiliary winding was used to generate primary side bias to improve the converter's efficiency.

The final configuration of the power transformer is illustrated as Fig. 2.

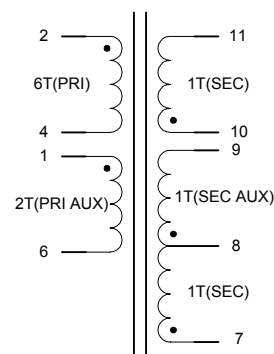


Fig.2 Illustration of the power transformer PA0944G (PUSLE ENGINEERING)

**Power MOSFET Selection**

The selection of the switching power MOSFET is based on the peak & RMS current rating, the total gate charge, Rds and drain to source voltage rating. In this application, SI4842 was chosen for the secondary side synchronous rectification MOSFET. And SI4488 was chosen for the primary side main switching and reset MOSFET.

**Output Filter Design**

The output filtering circuit consists of the output inductor and output capacitors. The design of the output capacitor usually depends on the specification of the requirement of the output ripple. Given the worst case output ripple requirement and peak to peak output current ripple plus the duty ratio under the different line and load condition, output capacitance is calculated to meet the output ripple requirement. After all, ESR and ESL of the output capacitor under certain switching frequency should also be considered during the calculation. The value of the output inductance would affect the peak to peak value of the output current, which would also influence the

**POWER MANAGEMENT**

**Application Information (Cont.)**

output voltage ripple. The designer needs to take the output inductance and output capacitance and the ESL and ESR of the output capacitor into consideration during the design.

For this application, one Panasonic power choke output inductor was selected and three 6.3V, 100uF TDK ceramic capacitors were adopted in the design.

**Selection of the Current Sensing Resistor**

The selection of the current sensing resistor is based on the over-current protection triggering point. SC4810 employs a Hiccup mode over-current protection with an overcurrent threshold of 600mV. A voltage signal above 600mV on the CS pin will trigger hiccup mode overcurrent protection. Suppose the over-current protection setpoint is set to be I<sub>OV</sub>. The threshold voltage of SC4810 is V<sub>threshold</sub>. The turns ratio of the power transformer is N<sub>s</sub>/N<sub>p</sub>. The turns ratio of the current sensing transformer is N<sub>cs</sub>:1. Then the R<sub>sense</sub> would be calculated as:

$$R_{sense} = \frac{V_{Threshold} \times N_P \times N_{CS}}{I_{OV} \times N_S} \dots\dots(1)$$

**Set Clock Frequency**

The SC4810 uses a pair of resistors and capacitors to generate a triangle signal as the clock signal, as illustrated in Fig. 3.

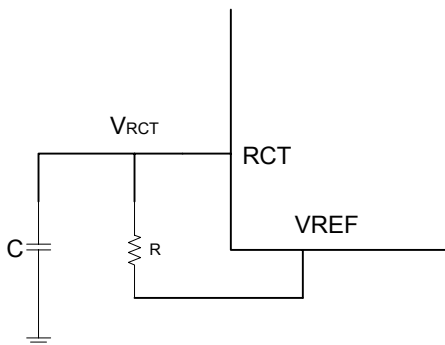


Fig. 3 Configuration for Clock Signal

The voltage waveform on the RCT pin is illustrated as in Fig. 4.

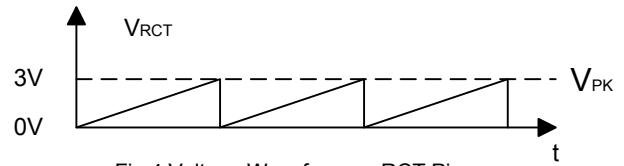


Fig.4 Voltage Waveform on RCT Pin

As illustrated, the capacitor C is charged via the resistor R from V<sub>REF</sub>. Whenever the voltage on the RCT pin reaches 3V, the capacitor C will be discharged through an internal FET shorted to ground. When the clock signal circuit is connected as in Fig.3, the frequency of the clock signal is defined, as in equation 2.

$$F = \frac{1}{\left[ (RT + 1k) \cdot CT \cdot \ln \left( 1 - \frac{V_{P-K}}{V_{REF}} \right) \right]} \dots\dots(2)$$

V<sub>REF</sub> is the reference voltage of the SC4810, 4V for SC4810A/D and 5V for SC4810B/C/E. In this application, to get 600kHz, C = 180pF, (R + 1k) = 10k ohms and V<sub>P-K</sub> = 3V.

**Maximum Duty Ratio Limit**

SC4810 features maximum duty ratio limitation for extra protection. The maximum duty ratio is determined by the voltage on DMAX pin. As illustrated as in Fig. 5, V<sub>DMAX</sub> will be compared with V<sub>RCT</sub> and DMAX is determined by the comparison of the two signals.

**POWER MANAGEMENT**

**Application Information (Cont.)**

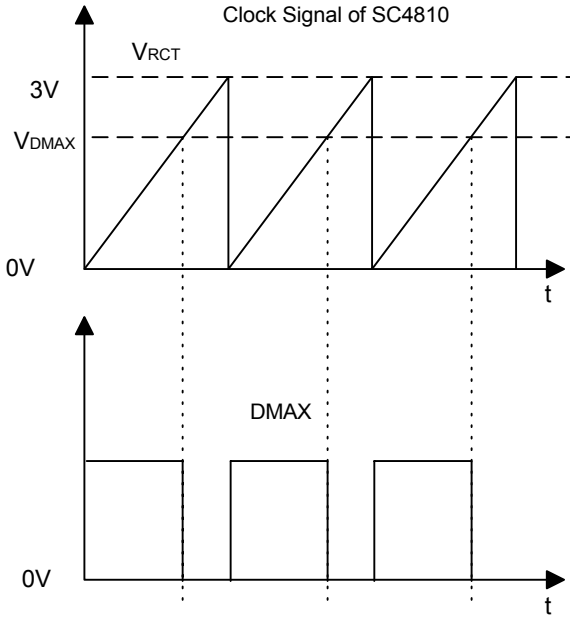


Fig. 5 Illustration for DMAX

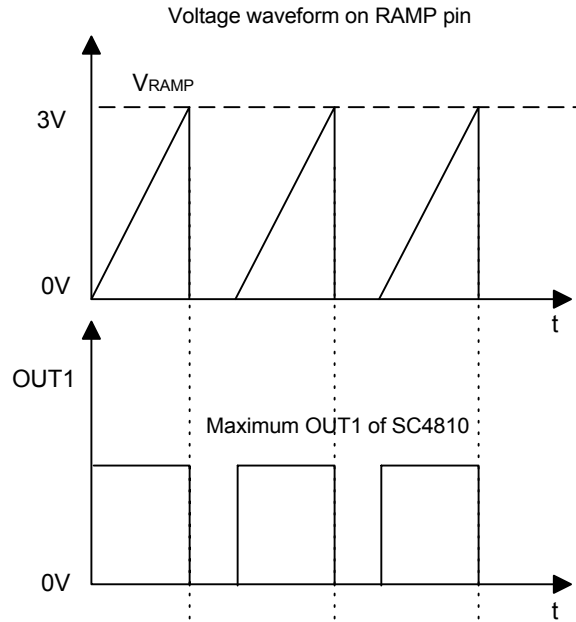


Fig. 6 Illustration of the programmable limits for power transformer voltage-second product

In this application,  $V_{D_{MAX}}$  was designed to be 2.8V. So the  $D_{MAX} = 90\%$ .

**Limit for Power Transformer Voltage Second Product**

The SC4810 also features programmable limits for power transformer voltage-second product. As illustrated in Fig. 6 and Fig. 7 RAMP pin is charged up via a resistor R from the input line voltage. The capacitor C will be discharged via an internal FET shorted to ground and the output OUT1 will be pulled low whenever the voltage on RAMP pin hits 3V. By adjusting the values of the resistor R and the value of the capacitor C, the maximum voltage-second product imposed on the power transformer is preset. The maximum voltage-second product limitation helps prevent saturation of the power transformer.

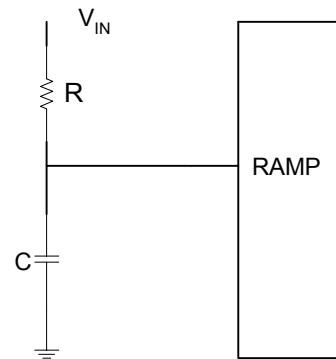


Fig. 7 Illustration for Maximum voltage-second product on the power transformer

The selection of the R and C should consider the maximum voltage rating of the main switching FET. In this application, the voltage rating of SI4488 is 150V. Since  $V_{in} \cdot D / (1-D) = 150V$ ,  $D = 0.8$  for low line 36V. So to get 80% at low line,  $R = 165k\Omega$  and  $C = 220pF$  were selected using volt-second product equation:  
 $3 \cdot \text{Ramp} \cdot \text{Cramp}$



**POWER MANAGEMENT**
**Application Information (Cont.)**
**VDD and LUVLO**

SC4810 features three different input turn-on voltage thresholds, as specified in the Electrical Characteristics on page 2.  $V_{REF}$  starts to regulate when the supply voltage on the VDD pin is above the turn-on voltage threshold.  $V_{REF}$  drops to ground when VDD is lower than the turn-on threshold minus the hysteresis value. The soft start cap remains grounded as long as LUVLO is below the threshold voltage 3V. The soft start cap will be charged up through an internal 5uA current source when LUVLO is above the threshold voltage.

**Soft Start**

The soft-start function is implemented by charging the soft-start cap through an internal 5uA current source. Under normal soft-start, the SS pin is discharged below 0.65V and ramps up to 1V, during which time the output driving signals OUT1 and OUT2 are held low. During the time when the SS pin is charged from 1V to 2.5V, soft-start is implemented by an increasing output duty ratio. The duty ratio is completely under the control of the feedback after the SS pin is above 2.5V.

When the SS pin is pulled down below 0.5V, OUT1 and OUT2 will be held low and the VREF pin will be grounded via an internal FET.

**Complementary Driving with Programmable Delays**

The SC4810 features dual driving signals to drive two power switches complementarily. This feature makes the SC4810 suitable for a variety of applications in which dual complimentary driving signals are needed. The SC4810 even provides programmable driving delay as an extra feature for applications such as active-clamp forward topology. The users can program the driving delay by adjusting the resistors tied to pin DELAY1 and pin DELAY2 respectively to achieve the optimum delay for each output. The delay of OUT1 is controlled by the resistor tied to pin DELAY1 and the delay of OUT2 is controlled by the resistor tied to pin DELAY2. For illustration, see Fig. 8.

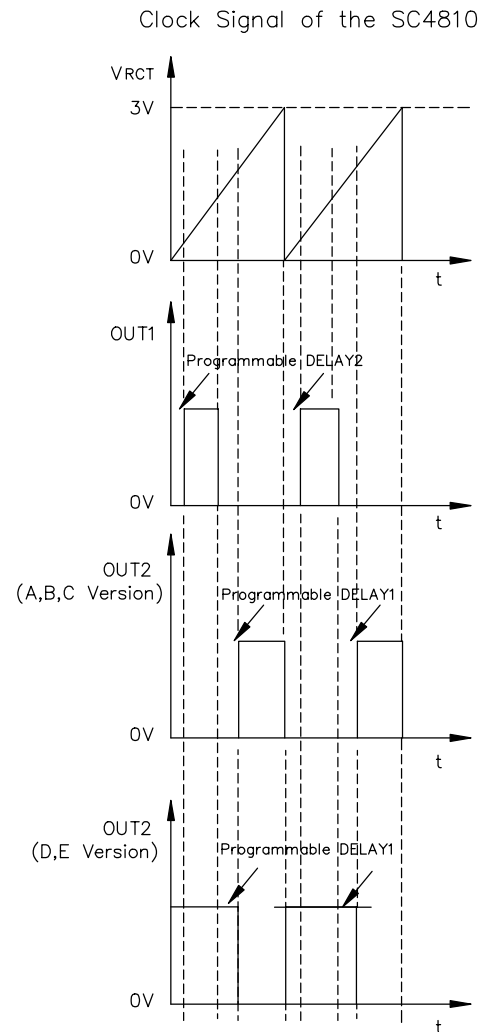


Fig. 8 Illustration for programmable delay of  $OUT1$  and  $OUT2$

**Over Current Protection**

The SC4810 provides Hiccup mode over-current protection when the sensed current signals are beyond 0.6V. When the hiccup mode over-current protection is triggered, the soft-start cap will be discharged immediately by an internal grounded FET. When the soft-start pin SS is pulled down below 1V,  $OUT1$  and  $OUT2$  will be disabled, and a soft re-start sequence will follow.

SC4810 can also be configured to implement cycle-by-cycle over-current limit. As illustrated in Fig. 9, cycle-by-cycle over-current limitation can be achieved by adjusting the values of  $R1$  and  $R2$  to limit the voltage of FB pin to less than the threshold voltage (0.6V) of the hiccup over-current protection, using equations (3) and (4).

**POWER MANAGEMENT**

**Application Information (Cont.)**

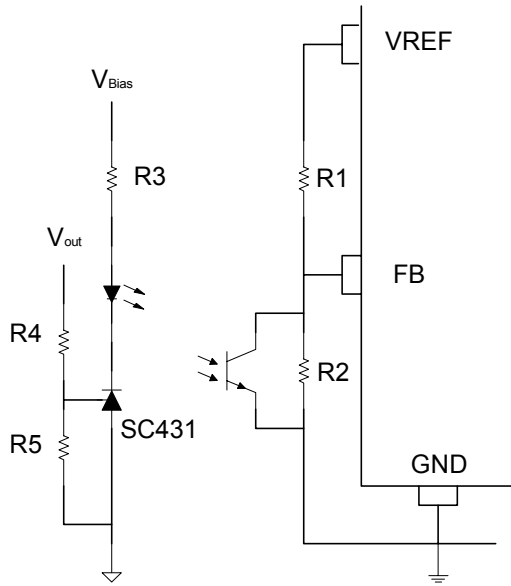


Fig.9 Cycle-by-cycle over-current limitation

$$V_{FB} = 2 \cdot V_{CS} + 1.3V \dots\dots(3)$$

$$V_{FB} = V_{REF} \cdot \frac{R_2}{R_1 + R_2} \dots\dots(4)$$

**Synchronization**

SC4810 features a special synchronization function which is leading-edge triggered with a threshold set to 2.1V. Applications like multi-phase interleaving can be achieved using the SYNC pin. When the SYNC pin is connected to the RCT pin of the master SC4810, the outputs of the two SC4810's will be out of phase. The frequency of the master SC4810 clock signal should be at least 30% faster than that of the slave SC4810 for the

guaranteed synchronization. SYNC pin should be grounded if synchronization is unused. (The patent for the synchronization scheme is pending).

The synchronous function is illustrated as in Fig. 10.

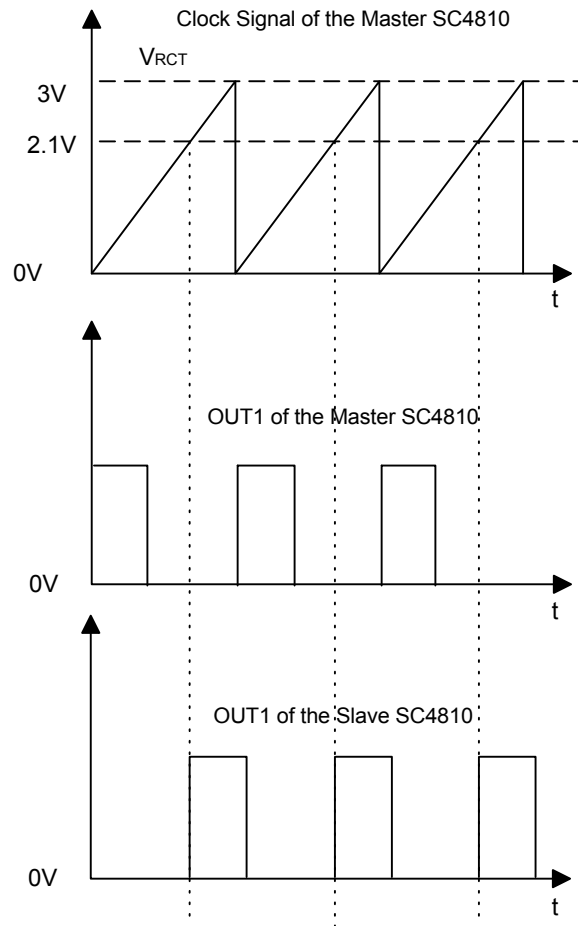


Fig. 10 Illustration for Synchronization

**POWER MANAGEMENT****Applications Information (Cont.)****PCB Layout Guidelines**

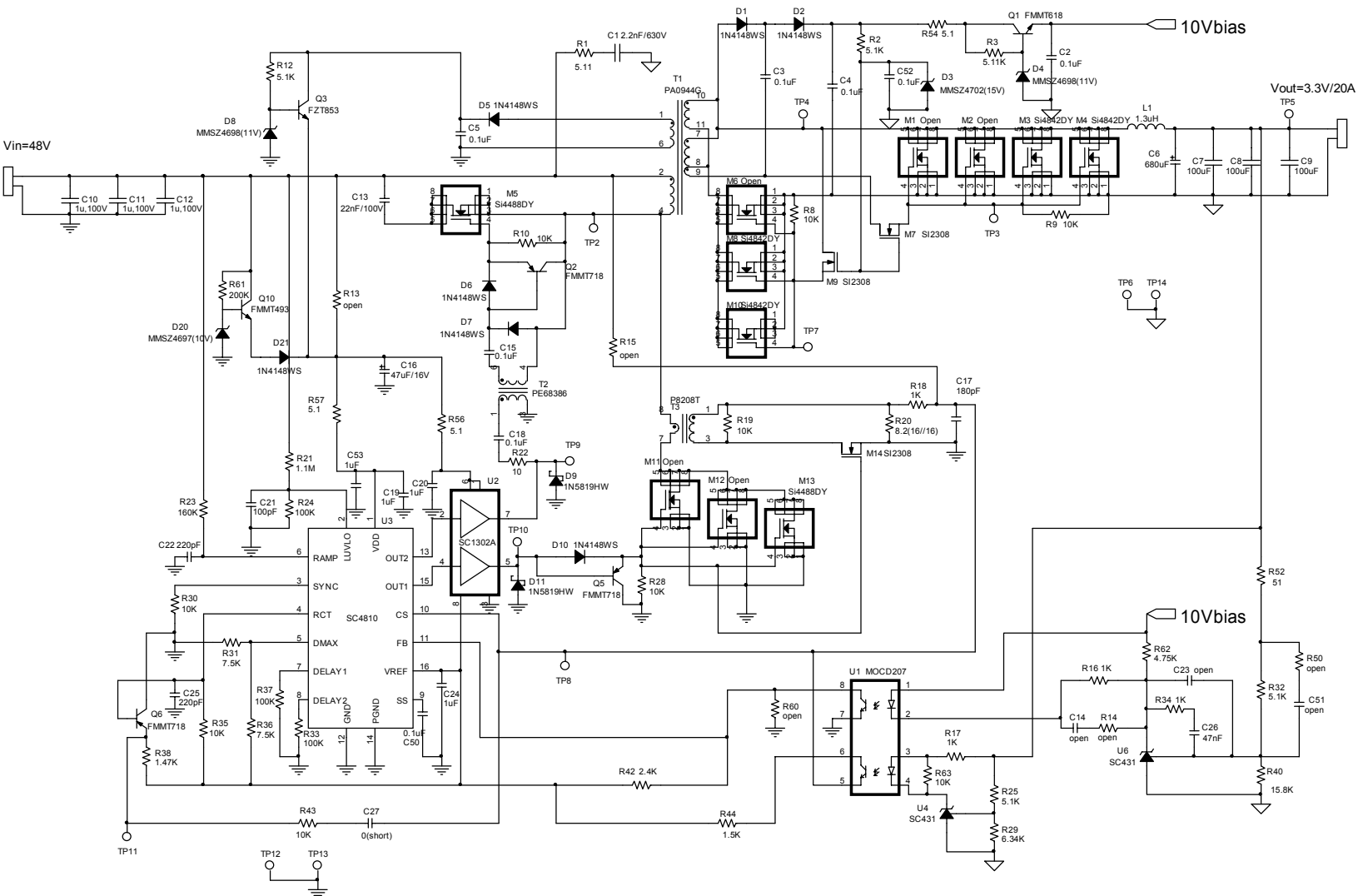
PCB layout is very critical, and the following should be used to insure proper operation of the SC4810. High switching currents are present in applications and their effect on ground plane must be understood and minimized.

- 1) The high power parts of the circuit should be placed on a board first. A ground plane should be used. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and the main switch FET ground.
- 2) The loop formed by the Input Capacitor(s) ( $C_{in}$ ), the main transformer and the main switch FET must be kept as small as possible. This loop contains all the high fast transient switching current. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.
- 3) The connection between FETs and the main transformer should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.
- 4) The output capacitor(s) ( $C_{out}$ ) should be located as close to the load as possible. Fast transient load currents are supplied by  $C_{out}$  only. Connections between  $C_{out}$  and the load must be short, wide copper areas to minimize inductance and resistance.
- 5) A 0.1 $\mu$ F to 1 $\mu$ F ceramic capacitor should be directly connected between VDD and PGND and a 1 $\mu$ F to 4.7 $\mu$ F ceramic capacitor between VREF and PGND. The SC4810 is best placed over a quiet ground plane area. Avoid pulse currents in the  $C_{in}$  and the main switch FET loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the VDD supply capacitor(s). Under no circumstances should GND be returned to a ground inside the  $C_{in}$  and the main switch FET loop. This can be achieved by making a star connection between the quiet GND planes that the SC4810 will be connected to and the noisy high current GND planes connected to the FETs.
- 6) The feed back connection between the error amplifier and the FB pin should be kept as short as possible, and the GND connections should be to the quiet GND used for the SC4810.
- 7) If an opto-coupler is used for isolation, quiet primary and secondary ground planes should be used. The same precautions should be followed for the primary GND plane as mentioned in item 5. For the secondary GND plane, the GND plane method mentioned in item 4 should be followed.
- 8) All the noise sensitive components such as VDD bypass capacitor, RCT oscillator resistor/capacitor network, DMAX resistive divider, VREF bypass capacitor, delay setting resistors, current sensing circuitry and feedback circuitry should be connected as close as possible to the SC4810. The GND return should be connected to the quiet SC4810 GND plane.
- 9) The connection from the OUT of the SC4810 should be minimized to avoid any stray inductance. If the layout can not be optimized due to constraints, a small Schottky diode may be connected from the OUT pin to the ground directly at the IC. This will clamp excessive negative voltages at the IC.
- 10) If the SYNC function is not used, the SYNC pin should be grounded at the SC4810 GND to avoid noise pick up.



## POWER MANAGEMENT

### SC4810B Evaluation Board - Schematic



**POWER MANAGEMENT**
**SC4810B Evaluation Board - BOM**

Item	Quantity	Reference	Part	Package	Manufacturer	P/N
1	1	C1	2.2nF/630V	SM0805	TDK	C3216X7R2J222K
2	11	C2,C3,C4,C5, C15,C18,C19, C20,C50,C52,C53	0.1uF	SM0805		
3	1	C6	680uF	SM/CT_7343_12	Sanyo	4TPB680M
4	3	C7,C8,C9	100uF	SM/C_1812	TDK	C4532X5ROJ107MT
5	3	C10,C11,C12	1u,100V	SM/C_1210	TDK	C3225X7R2A105K
6	1	C13	22nF/100V	SM1206	TDK	C3216X7R2J223M
8	1	C16	47uF/16V	SM/CT_7343	Sanyo	16TQC47M
9	1	C17	180pF	SM0805		
10	1	C21	100pF	SM0805		
11	2	C25,C22	220pF	SM0805		
12	1	C24	1uF	SM0805		
13	1	C26	47nF	SM0805		
14	1	C27	0(short)	SM0805		
15	7	D1,D2,D5, D6,D7,D10,D21	1N4148WS	SOD123	Vishay	1N4148WS
16	1	D3	MMSZ4702(15V)	SOD123	On Semi	MMSZ4702T1
17	2	D4,D8	MMSZ4698(11V)	SOD123	On Semi	MMSZ4698T1
18	2	D9,D11	SL04	SOD123	Vishay	SL04
19	1	D20	MMSZ4697(10V)	SOD123	On Semi	MMSZ4697T1
20	1	L1	1.3uH	PCC-S1	Panasonic	ETQPAF1R3EFA
22	4	M3,M4,M8,M10	Si4842DY	SO-8	Vishay	Si4842DY
23	2	M5,M13	Si4488DY	SO-8	Vishay	Si4488DY
24	3	M7,M9,M14	SI2308	SOT-23	Vishay	SI2308
25	1	Q1	FMMT618	SOT-23	Zetex	FMMT618
26	3	Q2,Q5,Q6	FMMT718	SOT-23	Zetex	FMMT718
27	1	Q3	FZT853	SM/SOT223_BCEC	Zetex	FZT853
28	1	Q10	FMMT493	SOT-23	Zetex	FMMT493
29	1	R1	5.11	SM0805		
30	4	R2,R12,R25,R32	5.1K	SM0805		
31	1	R3	5.11K	SM0805		
32	9	R8,R9,R10,R19, R28,R30,R35,R43,R63	10K	SM0805		
33	1	R13	open	SM1206		
34	1	R16	1K	RC0805		
35	3	R17,R18,R34	1K	SM0805		



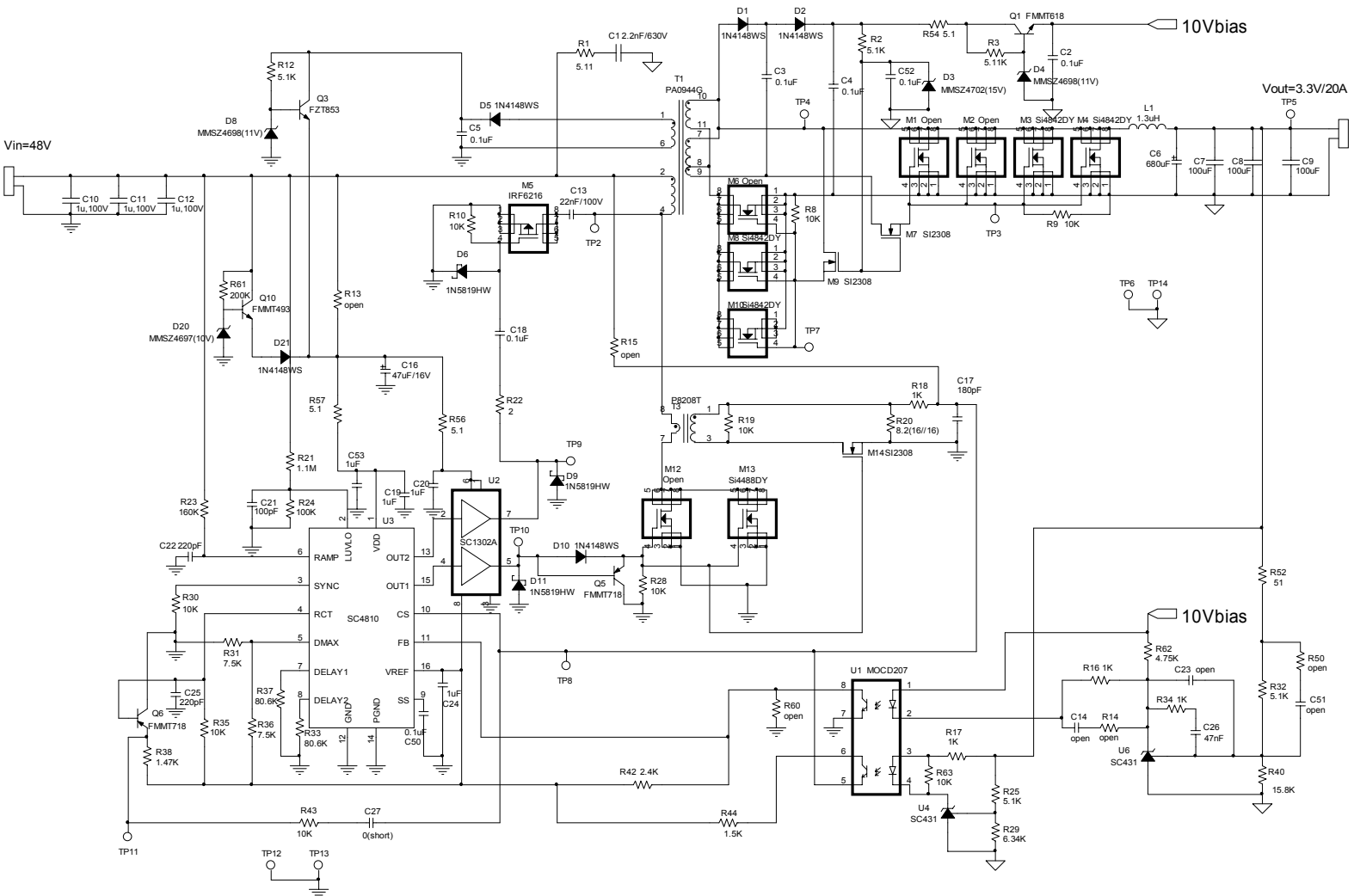
**POWER MANAGEMENT**
**SC4810B Evaluation Board - BOM**

36	1	R20	8.2	SM0805		
37	1	R21	1.1M	SM0805		
38	1	R22	10	SM0805		
39	1	R23	160K	SM0805		
40	1	R24	100K	SM0805		
41	1	R29	6.34K	SM0805		
42	2	R31,R36	7.5K	SM0805		
43	2	R33,R37	100K	SM0805		
44	1	R38	1.47K	SM0805		
45	1	R40	15.8K	SM0805		
46	1	R42	2.4K	SM0805		
47	1	R44	1.5K	SM0805		
48	1	R52	51	SM0805		
49	3	R54,R56,R57	5.1	SM0805		
50	1	R61	200K	SM0805		
51	1	R62	4.75K	SM0805		
53	1	T1	PA0944G	PA0646	Pulse	PA0944G
54	1	T2	PE68386	PE68386	Pulse	PE68386
55	1	T3	P8208T	P8208	Pulse	P8208T
56	1	U1	MOCD207	SO-8	Fairchild	MOCD207
57	1	U2	SC1302A	MSOP-8	<b>Semtech</b>	SC1302A
58	1	U3	SC4810	TSSOP16	<b>Semtech</b>	SC4810
59	2	U4,U6	SC431	SOT-23	<b>Semtech</b>	SC431



## POWER MANAGEMENT

### SC4810E Evaluation Board - Schematic



**POWER MANAGEMENT**
**SC4810E Evaluation Board - BOM**

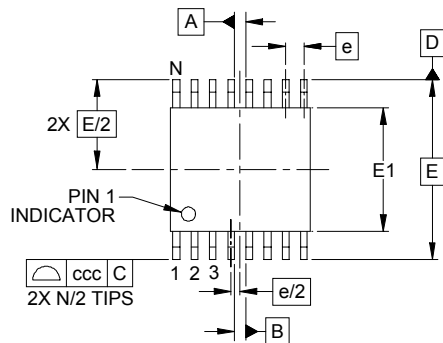
Item	Quantity	Reference	Part	Package	Manufacturer	P/N
1	1	C1	2.2nF/630V	SM0805	TDK	C3216X7R2J222K
2	10	C2,C3,C4,C5,C18, C19,C20,C50,C52,C53	0.1uF	SM0805		
3	1	C6	680uF	SM/CT_7343	Sanyo	4TPB680M
4	3	C7,C8,C9	100uF	SM/C_1812	TDK	C4532X5ROJ107MT
5	3	C10,C11,C12	1u,100V	SM/C_1210	TDK	C3225X7R2A105K
6	1	C13	22nF/100V	SM1206	TDK	C3216X7R2J223M
8	1	C16	47uF/16V	SM/CT_7343	Sanyo	16TQC47M
9	1	C17	180pF	SM0805		
10	1	C21	100pF	SM0805		
11	2	C25,C22	220pF	SM0805		
12	1	C24	1uF	SM0805		
13	1	C26	47nF	SM0805		
14	1	C27	0(short)	SM0805		
15	5	D1,D2,D5,D10,D21	1N4148WS	SOD123	Vishay	1N4148WS
16	1	D3	MMSZ4702(15V)	SOD123	On Semi	MMSZ4702T1
17	2	D4,D8	MMSZ4698(11V)	SOD123	On Semi	MMSZ4698T1
18	3	D6,D9,D11	SL04	SOD123	Vishay	SL04
19	1	D20	MMSZ4697(10V)	SOD123	On Semi	MMSZ4697T1
20	1	L1	1.3uH	PCC-S1	Panasonic	ETQPAF1R3EFA
22	4	M3,M4,M8,M10	Si4842DY	SO-8	Vishay	Si4842DY
23	1	M5	IRF6216	SO-8	I. R.	IRF6216
24	3	M7,M9,M14	SI2308	SOT-23	Vishay	SI2308
25	1	M13	Si4488DY	SO-8	Vishay	Si4488DY
26	1	Q1	FMMT618	SOT-23	Zetex	FMMT618
27	1	Q3	FZT853	SM/SOT223	Zetex	FZT853
28	2	Q5,Q6	FMMT718	SOT-23	Zetex	FMMT718
29	1	Q10	FMMT493	SOT-23	Zetex	FMMT493
30	1	R1	5.11	SM0805		
31	4	R2,R12,R25,R32	5.1K	SM0805		
32	1	R3	5.11K	SM0805		
33	9	R8,R9,R10,R19, R28,R30,R35,R43,R63	10K	SM0805		
35	1	R16	1K	SM0805		

**POWER MANAGEMENT**
**SC4810E Evaluation Board - BOM**

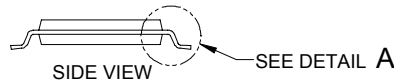
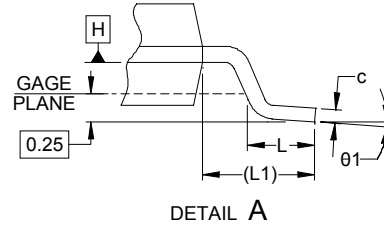
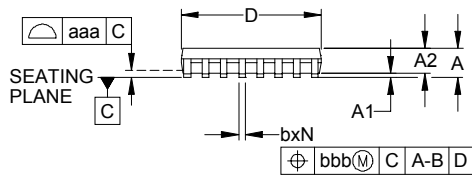
36	3	R17,R18,R34	1K	SM0805		
37	1	R20	8.2	SM0805		
38	1	R21	1.1M	SM0805		
39	1	R22	2	SM0805		
40	1	R23	160K	SM0805		
41	1	R24	100K	SM0805		
42	1	R29	6.34K	SM0805		
43	2	R31,R36	7.5K	SM0805		
44	2	R33,R37	80.6K	SM0805		
45	1	R38	1.47K	SM0805		
46	1	R40	15.8K	SM0805		
47	1	R42	2.4K	SM0805		
48	1	R44	1.5K	SM0805		
49	1	R52	51	SM0805		
50	3	R54,R56,57	5.1	SM0805		
51	1	R61	200K	SM0805		
52	1	R62	4.75K	SM0805		
54	1	T1	PA0944G	PA0646	Pulse	PA0944G
55	1	T3	P8208T	P8208	Pulse	P8208T
56	1	U1	MOCD207	SO-8	Fairchild	MOCD207
57	1	U2	SC1302A	MSOP-8	<b>Semtech</b>	SC1302A
58	1	U3	SC4810	TSSOP16	<b>Semtech</b>	SC4810
59	2	U4,U6	SC431	SOT-23	<b>Semtech</b>	SC431

POWER MANAGEMENT

Outline Drawing - TSSOP-16

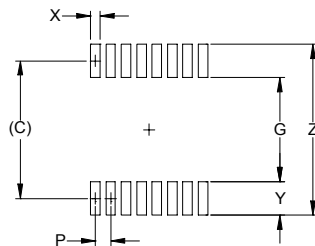


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.192	.196	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(0.039)			(1.0)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **E-H**.
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MO-153, VARIATION AB.

Land Pattern - TSSOP-16



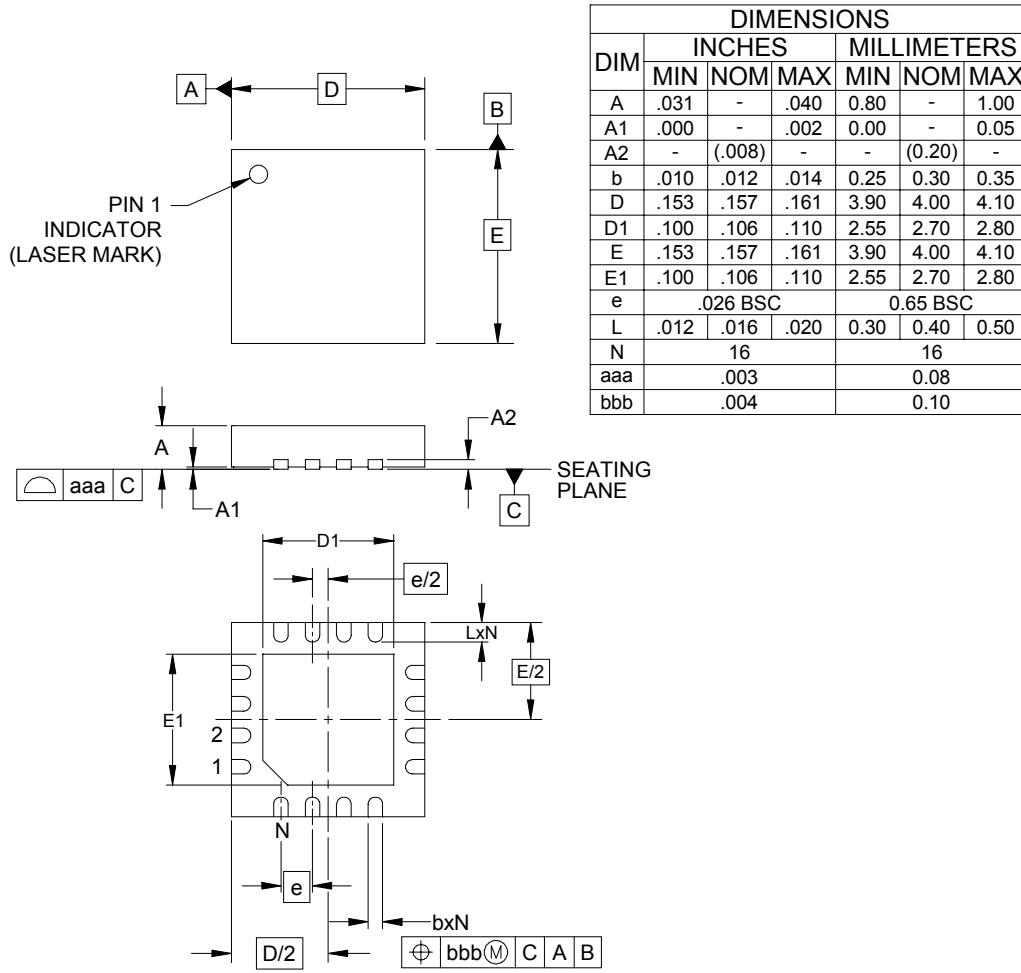
DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.



POWER MANAGEMENT

Outline Drawing - MLPQ-16, 4 x 4

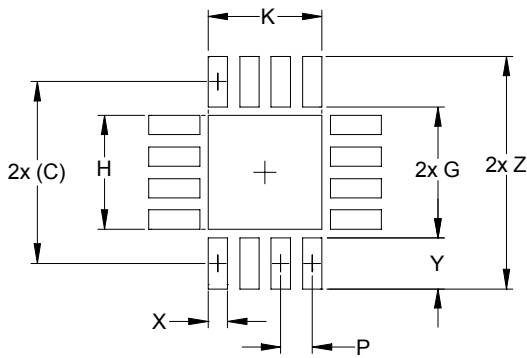


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**POWER MANAGEMENT**

**Land Pattern - MLPQ-16, 4 x 4**



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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