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POWER MANAGEMENT

Features

- Seven LED backlight sinks with 32 current settings from 0mA to 25mA
- Up to four LED backlight banks
- Lighting effects — fade-in/fade-out, breathe, blink, auto-dim full, and auto-dim partial functions
- ADP (Automatic Dropout Prevention) for backlights
- ALS (Ambient Light Sense) option sets the backlight brightness according to ambient lighting conditions
- I²C Bus fast mode and standard mode
- IRQ (Interrupt request) — open-drain output indicates a change of state for the ALS
- Backlight current accuracy — $\pm 1.5\%$ typical
- Backlight current matching — $\pm 0.5\%$ typical
- Four programmable 200mA low-noise LDO regulators
- PWM interface (200Hz to 50kHz) with internal digital low-pass filter
- Automatic sleep mode with all LEDs off
- Shutdown current — 0.1 μ A typical
- Ultra-thin package — 3 x 3 x 0.6 (mm)
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD modules
- Portable media players and digital cameras
- Personal navigation devices
- Display/keypad backlighting and LED indicators

Description

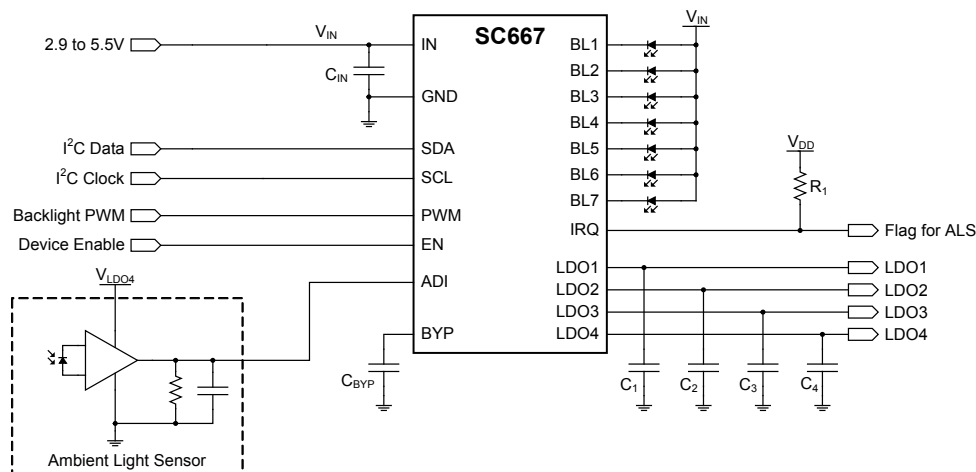
The SC667 is a highly integrated light management unit that provides programmable current for up to seven LED current sinks. Four LED banks are provided to allow settings for various LED zones or indicators. Four low-noise LDOs with programmable outputs ranging from 1.2V to 3.3V and 200mA maximum output current are also included.

ADP limits the maximum LED current to a level that ensures the LEDs maintain matched currents when the supply voltage approaches dropout. This feature produces acceptable light output at low supply voltage levels without requiring a boost converter or charge pump.

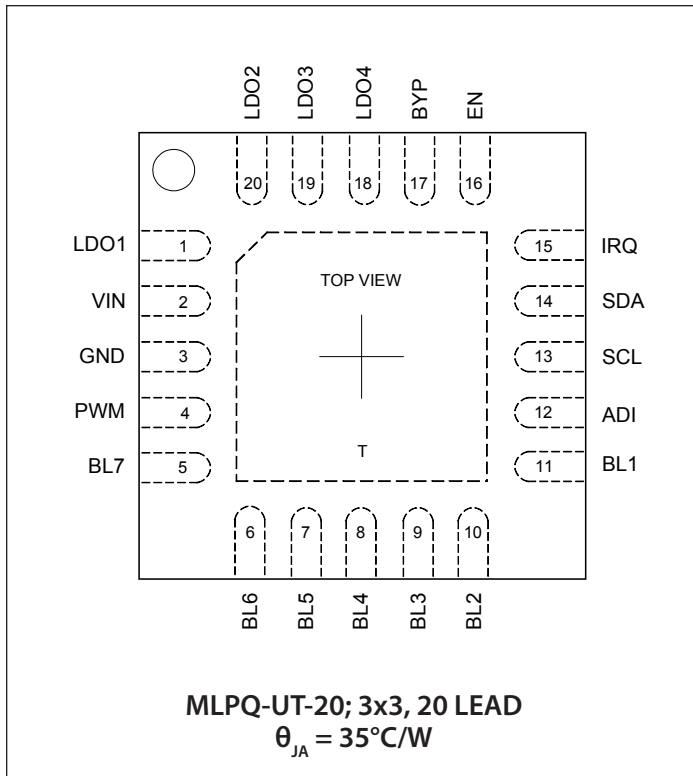
Two interfaces are provided for design flexibility. The I²C interface controls the LED on/off functions, assigns the LEDs to backlight banks, programs the LED currents, programs the lighting effects, enables the LDOs, and sets the LDO output voltages. The PWM interface reduces the current setting for LED bank #1 by a factor equal to the duty cycle of the applied PWM signal. A filter at the PWM input converts the pulsed signal to a DC current level, resulting in less switching noise compared to pulsed current methods.

The ADI input translates the voltage from an external ALS (Ambient Light Sensor) into a digitized code using a sigma-delta ADC. This block includes level detection to adjust the current setting of bank #1 with two different programmable levels based on the ambient light level. An interrupt output transitions low to notify the host processor that a level adjustment has been made.

Typical Application Circuit



Pin Configuration



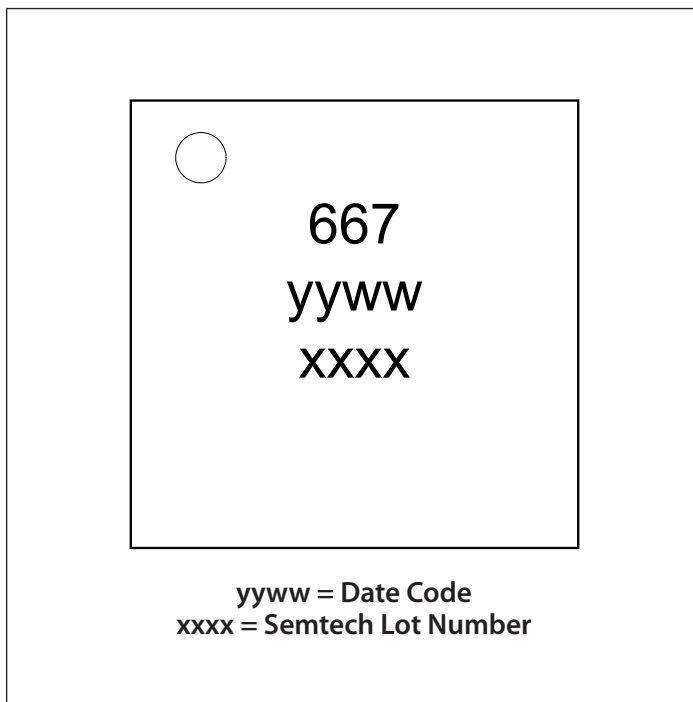
Ordering Information

| Device | Package |
|------------------------------|------------------|
| SC667ULTRT ⁽¹⁾⁽²⁾ | MLPQ-UT-20 3x3 |
| SC667EVB | Evaluation Board |

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Lead-free package only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



Absolute Maximum Ratings

| | |
|--|----------------------------|
| Pin Voltage — IN (V) | -0.3 to +6.0 |
| Pin Voltage — All Other Pins (V) | -0.3 to ($V_{IN} + 0.3$) |
| LDO ⁿ Short Circuit Duration | Continuous |
| ESD Protection Level ⁽²⁾ (kV) | 4.5 |

Recommended Operating Conditions

| | |
|-------------------------------------|------------------------------|
| Ambient Temperature Range (°C)..... | $-40 \leq T_A \leq +85$ |
| Input Voltage (V) | $2.9 \leq V_{IN} \leq 5.5$ |
| Backlight Sink Voltage (V) | $0.05 \leq V_{BLn} \leq 4.2$ |

Thermal Information

| | |
|--|-------------|
| Thermal Resistance, Junction to Ambient ⁽³⁾ (°C/W) | 35 |
| Storage Temperature Range (°C)..... | -65 to +150 |
| Peak IR Reflow Temperature (10s to 30s) (°C) | +260 |

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

- Subscripting for all LDOs (LDO_n), n = 1, 2, 3, 4.
- Tested according to JEDEC standard JESD22-A114-B.
- Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, $T_A = +25^\circ\text{C}$ for Typ, -40°C to $+85^\circ\text{C}$ for Min and Max, $T_{J(\text{MAX})} = 125^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $C_{IN} = C_{LDO1} = C_{LDO2} = C_{LDO3} = C_{LDO4} = 1.0\mu\text{F}$, $C_{BYP} = 22\text{nF}$, (ESR = 0.03Ω)⁽¹⁾

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|------------------------------|--|------|-----------|------|---------------|
| Supply Specifications | | | | | | |
| Input Supply Voltage | V_{IN} | | 2.9 | | 5.5 | V |
| Shutdown Current | $I_{Q(\text{OFF})}$ | Shutdown, $V_{IN} = 4.2\text{V}$ | | 0.1 | 2.0 | μA |
| Total Quiescent Current | I_Q | Sleep (all LDOs off), $EN = V_{IN}^{(2)}$ | | 90 | 135 | μA |
| | | Sleep (all LDOs on), $EN = V_{IN}^{(2)}$ | | 300 | 450 | |
| | | 7 LEDs on | | 1.4 | | mA |
| LED Sink Electrical Specifications | | | | | | |
| Maximum Total Backlight Current | $I_{\text{OUT}(\text{MAX})}$ | Sum of all active LED currents, V_{IN} above dropout level | | 175 | | mA |
| Backlight Current Setting Range | I_{BL} | Nominal setting for BL1 – BL7 | 0 | | 25 | mA |
| Backlight Current Accuracy | I_{BL_ACC} | $I_{BLn}^{(3)} = 12\text{mA}$ | | ± 1.5 | | % |
| Backlight Current Matching ⁽⁴⁾ | I_{BL-BL} | $I_{BLn}^{(3)} = 12\text{mA}$ | -3.5 | ± 0.5 | +3.5 | % |
| Dropout Voltage ⁽⁵⁾ | V_{DO} | One bank of 6 backlights set equal to 20mA | | 59 | | mV |
| Current Sink Off-State Leakage Current | $I_{BL/FL(\text{OFF})}$ | $V_{IN} = V_{BLn}^{(3)} = 4.2\text{V}$ | | 0.1 | 1 | μA |

Electrical Characteristics (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|--------------------|---|------|-----------|------|---------------------|
| LDO Electrical Specifications | | | | | | |
| LDO1, LDO3, and LDO4 Voltage Setting Range | $V_{LDOm}^{(6)}$ | Range of nominal settings | 1.5 | | 3.3 | V |
| LDO2 Voltage Setting Range | V_{LDO2} | Range of nominal settings | 1.2 | | 1.8 | V |
| Output Voltage Accuracy | ΔV_{LDO} | $I_{LDOm}^{(6)} = 1\text{mA}, T_A = 25^\circ\text{C}, 2.9\text{V} \leq V_{IN} \leq 4.2\text{V}$ | -3 | ± 1.0 | +3 | % |
| | | $I_{LDOm}^{(6)} = 1\text{mA to } 100\text{mA}, 2.9\text{V} \leq V_{IN} \leq 4.2\text{V}$ | -3.5 | | +3.5 | % |
| Dropout Voltage | $V_{Dm}^{(6)}$ | $I_{LDOm}^{(6)} = 150\text{mA}, V_{IN} = V_{LDOm} + V_{Dm}$ | | 150 | 200 | mV |
| | V_{D2} | $I_{LDO2} = 100\text{mA}, V_{IN} = V_{LDO2} + V_{D2}$ | | 100 | 150 | |
| Current Limit | I_{LIM} | | 200 | | | mA |
| Line Regulation | ΔV_{LINE} | $I_{LDOm}^{(6)} = 1\text{mA}, V_{IN} = 2.9\text{V to } 4.2\text{V}, V_{LDOm} = 2.8\text{V}$ | | 2.1 | 7.2 | mV |
| | | $I_{LDO2} = 1\text{mA}, V_{IN} = 2.9\text{V to } 4.2\text{V}, V_{LDO2} = 1.8\text{V}$ | | 1.3 | 4.8 | |
| Load Regulation | ΔV_{LOAD} | $V_{LDOm}^{(6)} = 3.3\text{V}, I_{LDOm} = 1\text{mA to } 100\text{mA}$ | | 10 | 25 | mV |
| | | $V_{LDO2} = 1.8\text{V}, I_{LDO2} = 1\text{mA to } 100\text{mA}$ | | 8 | 20 | |
| Power Supply Rejection Ratio | $PSRR_m^{(6)}$ | $1.5\text{V} < V_{LDOm} < 3.0\text{V}, f < 10\text{kHz}, C_{BYP} = 22\text{nF}, I_{LDOm} = 50\text{mA}, \text{with } 0.5\text{V}_{p-p} \text{ supply ripple}$ | | 53 | | dB |
| | $PSRR_2$ | $1.2\text{V} < V_{LDO2} < 1.8\text{V}, f < 10\text{kHz}, C_{BYP} = 22\text{nF}, I_{LDO2} = 50\text{mA}, \text{with } 0.5\text{V}_{p-p} \text{ supply ripple}$ | | 61 | | |
| Output Voltage Noise | $e_{n-LDOm}^{(6)}$ | $10\text{Hz} < f < 100\text{kHz}, C_{BYP} = 22\text{nF}, C_{LDOm} = 1\mu\text{F}, I_{LDOm} = 50\text{mA}, 1.5\text{V} < V_{LDOm} < 3.0\text{V}$ | | 67 | | μV_{RMS} |
| | e_{n-LDO2} | $10\text{Hz} < f < 100\text{kHz}, C_{BYP} = 22\text{nF}, C_{LDO2} = 1\mu\text{F}, I_{LDO2} = 50\text{mA}, 1.2\text{V} < V_{LDO2} < 1.8\text{V}$ | | 47 | | |
| Minimum LDO Capacitor ⁽¹⁾ | $C_{LDO(MIN)}$ | Nominal value for $C_{LDOm}^{(6)}$ | 1 | | | μF |
| ADC Specifications | | | | | | |
| Resolution | AD_{RES} | | | 8 | | bits |
| Offset | AD_{OFFSET} | $V_{LDO4} = 3.3\text{V}$ | | 1 | | LSB |
| Gain Error | AD_{GAIN_ERR} | $V_{LDO4} = 3.3\text{V}$ | | 0.1 | | % |
| Integral Non-Linearity | INL | $V_{LDO4} = 3.3\text{V}$ | | 1 | | LSB |

Electrical Characteristics (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---------------|---|------|-----|-----|---------|
| Digital Input Electrical Specifications (PWM, EN, SDA, SCL) | | | | | | |
| Input High Threshold ^{(7) (8)} | V_{IH} | $V_{IN} = 5.5V$ | 1.6 | | | V |
| Input Low Threshold ^{(7) (8)} | V_{IL} | $V_{IN} = 2.9V$ | | | 0.4 | V |
| Input High Current | I_{IH} | $V_{IN} = 5.5V$ | -1 | | +1 | μA |
| Input Low Current | I_{IL} | $V_{IN} = 5.5V$ | -1 | | +1 | μA |
| Digital Output Electrical Specification (IRQ) | | | | | | |
| IRQ Output Low Level | V_{OL} | $I_{IRQ} \leq 3mA$ | | | 0.4 | V |
| PWM Input Specification (PWM) | | | | | | |
| PWM Input Frequency | f_{PWM} | | 0.2 | | 50 | kHz |
| I²C Interface | | | | | | |
| Interface complies with slave mode I ² C interface as described by Philips I ² C specification version 2.1 dated January, 2000. | | | | | | |
| Digital Input Voltage ⁽⁷⁾ | V_{B-IL} | | | | 0.4 | V |
| | V_{B-IH} | | 1.6 | | | V |
| SDA Output Low Level | | $I_{DIN} (SDA) \leq 3mA$ | | | 0.4 | V |
| Digital Input Current | I_{B-IN} | | -0.2 | | 0.2 | μA |
| Hysteresis of Schmitt Trigger Inputs | V_{HYS} | | | 0.1 | | V |
| Maximum Glitch Pulse Rejection | t_{SP} | | | 50 | | ns |
| I/O Pin Capacitance | C_{IN} | | | 10 | | pF |
| I²C Timing | | | | | | |
| Clock Frequency ⁽⁷⁾ | f_{SCL} | | | 400 | 440 | kHz |
| SCL Low Period ^{(7) (8)} | t_{LOW} | | 1.3 | | | μs |
| SCL High Period ^{(7) (8)} | t_{HIGH} | | 0.6 | | | μs |
| Data Hold Time ^{(7) (8)} | t_{HD_DAT} | | 0 | | | μs |
| Data Setup Time ^{(7) (8)} | t_{SU_DAT} | | 100 | | | ns |
| Setup Time for Repeated START Condition ^{(7) (8)} | t_{SU_STA} | | 0.6 | | | μs |
| Hold Time for Repeated START Condition ^{(7) (8)} | t_{HD_STA} | | 0.6 | | | μs |
| Setup Time for STOP Condition ^{(7) (8)} | t_{SU_STO} | | 0.6 | | | μs |
| Bus-Free Time Between STOP and START ^{(7) (8)} | t_{BUF} | | 1.3 | | | μs |
| Interface Start-up Time ^{(7) (8)} | t_{EN} | Bus start-up time after EN pin is pulled high | | | 900 | μs |

Electrical Characteristics (continued)

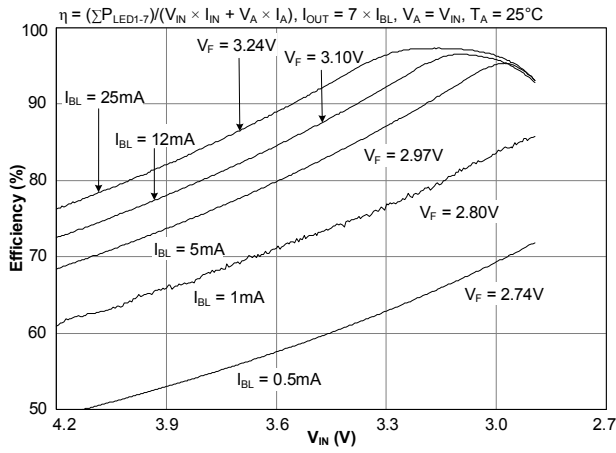
| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------|----------------|---------------------|-----|-----|-----|-------|
| Fault Protection | | | | | | |
| Over-Temperature | T_{OTP} | Rising threshold | | 165 | | °C |
| | T_{HYS} | Hysteresis | | 30 | | °C |
| Under Voltage Lockout | V_{UVLO} | Increasing V_{IN} | | 2.4 | | V |
| | $V_{UVLO-HYS}$ | | | 500 | | mV |

Notes:

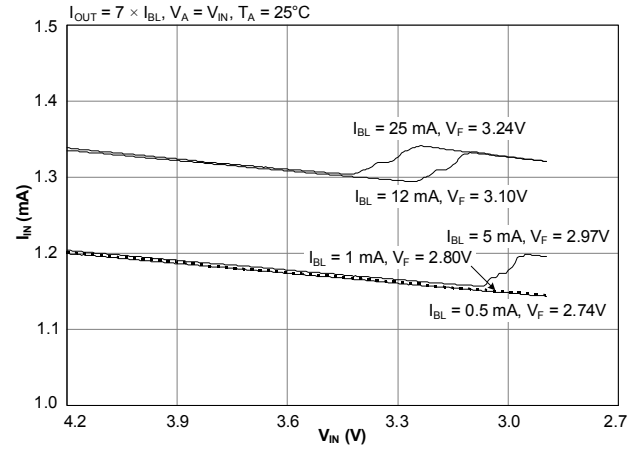
- (1) Capacitors are MLCC of X5R type.
- (2) EN is high for more than 10ms.
- (3) Subscript for all backlights (BLn), n = 1, 2, 3, 4, 5, 6, and 7.
- (4) Current matching is defined as $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.
- (5) V_{DO} is defined as the voltage at the BLn pin when current has dropped from the target value by 10%.
- (6) Subscript m = 1, 3, and 4 and applies only to LDO1, LDO3, and LDO4. Subscripting for all LDOs (LDO_n), n = 1, 2, 3, 4.
- (7) The host processor must meet these limits.
- (8) Guaranteed by design.

Typical Characteristics — Backlights

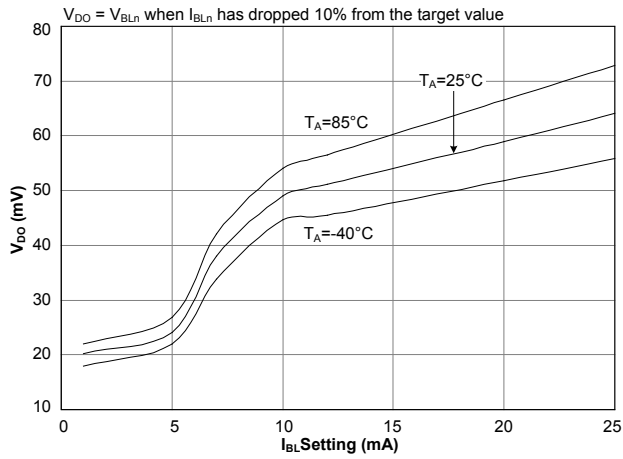
Backlight Efficiency (7 LEDs)



Supply Current (7 LEDs)

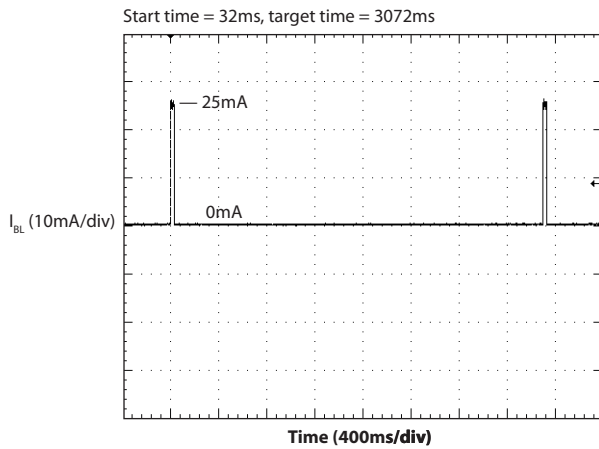


Dropout Voltage V_{DO} vs I_{BL} (6 LEDs)

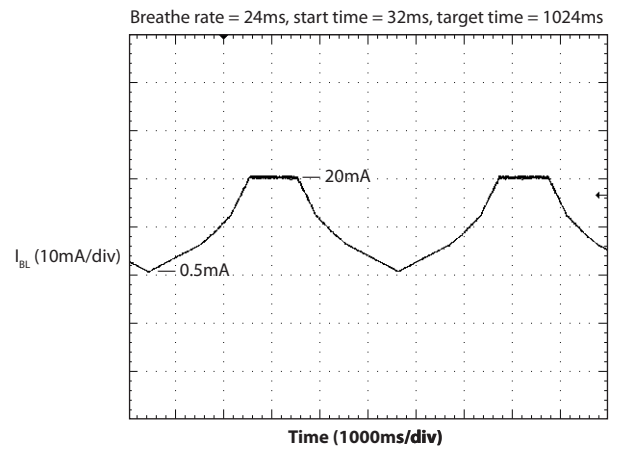


Typical Characteristics — Backlights (continued)

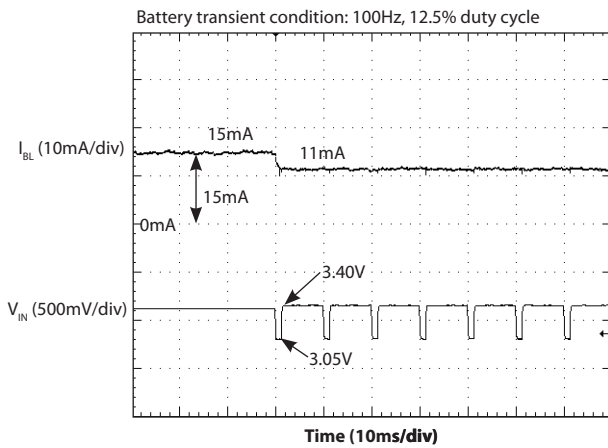
Group #1 Blink Function (25mA)



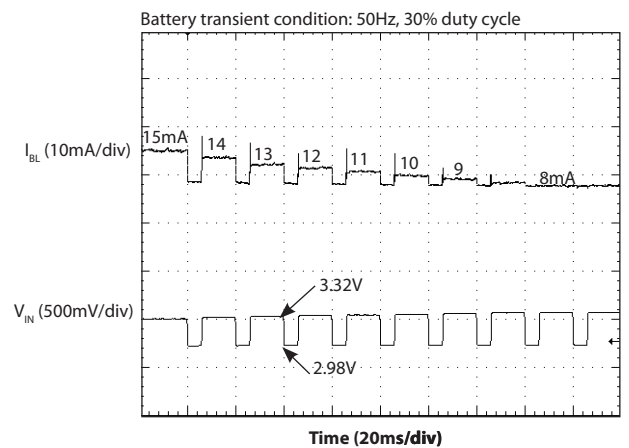
Group #1 Breathe Function (20mA to 0.5mA)



Bank #1 with ADP (rate = 256 μ s)

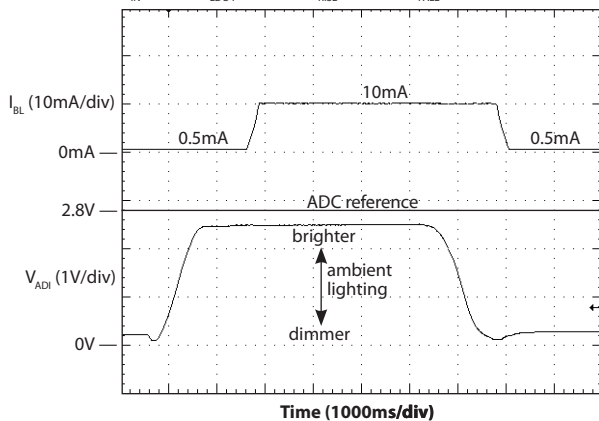


Backlight with ADP (rate = 4ms)



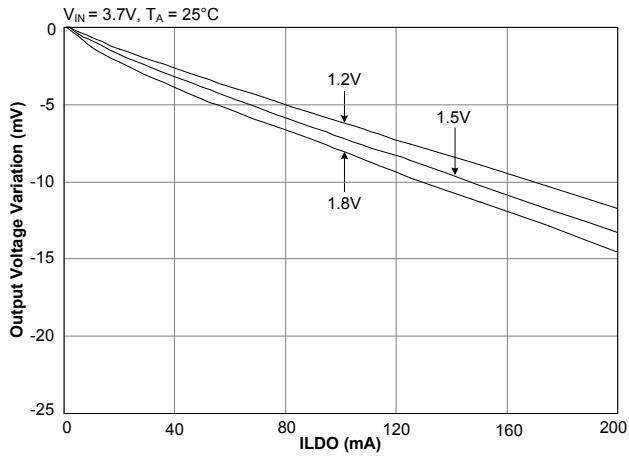
Backlight Dimming with ALS and Fade

$V_{IN} = 3.7V, V_{LD04} = 2.8V, AD_{RISE} = 80h, AD_{FALL} = 80h, 4ms$ fade rate

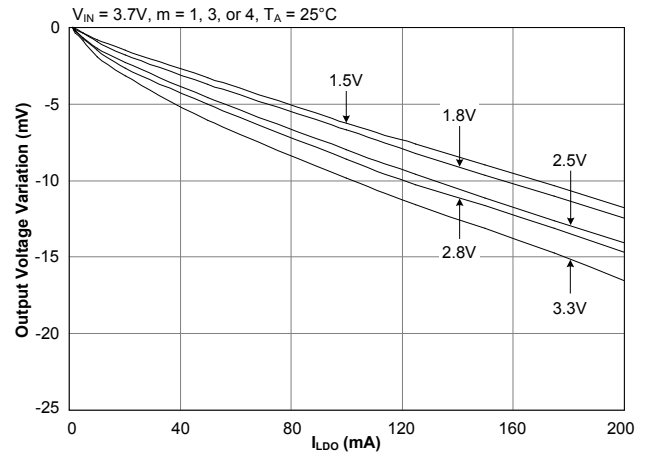


Typical Characteristics — LDOs

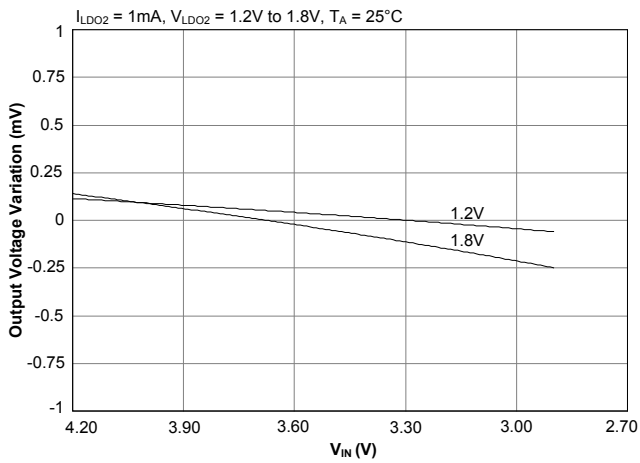
Load Regulation (LDO2)



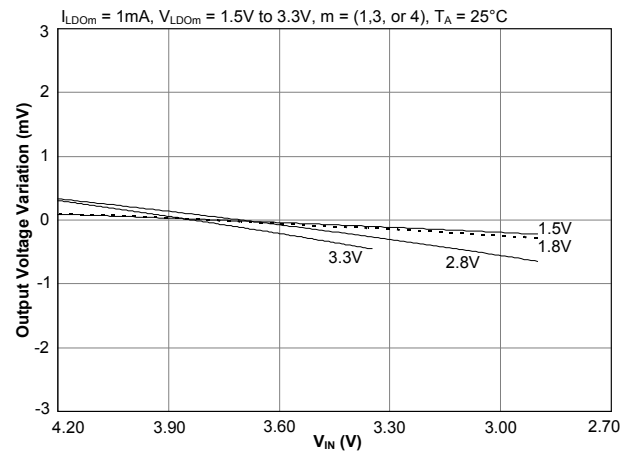
Load Regulation (LDOm)



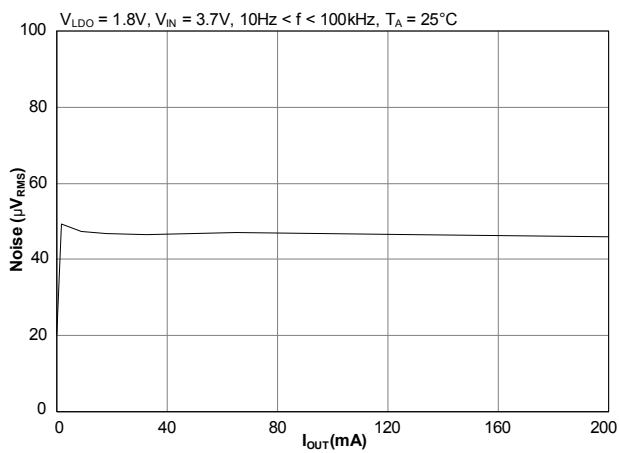
Line Regulation (LDO2)



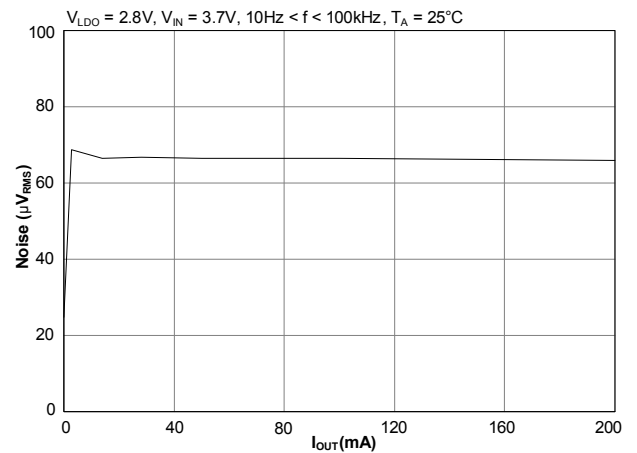
Line Regulation (LDOm)



LDO Noise vs. Load Current (1.8V)

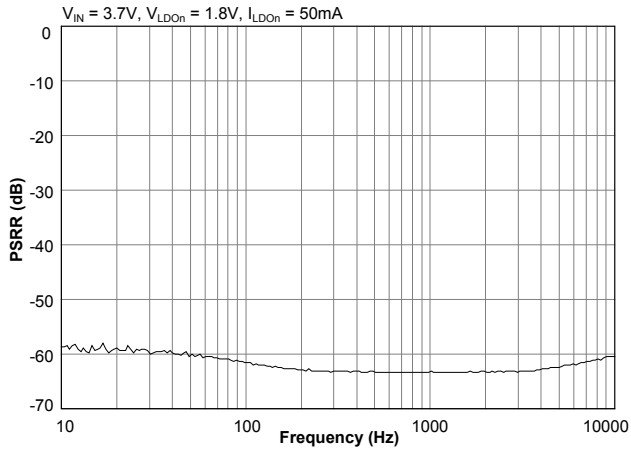


LDO Noise vs. Load Current (2.8V)

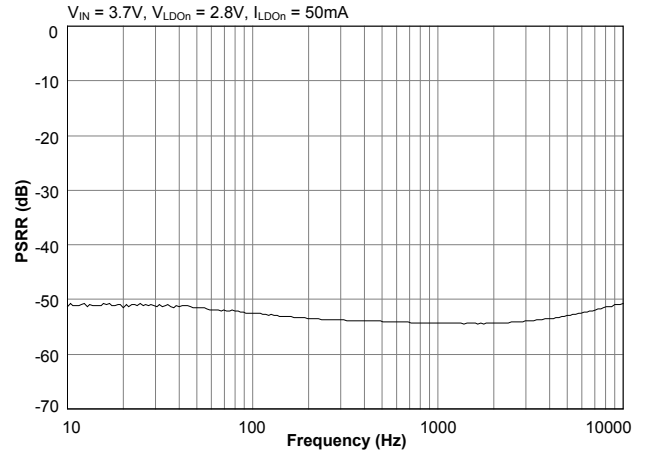


Typical Characteristics — LDOs (continued)

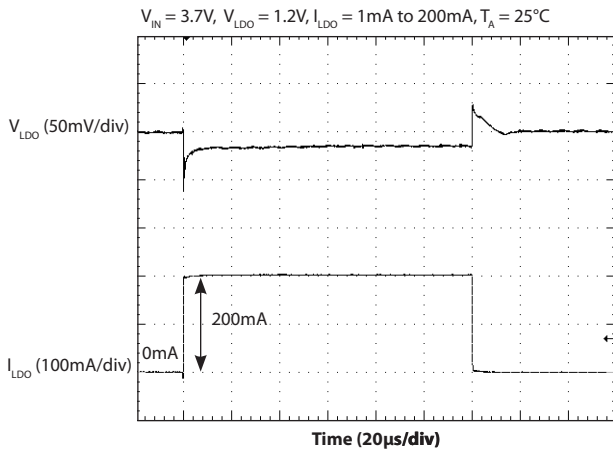
PSRR vs. Frequency (1.8V)



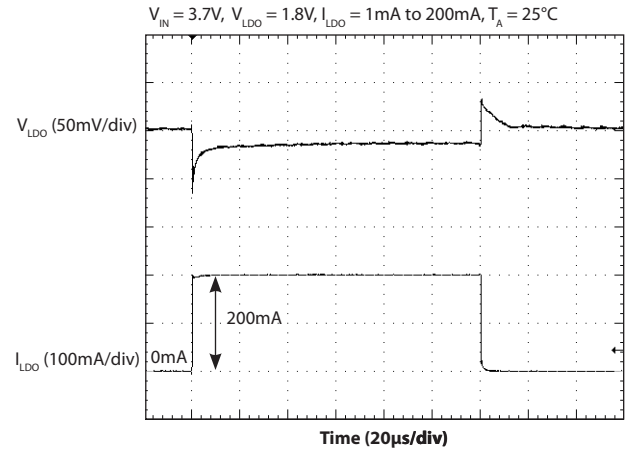
PSRR vs. Frequency (2.8V)



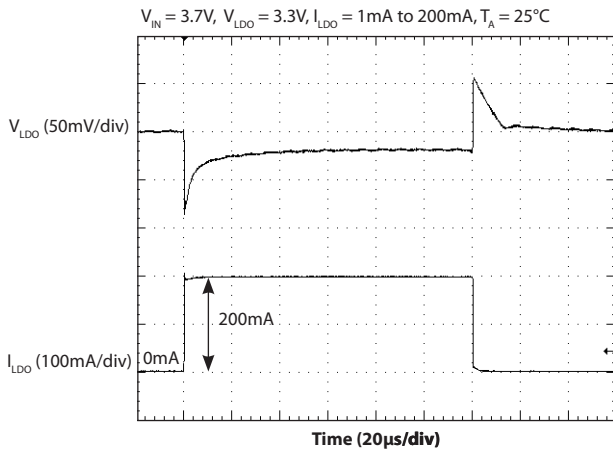
Load Transient Response (1.2V)



Load Transient Response (1.8V)



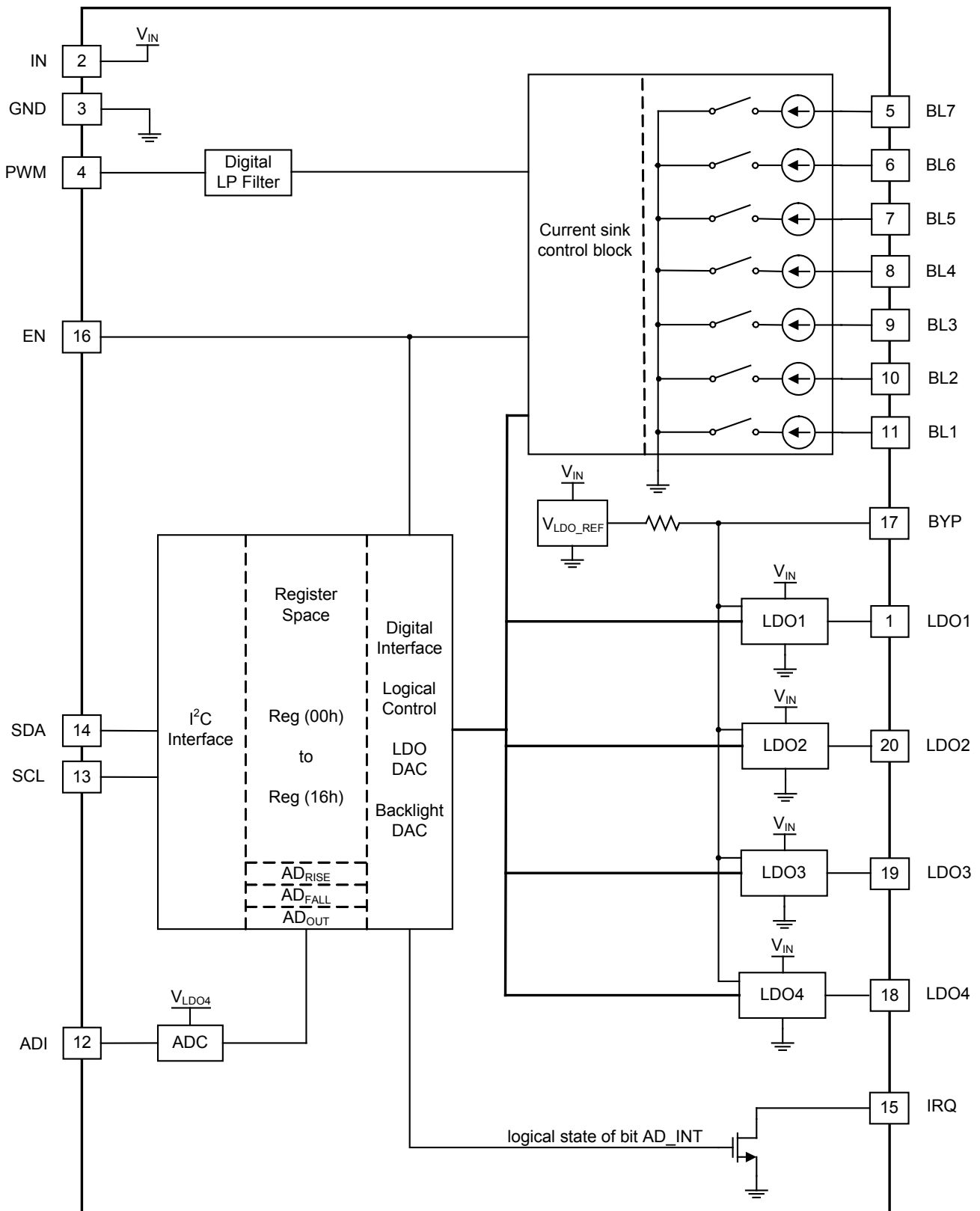
Load Transient Response (3.3V)



Pin Descriptions

| Pin # | Pin Name | Pin Function |
|-------|-------------|---|
| 1 | LDO1 | LDO1 output |
| 2 | VIN | Battery voltage input |
| 3 | GND | Ground pin |
| 4 | PWM | Backlight PWM control signal input |
| 5 | BL7 | Current sink output for backlight LED 7 — leave this pin open or grounded if unused |
| 6 | BL6 | Current sink output for backlight LED 6 — leave this pin open or grounded if unused |
| 7 | BL5 | Current sink output for backlight LED 5 — leave this pin open or grounded if unused |
| 8 | BL4 | Current sink output for backlight LED 4 — leave this pin open or grounded if unused |
| 9 | BL3 | Current sink output for backlight LED 3 — leave this pin open or grounded if unused |
| 10 | BL2 | Current sink output for backlight LED 2 — leave this pin open or grounded if unused |
| 11 | BL1 | Current sink output for backlight LED 1 — leave this pin open or grounded if unused |
| 12 | ADI | ADC input — connect this pin to ground if unused |
| 13 | SCL | I ² C clock input — I ² C buss pull-up resistor is required. |
| 14 | SDA | I ² C data — bi-directional line used for read and write operations for all internal registers (refer to Register Map and I ² C Interface sections) — I ² C buss pull-up resistor is required. |
| 15 | IRQ | Interrupt request — open-drain output, active-low |
| 16 | EN | Chip enable — active high |
| 17 | BYP | Bypass pin for LDO reference — connect a 22nF ceramic capacitor to GND |
| 18 | LDO4 | LDO4 output |
| 19 | LDO3 | LDO3 output |
| 20 | LDO2 | LDO2 output |
| T | THERMAL PAD | Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally |

Block Diagram



Applications Information

General Description

The SC667 is optimized for handheld applications supplied from a single cell Li-Ion and includes the following key functions:

- Seven matched current sinks — BL1, BL2, BL3, BL4, BL5, BL6, and BL7 regulate LED backlighting current, with 0mA to 25mA per LED.
- Four adjustable LDOs — LDO1, LDO3, and LDO4 are adjustable with 15 settings from 1.5V to 3.3V. LDO2 is adjustable with 7 settings from 1.2V to 1.8V.
- ALS with a sigma-delta ADC that can also be used for general purpose ADC functions.
- PWM with an internal digital low-pass filter
- I²C Bus fast mode and standard mode

LED Backlight Current Settings

The backlight current is set via the I²C interface. The current is regulated to one of 32 values between 0mA and 25mA. The step size varies depending upon the current setting. The first three steps are 50μA, 100μA, and 200μA. Between 0.5mA and 5mA, the step size is 0.5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current range and coarse adjustment at higher current settings where larger changes are not visible. The settings are pseudo-logarithmic. A zero setting also disables the current sink, providing an alternative to the enable bit.

LED Backlight Current Sinks

Backlight current is independent of forward voltage mismatch (ΔV_f) between LEDs. When two or more backlight sinks are set to the same target current, their currents will match, even if the LED voltages are different. The backlight current sinks are designed with a low dropout voltage (typically 59mV for a bank of 6 LEDs at 20mA) to optimize run-time when the LED anode voltage is provided by a battery.

LED Anode Supply

In the typical application circuit, the battery voltage supplies the LEDs. An alternative to this configuration is to connect the LED anodes to a second DC supply as shown in Figure 1. Such a connection is especially useful when an alternate voltage that is slightly higher than the

forward voltage of the LEDs is available. The resulting efficiency in this scenario would be optimal. To achieve best accuracy, the current sink amplifier requires the LED sink pin (BLn) to be within the operational range of $V_{DO} \leq V_{BLn} \leq 4.2V$. When the sink is off, V_{BLn} may float as high as 5.5V.

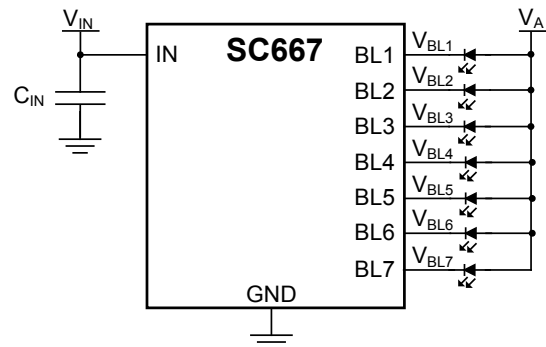


Figure 1 — Anode Supply

Unused Backlight Current Sinks

The backlight LEDs default to the off state upon power-up. For backlight applications using fewer than 7 LEDs, any unused output must be left open or grounded and the unused LED must remain disabled. When writing to the backlight enable register, a zero (0) must be written to the corresponding enable bit of any unused output.

Backlight Quiescent Current

The quiescent current required to operate the backlights is reduced when backlight current is less than 8.0mA. This feature results in higher efficiency under light-load conditions. Further quiescent current reduction will result from using fewer LEDs.

Backlight Configuration into Banks

The seven LED backlight drivers can be assigned to a single bank or divided among up to four independent banks — refer to the Register Map section for more details. The independent banks can each be configured with different settings for backlight current and fade operation.

Bank Configuration into Groups

The four backlight banks can be assigned to two groups (group #1 and group #2). Each group provides independent settings for the fade and breathe effect rate options. Each group also provides independent settings for target time and start time, which are used to customize the

Applications Information (continued)

blink and breathe lighting effects. Details of the fade, breathe, and blink effects are introduced later in this Applications Information section.

Target Backlight Settings for Lighting Effects

The target backlight setting is the current which will result at the end of a blink or breathe lighting effect cycle. The Register Map contains four control registers which set the target backlight currents for each bank. Registers 06h, 07h, 08h, and 09h contain the target current values for: bank #1, bank #2, bank #3, and bank #4, respectively.

Bank #1 also uses the target value of register 06h in association with the ALS function. Bank #1 can be set to automatically change to the target value of register 06h when the ADC exceeds a programmable rising threshold. ALS is defined in more detail under Ambient Light Sense, and in the Register Map section under ADC Function Register 12h.

Breathe Lighting Effect

The breathe lighting effect may be applied independently to each group. When this feature is enabled, the bank's backlight current will increase and decrease periodically at a rate that mimics calm and smooth breathing. Once initialized via the I²C interface, this function will run continuously, independent of the host processor, saving instruction cycles and simplifying timing requirements.

Three timing parameters must be set to define the breathe effect timing: effect rate, start time, and target time. Group #1 and group #2 have independent timing parameters to support a variety of options. When a bank is assigned to a group, it adopts the timing parameters of the respective group.

When enabled, the breathe function causes the backlights to change brightness by stepping the current incrementally, using the effect rate parameter, until the final backlight current is reached. The current will remain at the target value for a time set by the target time parameter. When the target time has ended, the brightness will again change, this time in reverse order, stepping the current incrementally, using the effect rate parameter, until the current returns to the start value. The current will remain at the start value for the time set by the start

time parameter. When the start time has ended, the breathe cycle begins again.

The breathe effect rate is programmable for group #1 and group #2 and can be independently set to 4, 8, 16, 24, 32, 48, or 64ms for each group. Also, the start time and target time parameters for group #1 and group #2 can be independently set to 32, 64, 256, 512, 1024, 2048, 3072, or 4096ms.

In addition to the group's timing parameters, start current and target current values and BxBEN (blink/breathe enable) and BxFEN (fade enable) bits are set for each bank to define that bank's min and max current during a breathe cycle and enable the breathe function.

The five parameters that define the breathe effect are:

1. Effect rate — write value to register 0Fh
2. Start current — write value to register 02h, 03h, 04h, or 05h (bank dependent)
3. Target current — write value to registers 06, 07h, 08h, or 09h (bank dependent)
4. Start time — write value to register 10h or 11h (group dependent)
5. Target time — write to register 10h or 11h (group dependent)

Figure 3 illustrates the breathe effect with respect to time. For an example of the breathe effect, with bank #1 assigned to group #1, the terms used in the illustration are as follows:

- I_{BL_START} = contents of register 02h (B1FEN must equal 1)
- I_{BL_TARGET} = contents of register 06h (B1BEN must equal 1)
- t_{START} = contents of bits ST1_[2:0] in register 10h
- t_{TARGET} = contents of bits TT1_[2:0] in register 10h
- $t_{BREATHE}$ = breathe time. Equal to the breathe rate times the number of steps between I_{BL_START} and I_{BL_TARGET} . Breathe time is set with the bits ER1_[2:0] in register 0Fh.

Blink Lighting Effect

The blink lighting effect provides an automatic LED blink-function that can be applied to a single LED driver or

Applications Information (continued)

an LED driver bank without any host processor interaction. Blinking can be initialized via the I²C interface at power up and the settings maintained in the SC667 registers with no need for additional software interaction.

Two timing parameters must be set to define the blink effect timing: start time and target time. Start and target times can be independently set to 32, 64, 256, 512, 1024, 2048, 3072, 4096ms. The total blink cycle time is equal to the sum of the start and target times.

In addition to timing parameters, start current and target current values are used to set the bank's min and max current, and a combination of bits BxBEN (blink/breathe enable) and BxFEN (fade enable) are used to enable the blink function.

The four parameters are:

1. Start current — write value to register 02h, 03h, 04h, or 05h (bank dependent)
2. Target current — write value to register 06, 07h, 08h, or 09h (bank dependent)
3. Start time — write value to register 10h or 11h (group dependent)
4. Target time — write to register 10h or 11h (group dependent)

Figure 4 illustrates the blink effect with respect to time. For an example of the blink effect, with bank #2 assigned to group #2, the terms used in the illustration are as follows:

- I_{BL_START} = contents of register 03h (B2FEN must equal 0)
- I_{BL_TARGET} = contents of register 07h (B2BEN must equal 1)
- t_{START} = contents of bits ST2_[2:0] in register 11h
- t_{TARGET} = contents of bits TT2_[2:0] in register 11h

Backlight Fade-In and Fade-Out Lighting Effects

When enabled, the fade function causes the backlights to change brightness by stepping the current incrementally until the final backlight current is reached. The backlight fade-in and fade-out may be applied to selected banks. When enabled, the bank current will gradually increase during fade-in and gradually decrease during fade-out. The rate of increase or decrease is programmable for

group #1 and group #2 and can be independently set to 1, 2, 4, 6, 8, 12, or 16ms for each group. The fade function causes the bank to begin stepping from its current state to the next programmed state as soon as the new state is stored in its register. For example, if the bank is set to 25mA, fade is enabled, and the bank is changed to 0mA, the bank will step from 25mA down to 0mA using all settings between 25mA and 0mA.

In addition to the 32 programmable backlight current values, there are also 75 non-programmable current steps. The non-programmable steps are active only during a fade or breathe operation to provide for a very smooth change in backlight brightness. Backlight current steps proceed at a programmable fade rate of 1, 2, 4, 6, 8, 12, or 16ms. The exact length of time used to fade between any two backlight values is determined by multiplying the fade rate by the number of steps between the old and new backlight values. The fade time can be calculated from the data provided in Table 1 on page 19.

Two parameters must be programmed to enable the fade effects: effect rate and start current. The fade function will begin when a new start current is set along with the FEN bit in the associated register.

The fade effect rate parameter must be set to define the fade timing. Group #1 and group #2 have independent sets of timing parameters to support a variety of fade timing options. When a bank is assigned to a group, it adopts the timing parameters of the respective group.

Registers associated with fade are described below:

1. Effect Rate — write a value to register 0Fh (group dependent)
2. Start Current — write value to register 02h, 03h, 04h, or 05h (bank dependent)

Figure 5 illustrates the fade-in and fade-out effects with respect to time. For an example of the fade effects assigned to bank 3 with effect rate 2, the terms in the illustration are as follows:

- $I_{BL_INITIAL}$ = contents of register 04h (B3FEN must equal 1)

Applications Information (continued)

- I_{BL_FINAL} = new value written to register 04h (register 07h bit B3BEN must equal 0), however, the “Target” value of register 07h has no effect on fade.
- t_{FADE_IN} = contents of bits ER2_[2:0] in register 0Fh
- $t_{FADE_OUT} = t_{FADE_IN}$

Auto-Dim Lighting Effect

Two auto-dim settings are provided — auto-dim full and auto-dim partial. These settings provide automatic dimming of bank #1. The auto-dim delay times are set using the group #1 target and start time register (10h). Delay times are 8 times the group #1 target and start times.

Auto-dim full provides a time-out and dimming function followed by a time-out and turn-off function. Auto-dim full begins when the bank is enabled (or re-enabled), the bank will first go to the target current and wait for a count of 8 times the group #1 target time. The bank will then dim to the “start” current and wait for a count of 8 times the group #1 start time. The bank will then turn off.

Auto dim partial provides the time-out and dimming function, but does not turn off backlights. Auto-dim partial begins when the bank is enabled (or re-enabled), the bank will first go to the target current and wait for a count of 8 times the group #1 target time. The bank will then dim to the “start” current. The bank will not turn off automatically.

Auto-dim is available only for group #1. After selecting an auto-dim option, the bank’s blink effect must be enabled to enable auto-dim. The bank must then be enabled or re-enabled to begin the auto-dim. Auto-dim partial is illustrated in Figure 6, and auto-dim full is illustrated in Figure 7.

Brightness Change without Effects

There are two ways to change brightness while using no lighting effect. One way is to set the effect rate option to the zero value “snap to target” (a function of register 0Fh). This method will block all lighting effects on all banks within a group. Another way to change brightness, with no lighting effect, is to set the BxFEN and BxBEN both equal to zero. This second method will block all lighting effects on a single bank, and with no influence over other banks within the group.

Writing a new value to the backlight current register, while effects are disabled, will cause the change in brightness to

occur immediately. When changing brightness without effects, registers 02h through 05h are used for this function. The target values of registers 06h through 09h are not involved.

Figure 8 illustrates the brightness change with respect to time. An example of brightness change to bank #4 with no lighting effect, is as follows:

- $I_{BL_INITIAL}$ = previous value written to register 05h
- I_{BL_FINAL} = new value written to register 05h

The register 05h bit B4FEN must equal 0, and register 09h bit B4BEN must equal 0, however, the “Target” value of register 09h has no effect on the final current.

Fade State Diagram

The state diagram in Figure 2 describes the fade operation. If the backlight enable bits are disabled during an

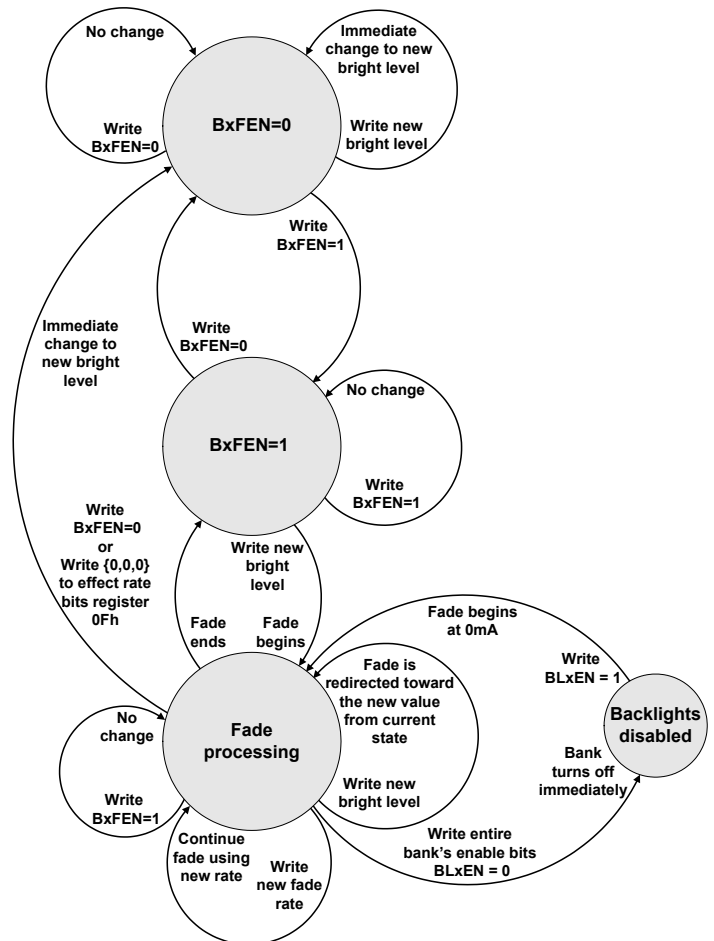
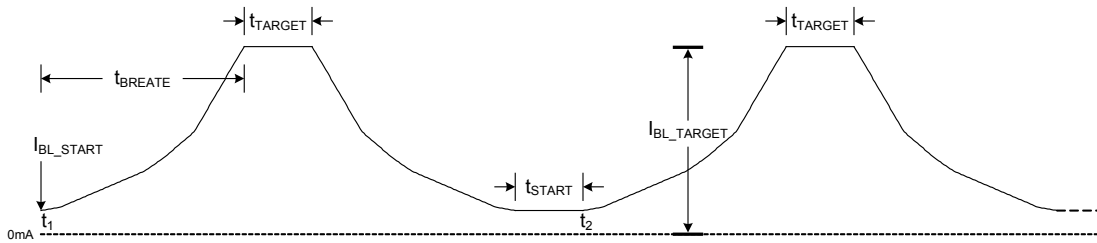
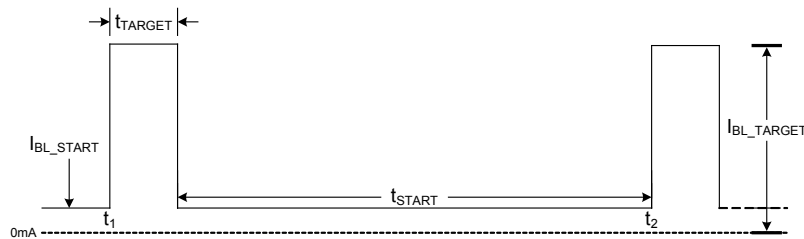
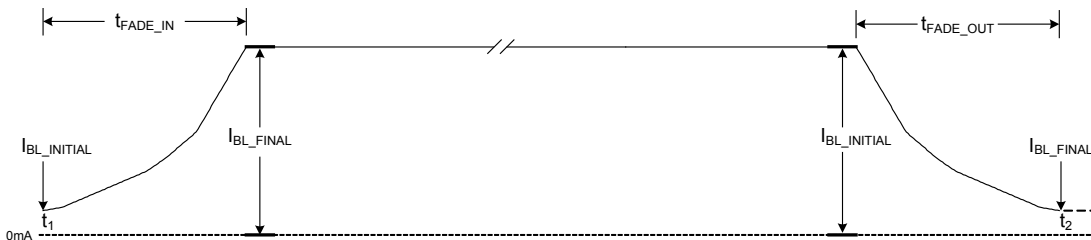
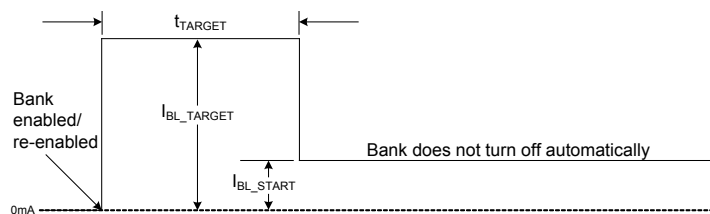
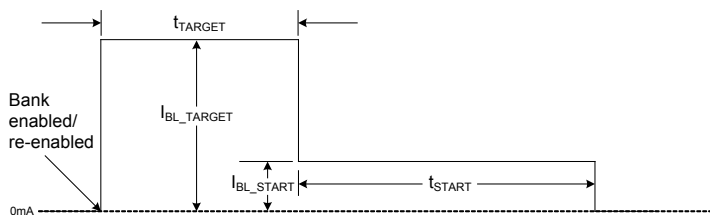
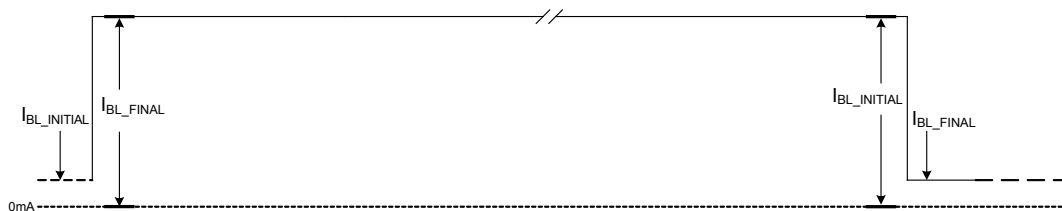


Figure 2 — State Diagram for Fade Function

Applications Information (continued)

Figure 3 — Breathe Timing Diagram

Figure 4 — Blink Timing Diagram

Figure 5 — Fade-in and Fade-out Timing Diagram

Figure 6 — Auto-Dim Partial Timing Diagram

Figure 7 — Auto-Dim Full Timing Diagram

Figure 8 — Brightness Increase and Decrease Without Fade Timing Diagram

Note: See next page for figure notes.

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Notes for figures on previous page

t_1 = start of cycle

t_2 = end of cycle

t_{START} = The time that the bank's current remains at the start value.

t_{TARGET} = The time that the bank's current remains at the target value.

$t_{BREATHE}$ = The time that the bank's current will continue to increase or decrease during a breathe cycle. Breathe time is determined by multiplying the breathe rate by the number of steps (from Table 1). Breathe rate is a group dependent value of the effect rate register 0Fh.

t_{FADE_IN} = The fade time of increasing bank current, determined by multiplying the fade rate by the number of steps (from Table 1). Fade rate is a group dependent value of the effect rate register 0Fh.

t_{FADE_OUT} = The fade time of decreasing bank current, determined by multiplying the fade rate by the number of steps (from Table 1). Fade

rate is a group dependent value of the effect rate register 0Fh. t_{FADE_IN} is always equal to t_{FADE_OUT} .

I_{BL_START} = The bank current at the start of the cycle. This is the bank dependent value of register 02h, 03h, 04h, or 05h.

I_{BL_TARGET} = The bank current at the end of the cycle. This is the bank dependent value of register 06h, 07h, 08h, or 09h.

$I_{BL_INITIAL}$ = The bank dependent value of register 02h, 03h, 04h, or 05h.

I_{BL_FINAL} = The bank dependent value of register 02h, 03h, 04h, or 05h.

NOTE: "START" and "TARGET" subscripts apply only to blink and breathe effects which require a target value to complete a cycle. "INITIAL" and "FINAL" subscripts apply when changing a bank's current without use of the target registers.



Applications Information (continued)

Table 1 — Number of Backlight Fade / Breathe Steps between Values (See Note)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|-----|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|----|
| Starting Value (mA) | 25 | 106 | 105 | 104 | 102 | 96 | 90 | 88 | 84 | 80 | 76 | 72 | 68 | 64 | 60 | 52 | 47 | 42 | 38 | 34 | 30 | 26 | 24 | 22 | 20 | 18 | 16 | 14 | 12 | 10 | 8 | 4 | 0 |
| | 23 | 102 | 101 | 100 | 98 | 92 | 86 | 84 | 80 | 76 | 72 | 68 | 64 | 60 | 56 | 48 | 43 | 38 | 34 | 30 | 26 | 22 | 20 | 18 | 16 | 14 | 12 | 10 | 8 | 6 | 4 | 0 | 4 |
| | 21 | 98 | 97 | 96 | 94 | 88 | 82 | 80 | 76 | 72 | 68 | 64 | 60 | 56 | 52 | 44 | 39 | 34 | 30 | 26 | 22 | 18 | 16 | 14 | 12 | 10 | 8 | 6 | 4 | 2 | 0 | 4 | 8 |
| | 20 | 96 | 95 | 94 | 92 | 86 | 80 | 78 | 74 | 70 | 66 | 62 | 58 | 54 | 50 | 42 | 37 | 32 | 28 | 24 | 20 | 16 | 14 | 12 | 10 | 8 | 6 | 4 | 2 | 0 | 2 | 6 | 10 |
| | 19 | 94 | 93 | 92 | 90 | 84 | 78 | 76 | 72 | 68 | 64 | 60 | 56 | 52 | 48 | 40 | 35 | 30 | 26 | 22 | 18 | 14 | 12 | 10 | 8 | 6 | 4 | 2 | 0 | 2 | 4 | 8 | 12 |
| | 18 | 92 | 91 | 90 | 88 | 82 | 76 | 74 | 70 | 66 | 62 | 58 | 54 | 50 | 46 | 38 | 33 | 28 | 24 | 20 | 16 | 12 | 10 | 8 | 6 | 4 | 2 | 0 | 2 | 4 | 6 | 10 | 14 |
| | 17 | 90 | 89 | 88 | 86 | 80 | 74 | 72 | 68 | 64 | 60 | 56 | 52 | 48 | 44 | 36 | 31 | 26 | 22 | 18 | 14 | 10 | 8 | 6 | 4 | 2 | 0 | 2 | 4 | 6 | 8 | 12 | 16 |
| | 16 | 88 | 87 | 86 | 84 | 78 | 72 | 70 | 66 | 62 | 58 | 54 | 50 | 46 | 42 | 34 | 29 | 24 | 20 | 16 | 12 | 8 | 6 | 4 | 2 | 0 | 2 | 4 | 6 | 8 | 10 | 14 | 18 |
| | 15 | 86 | 85 | 84 | 82 | 76 | 70 | 68 | 64 | 60 | 56 | 52 | 48 | 44 | 40 | 32 | 27 | 22 | 18 | 14 | 10 | 6 | 4 | 2 | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 16 | 20 |
| | 14 | 84 | 83 | 82 | 80 | 74 | 68 | 66 | 62 | 58 | 54 | 50 | 46 | 42 | 38 | 30 | 25 | 20 | 16 | 12 | 8 | 4 | 2 | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 18 | 22 |
| | 13 | 82 | 81 | 80 | 78 | 72 | 66 | 64 | 60 | 56 | 52 | 48 | 44 | 40 | 36 | 28 | 23 | 18 | 14 | 10 | 6 | 2 | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 20 | 24 |
| | 12 | 80 | 79 | 78 | 76 | 70 | 64 | 62 | 58 | 54 | 50 | 46 | 42 | 38 | 34 | 26 | 21 | 16 | 12 | 8 | 4 | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 22 | 26 |
| | 11 | 76 | 75 | 74 | 72 | 66 | 62 | 58 | 54 | 50 | 46 | 42 | 38 | 34 | 30 | 22 | 17 | 12 | 8 | 4 | 0 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 26 | 30 |
| | 10 | 72 | 71 | 70 | 68 | 62 | 58 | 54 | 50 | 46 | 42 | 38 | 34 | 30 | 26 | 18 | 13 | 8 | 4 | 0 | 4 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 30 | 34 |
| | 9 | 68 | 67 | 66 | 64 | 58 | 54 | 50 | 46 | 42 | 38 | 34 | 30 | 26 | 22 | 14 | 9 | 4 | 0 | 4 | 8 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 34 | 38 |
| | 8 | 64 | 63 | 62 | 60 | 54 | 50 | 46 | 42 | 38 | 34 | 30 | 26 | 22 | 18 | 10 | 5 | 0 | 4 | 8 | 12 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 | 38 | 42 |
| | 7 | 59 | 58 | 57 | 55 | 49 | 45 | 41 | 37 | 33 | 29 | 25 | 21 | 17 | 13 | 5 | 0 | 5 | 9 | 13 | 17 | 21 | 23 | 25 | 27 | 29 | 31 | 33 | 35 | 37 | 39 | 43 | 47 |
| | 6 | 54 | 53 | 52 | 50 | 44 | 40 | 36 | 32 | 28 | 24 | 20 | 16 | 12 | 8 | 0 | 5 | 10 | 14 | 18 | 22 | 26 | 28 | 30 | 32 | 34 | 36 | 38 | 40 | 42 | 44 | 48 | 52 |
| | 5 | 46 | 45 | 44 | 42 | 36 | 32 | 28 | 24 | 20 | 16 | 12 | 8 | 4 | 0 | 8 | 13 | 18 | 22 | 26 | 30 | 34 | 36 | 38 | 40 | 42 | 44 | 46 | 48 | 50 | 52 | 56 | 60 |
| | 4.5 | 42 | 41 | 40 | 38 | 32 | 28 | 24 | 20 | 16 | 12 | 8 | 4 | 0 | 4 | 12 | 17 | 22 | 26 | 30 | 34 | 38 | 40 | 42 | 44 | 46 | 48 | 50 | 52 | 54 | 56 | 60 | 64 |
| | 4 | 38 | 37 | 36 | 34 | 28 | 24 | 20 | 16 | 12 | 8 | 4 | 0 | 4 | 8 | 16 | 21 | 26 | 30 | 34 | 38 | 42 | 44 | 46 | 48 | 50 | 52 | 54 | 56 | 58 | 60 | 64 | 68 |
| | 3.5 | 34 | 33 | 32 | 30 | 24 | 20 | 16 | 12 | 8 | 4 | 0 | 4 | 8 | 12 | 20 | 25 | 30 | 34 | 38 | 42 | 46 | 48 | 50 | 52 | 54 | 56 | 58 | 60 | 62 | 64 | 68 | 72 |
| | 3.0 | 30 | 29 | 28 | 26 | 20 | 16 | 12 | 8 | 4 | 0 | 4 | 8 | 12 | 16 | 24 | 29 | 34 | 38 | 42 | 46 | 50 | 52 | 54 | 56 | 58 | 60 | 62 | 64 | 66 | 68 | 72 | 76 |
| | 2.5 | 26 | 25 | 24 | 22 | 16 | 12 | 8 | 4 | 0 | 4 | 8 | 12 | 16 | 20 | 28 | 33 | 38 | 42 | 46 | 50 | 54 | 56 | 58 | 60 | 62 | 64 | 66 | 68 | 70 | 72 | 76 | 80 |
| | 2.0 | 22 | 21 | 20 | 18 | 12 | 8 | 4 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 32 | 37 | 42 | 46 | 50 | 54 | 58 | 60 | 62 | 64 | 66 | 68 | 70 | 72 | 74 | 76 | 80 | 84 |
| 1.5 | 18 | 17 | 16 | 14 | 8 | 4 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 36 | 41 | 46 | 50 | 54 | 58 | 62 | 64 | 66 | 68 | 70 | 72 | 74 | 76 | 78 | 80 | 84 | 88 | |
| 1.0 | 14 | 13 | 12 | 10 | 4 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | 40 | 45 | 50 | 54 | 58 | 62 | 64 | 66 | 68 | 70 | 72 | 74 | 76 | 78 | 80 | 82 | 86 | 90 | |
| 0.5 | 10 | 9 | 8 | 6 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | 36 | 44 | 49 | 54 | 58 | 62 | 66 | 70 | 72 | 74 | 76 | 78 | 80 | 82 | 84 | 86 | 88 | 92 | 96 | |
| 0.2 | 4 | 3 | 2 | 0 | 6 | 10 | 14 | 18 | 22 | 26 | 30 | 34 | 38 | 42 | 50 | 55 | 60 | 64 | 68 | 72 | 76 | 78 | 80 | 82 | 84 | 86 | 88 | 90 | 92 | 94 | 98 | 102 | |
| 0.1 | 2 | 1 | 0 | 2 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | 36 | 40 | 44 | 52 | 57 | 62 | 66 | 70 | 74 | 78 | 80 | 82 | 84 | 86 | 88 | 90 | 92 | 94 | 96 | 100 | 104 | |
| 0.05 | 1 | 0 | 1 | 3 | 9 | 13 | 17 | 21 | 25 | 29 | 33 | 37 | 41 | 45 | 53 | 58 | 63 | 67 | 71 | 75 | 79 | 81 | 83 | 85 | 87 | 89 | 91 | 93 | 95 | 97 | 101 | 105 | |
| 0.0 | 0 | 1 | 2 | 4 | 10 | 14 | 18 | 22 | 26 | 30 | 34 | 38 | 42 | 46 | 54 | 59 | 64 | 68 | 72 | 76 | 80 | 82 | 84 | 86 | 88 | 90 | 92 | 94 | 96 | 98 | 102 | 106 | |
| | 0.0 | 0.05 | 0.1 | 0.2 | 0.5 | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 | 4.5 | 5.0 | 6.0 | 7.0 | 8.0 | 9.0 | 10.0 | 11.0 | 12.0 | 13.0 | 14.0 | 15.0 | 16.0 | 17.0 | 18.0 | 19.0 | 20.0 | 21.0 | 23.0 | 25.0 | |

Ending Value (mA)

NOTE

The fade time is determined by multiplying the number of steps by the fade rate (fade steps × fade rate = fade time).

The breathe time is determined by multiplying the number of steps by the breathe rate (breathe steps × breathe rate = breathe time).

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ongoing fade, the bank will turn off immediately. When the backlight bits are re-enabled and BxFEN = 1, the backlight currents will begin at 0mA and fade to the value determined by the backlight current register bits IBx[4:0]. If the backlight enable bits are re-enabled and BxFEN = 0, the main backlights will proceed immediately to the value of IBx[4:0]. Note that the words “target value” are not used to describe the final value after a fade operation. “Target value” is reserved for describing the backlight settings at the end of the blink or breathe effect cycles.

Non-Programmable Backlight Steps

In addition to the 32 programmable backlight steps, there are 75 non-programmable steps which are used only during a fade or breathe operation. Table 1 provides the total number of steps between the starting and ending value of any fade or breathe operation. The value from Table 1 is multiplied by the fade rate to determine the total fade time. The maximum possible fade-in duration, from 0mA to 25mA, or fade-out duration, from 25mA to 0mA, is equal to $106 \times 16\text{ms} = 1696\text{ms}$.

Figures 10 through 14 provide additional information about the non-programmable steps. Each figure represents one linear segment of the overall fade range shown in Figure 15. The overall fade range is a piece-wise linear approximation of a logarithmic function which provides for a very smooth visual fading or breathing effect.

The fade rate may be changed dynamically when a fade operation is active by writing new values to the fade register. When a new backlight level is written during an ongoing fade operation, the fade will be redirected to the new value from the present state. An ongoing fade operation may be cancelled by disabling fade, which will result in the backlight current changing immediately to the final value. If fade is disabled, the current level will change immediately to the final value without the fade delay.

PWM Operation on Bank #1

A PWM signal on the PWM pin can be used to adjust the DC current through the LEDs in bank #1. When the duty cycle is 100%, the backlight current through each LED (I_{BL}) equals the full scale current value set for bank #1. The PWM input samples voltage at the PWM pin and converts

the duty cycle to a DC current level. A DC current is passed through the LEDs, providing lower noise compared to the more conventional pulsed current PWM method.

PWM Sampling

The sampling system that translates the PWM signal to a DC current requires the PWM pin to have a minimum high time t_{HIGH_MIN} to set the DC level. High time less than t_{HIGH_MIN} impacts the accuracy of the target I_{BL} . The minimum duty cycle needed to support the minimum high time specification varies with the applied PWM frequency (see Figure 9). Note that use of a lower PWM frequency, from 200Hz to 10kHz, will support a lower minimum duty cycle and an extended backlight dimming range.

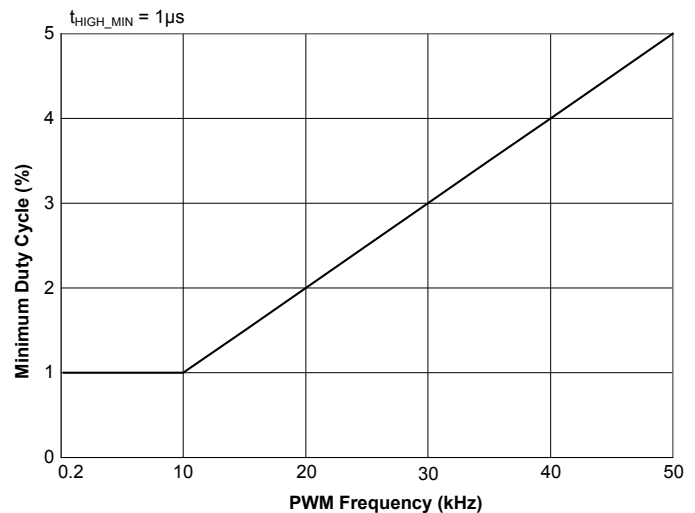


Figure 9 — Minimum Duty Cycle

Ambient Light Sense

The SC667 includes a general purpose sigma-delta ADC that is designed to interface with an ambient light sensor. The ADC input accepts the output of an external ambient light sensor circuit. When the ADC is enabled via the I²C bus, the analog signal produced by the ambient light sensor is compared with two user programmable threshold levels. The result of the comparison is then used to automatically change the brightness of the LEDs in bank #1 to a user defined value. This function is used to compensate for ambient lighting conditions — increasing brightness where brighter ambient conditions exist and decreasing brightness in lower lighting conditions.

Applications Information (continued)

NOTES: ● = Programmable backlight steps, ○ = Non-programmable fade/breathe steps

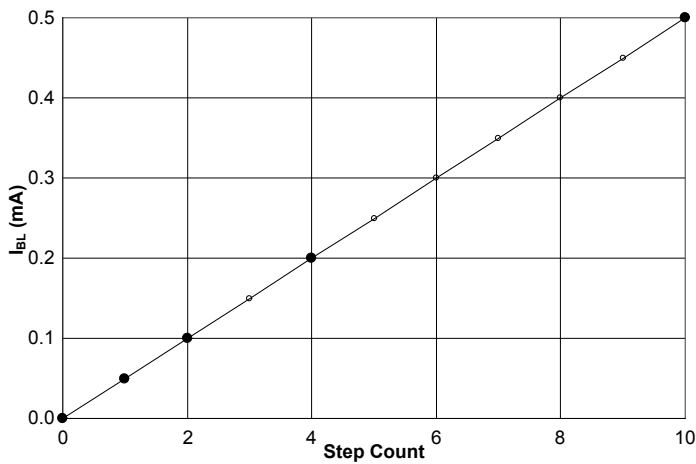


Figure 10 — Backlight Steps (0.0mA to 0.5mA)

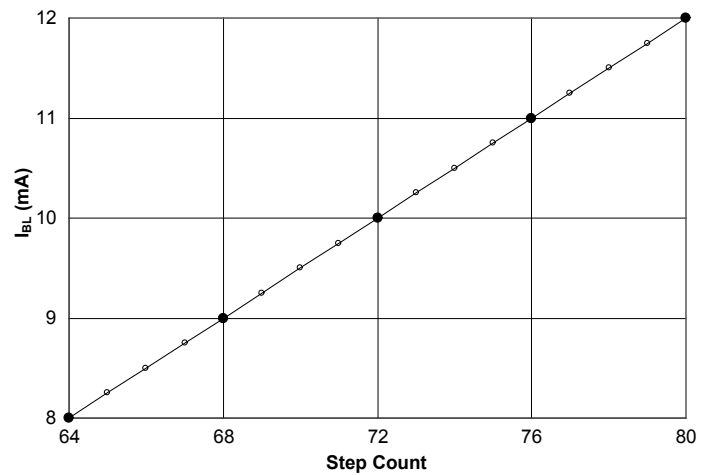


Figure 13 — Backlight Steps (8.0mA to 12.0mA)

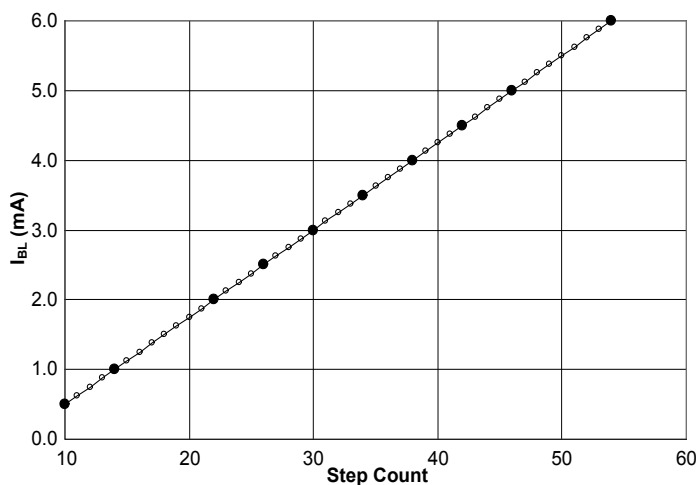


Figure 11 — Backlight Steps (0.5mA to 6.0mA)

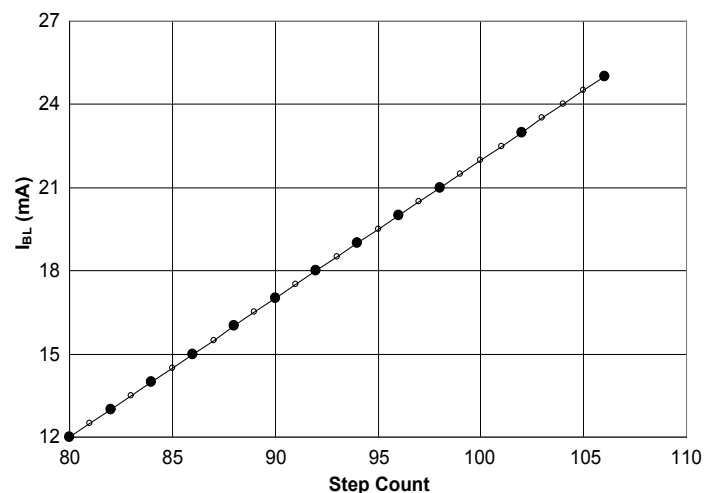


Figure 14 — Backlight Steps (12.0mA to 25.0mA)

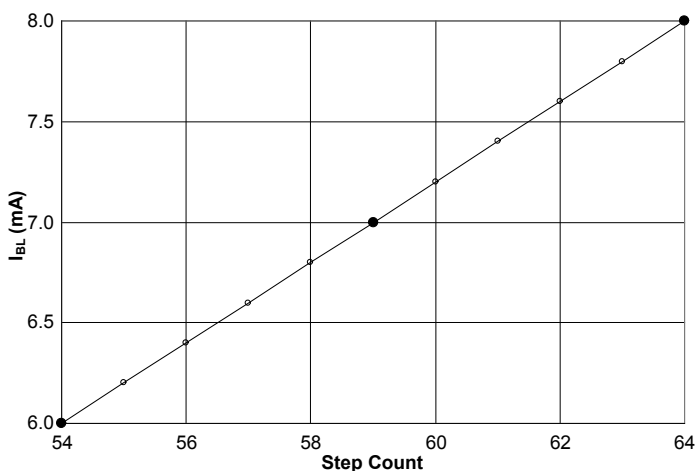


Figure 12 — Backlight Steps (6.0mA to 8.0mA)

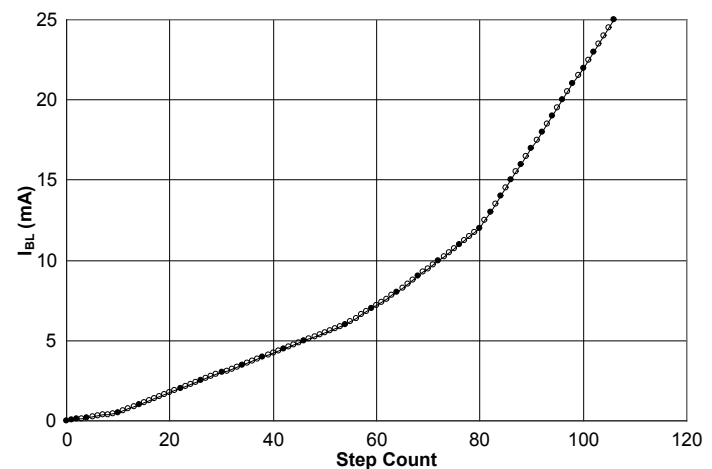


Figure 15 — Backlight Steps (0.0mA to 25.0mA)

Applications Information (continued)

General Purpose ADC

The ADI pin may also be used for general purpose ADC functions. For example, a linear temperature sensor may be added to the application circuit, and the SC667 may provide temperature data or an over-temperature warning flag. In this case, registers 13h, 14h, and 15h can be used to store the ADC reading and set thresholds that will trigger and interrupt output if the reading does not remain between them.

IRQ Output

A hardware interrupt request function is provided by the IRQ pin. This is an open-drain, active-low output that provides a flag indicating that the ALS input has exceeded a threshold level, or indicates that an overflow or underflow condition exists. Refer to Figure 16 for a description of this function.

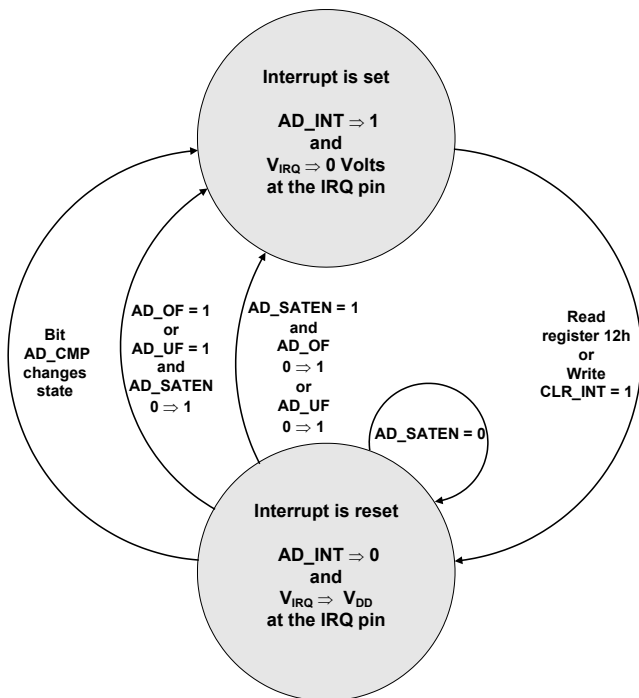


Figure 16 — IRQ Pin State Diagram

Programmable LDO Outputs

Four LDO (low dropout) regulators are included to supply power to peripheral circuits. Each LDO output voltage setting has $\pm 3.5\%$ accuracy over the line, load, and operating temperature ranges. Output current greater than specification is possible at somewhat reduced accuracy (refer to the typical characteristic section of this datasheet for load regulation examples). LDO1, LDO3, and LDO4

have identical specifications, with a programmable output ranging from 1.5V to 3.3V. LDO2 is specified to operate with programmable output ranging from 1.2V to 1.8V. All of the LDOs are low noise and can be used with noise sensitive circuits.

LDO4 is internally connected to the ADC (Analog to Digital Converter) to provide the reference voltage for the ADC. LDO4 must be enabled for the ADC to function. When the ALS function is used, LDO4 may also be used to provide power to the external ALS circuit.

Shutdown Mode

The device is disabled when the EN pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default conditions at shutdown. Typical current consumption in this mode is 0.1 μ A.

Sleep Mode

Sleep mode is activated when all backlights are off. This is a reduced current mode that helps minimize overall current consumption. In sleep mode, the I²C interface continues to monitor its input for commands from the host processor. All registers retain their settings in sleep mode. Typical current consumption in this mode is 90 μ A.

Protection Features

The SC667 provides OT (Over-temperature) protection and LDO current limiting to safeguard the device from catastrophic failures.

Over-Temperature Protection

The OT protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 30°C is provided to ensure that the device cools sufficiently before re-enabling.

LDO Current Limit

The device limits current at each LDO output pin. The typical limit is 400mA, with a minimum limit rating of 200mA. The LDOs may be used for up to 200mA without tripping the current limit.

Applications Information (continued)

Thermal Management

A junction temperature calculation should be performed for each new application design to ensure the device will not exceed 125°C during normal operation. The first step is to determine how much power can be dissipated by the SC667 in the application. The following formula approximates the maximum dissipation. This formula can be used to sum the maximum internal power dissipation required of each LDO and each backlight sink.

$$P_D = \sum_{n=1}^4 (V_{IN} - V_{LDO_n}) \times I_{LDO_n} + \sum_{m=1}^7 V_{BL_m} \times I_{BL_m}$$

The resulting power dissipation can then be used in the calculation for maximum junction temperature.

$$T_J = T_A + \Theta_{JA} \times P_D$$

where,

T_A = Maximum ambient temperature rating in °C.

Θ_{JA} = Thermal resistance, from junction to ambient, equal to 35°C/W for a optimum circuit board layout.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 17 illustrates a two-layer PCB layout for the SC667 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all bypass and decoupling capacitors — C_{IN} , C_{LDO1} , C_{LDO2} , C_{LDO3} , C_{LDO4} , and C_{BYP} as close to the device as possible.
- Ensure that all connections to pins IN and OUT make use of wide traces so that the resistive drop on each connection is minimized.
- The thermal pad should be connected to the ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.
- C_{LDO1} , C_{LDO2} , C_{LDO3} , C_{LDO4} , and C_{BYP} should be grounded together. Connect these capacitors to the ground plane at one point near the SC667 as shown in Figure 17.

- Figure 18 shows the component copper layer. Make all ground connections to a solid ground plane as shown in Figure 19.
- All LDO output traces should be made as wide as possible to minimize resistive losses.

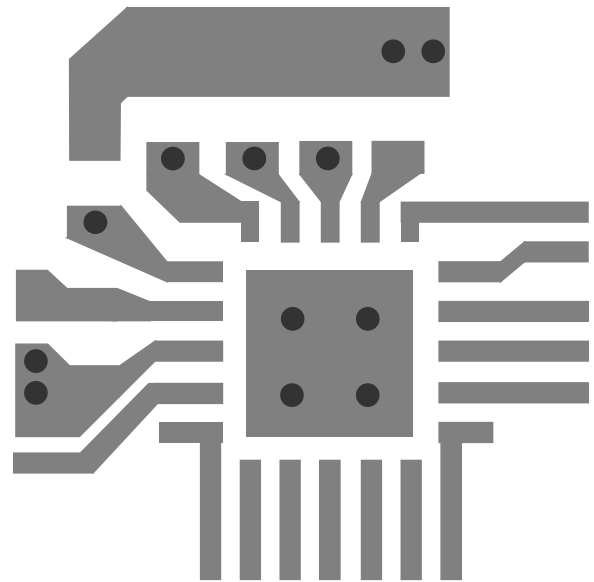


Figure 18 — Layer 1

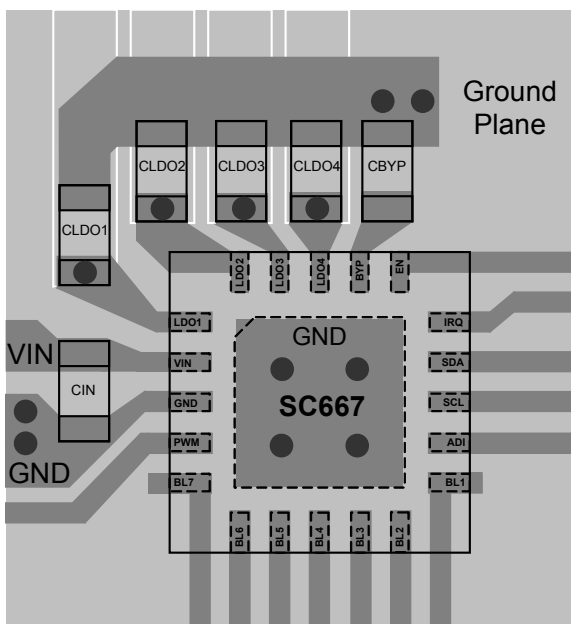


Figure 17 — Recommended PCB Layout

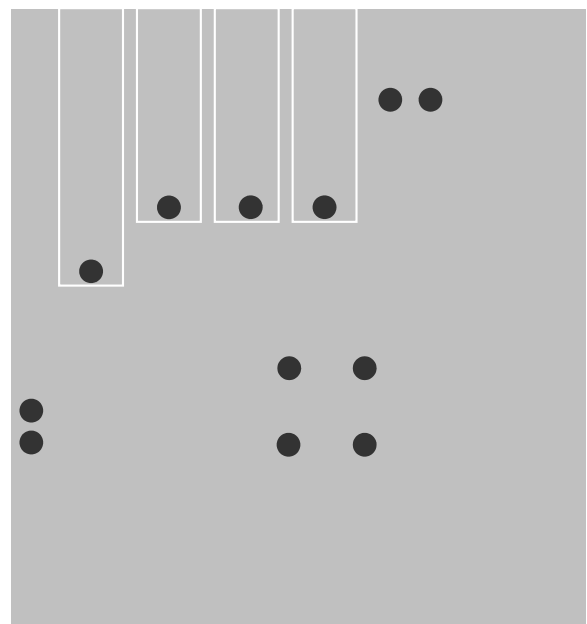


Figure 19 — Layer 2

Serial Interface

The I²C General Specification

The SC667 is a read-write slave-mode I²C device and complies with the Philips I²C standard Version 2.1, dated January 2000. The SC667 has twenty-three user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, supporting direct format for write operation. Read operations are supported on both combined format and stop separated format. While there is no auto increment/decrement capability in the SC667 I²C logic, a tight software loop can be designed to randomly access the next register independent of which register you begin accessing. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

SC667 Limitations to the I²C Specifications

The SC667 only recognizes seven bit addressing. This means that ten bit addressing and CBUS communication are not compatible. The device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s).

Slave Address Assignment

The seven bit slave address is 1110 000x. The eighth bit is the data direction bit. E0h is used for a write operation, and E1h is used for a read operation.

Supported Formats

The supported formats are described in the following subsections.

Direct Format — Write

The simplest format for an I²C write is direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC667 I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends

the appropriate 8 bit data byte. Once again, the slave acknowledges and the master terminates the transfer with the stop condition [P].

Combined Format — Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC667 I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the 8 bit data from the previously addressed register; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

Stop Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The SC667 then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the SC667 with a read command. The device acknowledges this request and returns the data from the register location that had previously been set up.