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SC68C2550B

5 V, 3.3 V and 2.5 V dual UART, 5 Mbit/s (max.), with 16-byte FIFOs and 68 mode μP interface

Rev. 03 — 9 October 2009 Product data sheet

1. General description

The SC68C2550B is a two channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s.

The SC68C2550B provides enhanced UART functions with 16-byte FIFOs, modem control interface, DMA mode data transfer. The DMA mode data transfer is controlled by the FIFO trigger levels and the $\overline{\text{TXRDYn}}$ and $\overline{\text{RXRDYn}}$ signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loopback capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC68C2550B operates at 5 V, 3.3 V and 2.5 V and the industrial temperature range, and is available in a plastic LQFP48 package.

2. Features

- 2 channel UART with 68 mode (Motorola) μP interface
- 5 V, 3.3 V and 2.5 V operation
- 5 V tolerant on input only pins[1]
- Industrial temperature range
- Up to 5 Mbit/s data rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 16-byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 16-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels
- Software selectable baud rate generator
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (DC to 5 Mbit/s)
- False start-bit detection

1. For data bus pins D7 to D0, see Table 22 “Limiting values”.

- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{CD}$)

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC68C2550BIB48	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

4. Block diagram

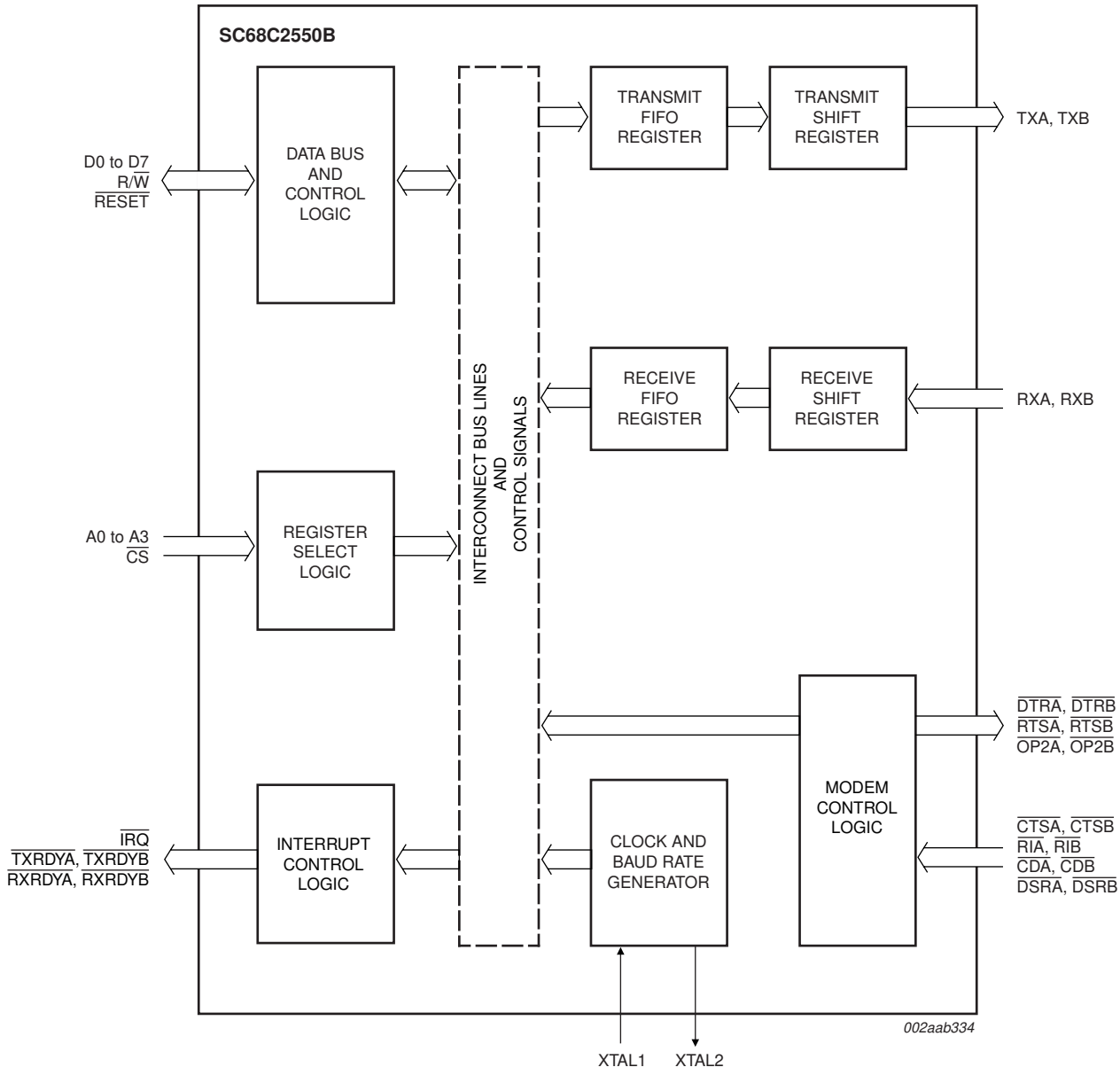

Fig 1. Block diagram of SC68C2550B

5. Pinning information

5.1 Pinning

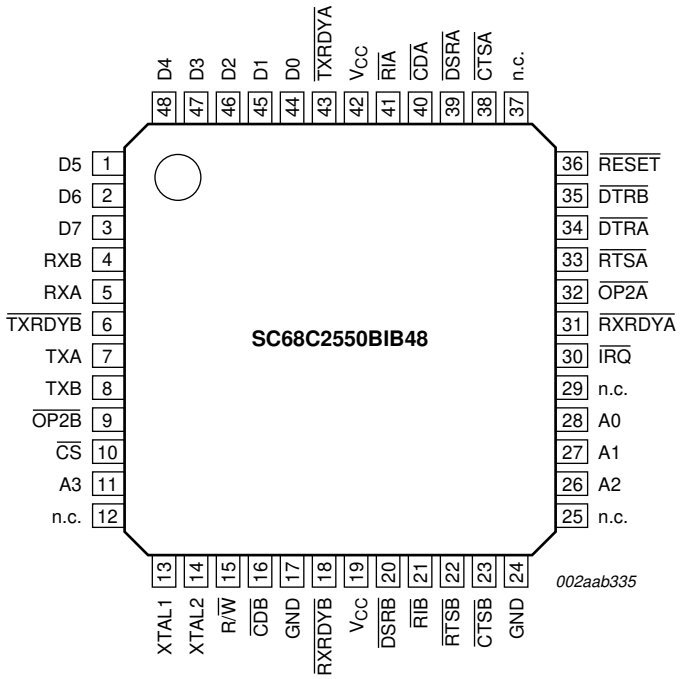

Fig 2. Pin configuration for LQFP48

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	28	I	**Address 0 select bit.** Internal register address selection.
A1	27	I	**Address 1 select bit.** Internal register address selection.
A2	26	I	**Address 2 select bit.** Internal register address selection.
A3	11	I	**Address 3.** A3 is used to select Channel A or Channel B. A logic LOW selects Channel A, and a logic HIGH selects Channel B. (See Table 3.)
$\overline{CDA}$	40	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	16	I	
$\overline{CS}$	10	I	**Chip Select (active LOW).** This pin enables data transfers between the user CPU and the SC68C2550B for the channel(s) addressed. Individual UART sections (A, B) are addressed by A3. See Table 3.
$\overline{CTSA}$	38	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{CTSn}$ pin indicates the modem or data set is ready to accept transmit data from the SC68C2550B. Status can be tested by reading MSR[4]. This pin has no effect on the UART's transmit or receive operation.
$\overline{CTSB}$	23	I	

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
D0	44	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
D1	45	I/O	
D2	46	I/O	
D3	47	I/O	
D4	48	I/O	
D5	1	I/O	
D6	2	I/O	
D7	3	I/O	
$\overline{DSRA}$	39	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
$\overline{DSRB}$	20	I	
$\overline{DTRA}$	34	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the SC68C2550B is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTRn}$ output pin to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation.
$\overline{DTRB}$	35	O	
GND	17, 24	I	**Signal and power ground.**
$\overline{IRQ}$	30	O	**Interrupt Request.** Interrupts from UART channels A-B are wire-ORed internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using $\overline{CS}$ and A3. An external pull-up resistor must be connected between this pin and V_{CC}.
$\overline{OP2A}$	32	O	**Output 2 (user-defined).** This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of MCR[3]. $\overline{OP2A}$/$\overline{OP2B}$ is a logic 0 when MCR[3] is set to a logic 1. $\overline{OP2A}$/$\overline{OP2B}$ is a logic 1 when MCR[3] is set to a logic 0. The output of these two pins is HIGH after reset.
$\overline{OP2B}$	9	O	
R/$\overline{W}$	15	I	A logic LOW on this pin will transfer the contents of the data bus (D[7:0]) from an external CPU to an internal register that is defined by address bits A[2:0]. A logic HIGH on this pin will load the contents of an internal register defined by address bits A[2:0] on the SC68C2550B data bus (D[7:0]) for access by an external CPU.
$\overline{RESET}$	36	I	**Reset (active LOW).** A logic 0 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See Section 7.10 "SC68C2550B external reset condition" for initialization details.)
$\overline{RIA}$	41	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
$\overline{RIB}$	21	I	
$\overline{RTSA}$	33	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{RTSn}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit or receive operation.
$\overline{RTSB}$	22	O	
RXA	5	I	**Receive data A, B.** These inputs are associated with individual serial channel data to the SC68C2550B receive input circuits, A-B. The RXn signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the RXn input pin is disabled and transmit data is connected to the UART receive input, internally.
RXB	4	I	

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{\text{RXRDYA}}$	31	O	**Receive Ready A, B (active LOW).** These outputs provide the receive FIFO/RHR status for individual receive channels (A-B). $\overline{\text{RXRDYn}}$ is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFOs. A logic 0 indicates there is a receive data to read/upload, that is, receive ready status with one or more receive characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{\text{RXRDYB}}$	18	O	
TXA	7	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC68C2550B. The TXn pin will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the TXn output pin is disabled and transmit data is internally connected to the UART receive input.
TXB	8	O	
$\overline{\text{TXRDYA}}$	43	O	**Transmit Ready A, B (active LOW).** These outputs provide the TX FIFO/THR status for individual transmit channels (A-B). $\overline{\text{TXRDYn}}$ is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$ buffer ready status is indicated by logic 0, that is, at lease one location is empty and available in the FIFO or THR. This pin goes to a logic 1 (DMA mode 1) when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{\text{TXRDYB}}$	6	O	
V_{CC}	19, 42	I	**Power supply input**
XTAL1	13	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates. (See Section 6.5 "Programmable baud rate generator".) See Figure 3.
XTAL2	14	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1. For extended frequency operation, this pin should be tied to V_{CC} via a 2 kΩ resistor.
n.c.	12, 25, 29, 37	-	not connected

6. Functional description

The SC68C2550B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC68C2550B represents such an integration with greatly enhanced features. The SC68C2550B is fabricated with an advanced CMOS process.

The SC68C2550B is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory. The SC68C2550B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC68C2550B by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2450 without a receive FIFO, will require unloading of the RHR in 93 microseconds (this example uses a character length of 11 bits, including start/stop bits at 115.2 kbit/s). This means the external CPU will have to service the receive FIFO less than every 100 microseconds. However, with the 16-byte FIFO in the SC68C2550B, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval, giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the four selectable receive FIFO trigger interrupt levels is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC68C2550B is capable of operation up to 5 Mbit/s with a 80 MHz clock. With a crystal or external clock input of 7.3728 MHz, the user can select data rates up to 460.8 kbit/s.

The rich feature set of the SC68C2550B is available through internal registers. Selectable receive FIFO trigger levels, selectable transmit and receive baud rates, and modem interface controls are all standard features.

6.1 UART A-B functions

The UART provides the user with the capability to bidirectionally transfer information between an external CPU, the SC68C2550B package, and an external serial device. A logic 0 on chip select pin $\overline{CS}$ and A3 (LOW or HIGH) allows the user to configure, send data, and/or receive data via UART channels A and B. Individual channel select functions are shown in Table 3.

Table 3. Channel selection using $\overline{CS}$ pin

$\overline{CS}$	A3	UART select
1	-	none
0	0	channel A
0	1	channel B

6.2 Internal registers

The SC68C2550B provides two sets of internal registers (A and B) consisting of 12 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Table 4. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. The user can set the receive trigger level via FCR[7:6], but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 5. Flow control mechanism

Selected trigger level (characters)	$\overline{IRQ}$ pin activation
1	1
4	4
8	8
14	14

6.4 Hardware/software and time-out interrupts

The interrupts are enabled by IER[3:0]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC68C2550B will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The ISR register provides the current singular highest priority interrupt only. A condition can exist where a higher priority interrupt may mask the lower priority interrupt(s). Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC68C2550B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

6.5 Programmable baud rate generator

The SC68C2550B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s. The SC68C2550B can support a standard data rate of 921.6 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent transmit/receive channel control. The programmable Baud Rate Generator (BRG) is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC68C2550B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 6).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC68C2550B divides the basic external clock by 16. The basic 16× clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 6 shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

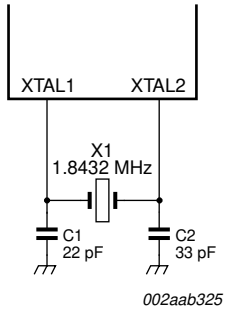

Fig 3. Crystal oscillator connection

Table 6. Baud rate generator programming table using a 1.8432 MHz clock

Output baud rate	Output 16× clock divisor (decimal)	Output 16× clock divisor (HEX)	DLM program value (HEX)	DLL program value (HEX)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
3600	32	20	00	20
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

6.6 DMA operation

The SC68C2550B FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[6:5] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC68C2550B activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the SC68C2550B sets the $\overline{\text{TXRDYn}}$ (or $\overline{\text{RXRDYn}}$) output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFOs are above the receive trigger level.

6.7 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally (see Figure 4). MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, the transmitter output pin (TXn) and the receiver input pin (RXn) are disconnected from their associated interface pins, and instead are connected together internally. The $\overline{\text{CTS}}$n, $\overline{\text{DSR}}$n, $\overline{\text{CD}}$n, and $\overline{\text{RI}}$n pins are disconnected from their normal modem control inputs pins, and instead are connected internally to MCR[1] $\overline{\text{RTS}}$, MCR[0] $\overline{\text{DTR}}$, MCR[3] ($\overline{\text{OP2}}$) and MCR[2] ($\overline{\text{OP1}}$). Loopback test data is entered into the transmit holding register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART transmit/receive circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational.

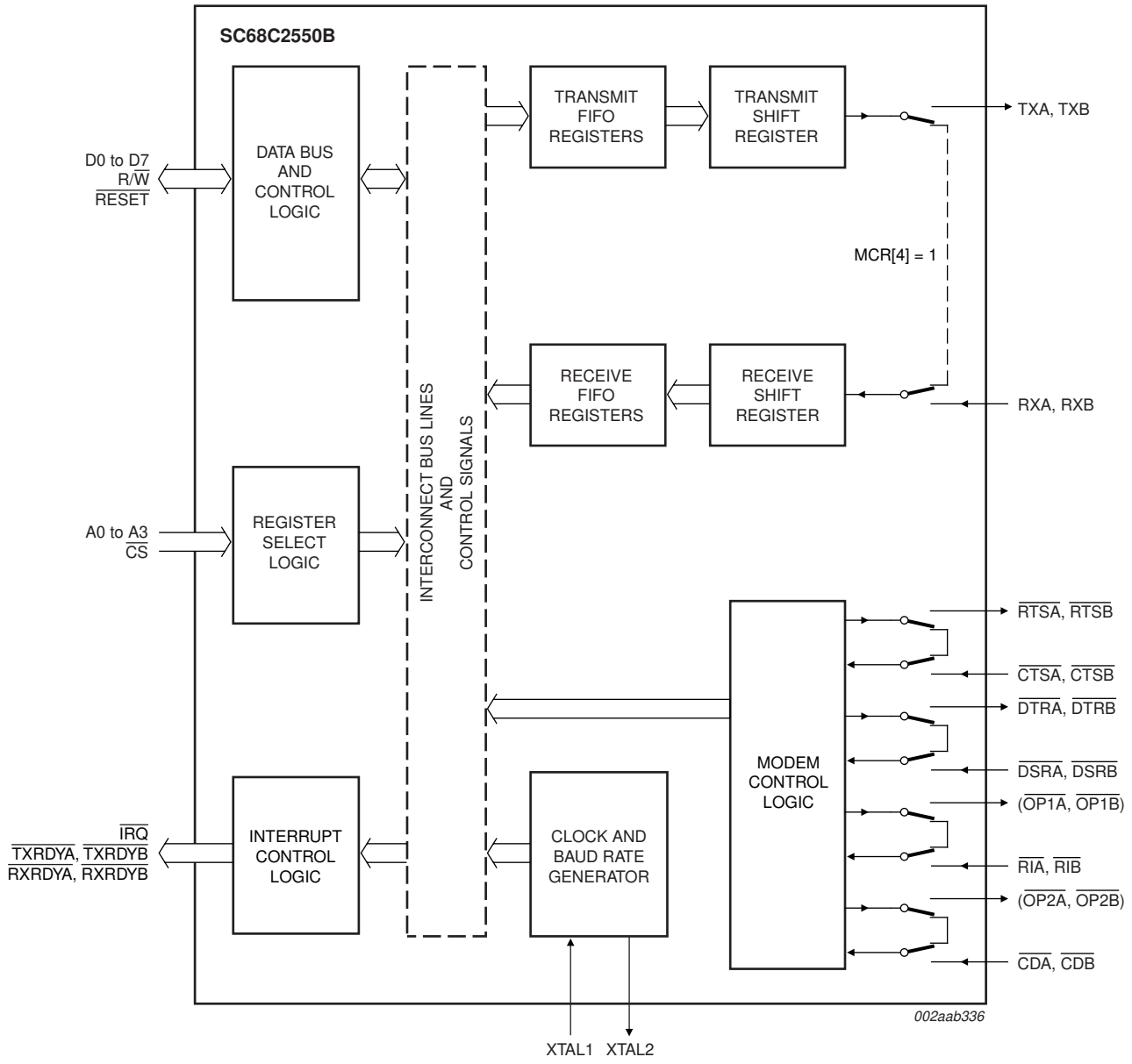

Fig 4. Internal Loopback mode diagram

7. Register descriptions

Table 7 details the assigned bit functions for the SC68C2550B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.10.

Table 7. SC68C2550B internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General register set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	reserved 0	reserved 0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	0	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	0	loop back	$\overline{OP2}$ control	($\overline{OP1}$)	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special register set[3]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown in represents the register's initialized hexadecimal value; X = n/a.

[2] Accessible only when LCR[7] is logic 0.

[3] Baud rate registers accessible only when LCR[7] is logic 1.

7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = at least one byte in FIFO/THR, logic 1 = FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC68C2550B and receive FIFO by reading the RHR register. The receive section provides a mechanism to

prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the $\overline{\text{IRQ}}$ output pin.

Table 8. Interrupt Enable Register bits description

Bit	Symbol	Description
7:4	IER[7:4]	not used
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. In the 16C450 mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register. In the 68C450 mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register, or by loading the THR with new data characters.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC68C2550B in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for transmit and/or receive data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 68C450 mode. Transmit Ready pin ($\overline{\text{TXRDYn}}$) will go to a logic 0 whenever the FIFO (THR, if FIFO is not enabled) is empty. Receive Ready pin ($\overline{\text{RXRDYn}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is empty. $\overline{\text{TXRDYn}}$ pin remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the

programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$n pin packages transitions LOW when the FIFO reaches the trigger level, and transitions HIGH when the FIFO empties.

7.3.2 FIFO mode

Table 9. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. logic 0 (or cleared) = normal default condition logic 1 = receive trigger level An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 10.
5:4	FCR[5:4]	not used; initialized to logic 0
3	FCR[3]	DMA mode select logic 0 = set DMA mode '0' logic 1 = set DMA mode '1' **Transmit operation in mode '0':** When the SC68C2550B is in the 68C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$n pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$n pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode '0':** When the SC68C2550B is in mode '0' (FCR[0] = logic 0), or in the FIFO mode (FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$n pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$n pin will go to a logic 1 when there are no more characters in the receiver. **Transmit operation in mode '1':** When the SC68C2550B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$n pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty. **Receive operation in mode '1':** When the SC68C2550B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDY}}$n pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	XMIT FIFO reset logic 0 = transmit FIFO not reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset logic 0 = receive FIFO not reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

Table 9. FIFO Control Register bits description *...continued*

Bit	Symbol	Description
0	FCR[0]	FIFOs enabled logic 0 = disable the transmit and receive FIFO (normal default condition). logic 1 = enable the transmit and receive FIFO. **This bit must be a '1' when other FCR bits are written to, or they will not be programmed.**

Table 10. RCVR trigger levels

FCR[7]	FCR[6]	Receive FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

7.4 Interrupt Status Register (ISR)

The SC68C2550B provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 11 shows the data values (bit 0 to bit 3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 11. Interrupt source

Priority level	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

Table 12. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the 68C450 mode. They are set to a logic 1 when the FIFOs are enabled in the SC68C2550B mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	not used
3:1	ISR[3:1]	INT priority bits 2 to 0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 11). logic 0 or cleared = default condition
0	ISR[0]	INT status logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 13. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor Latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = Divisor Latch disabled (normal default condition). Logic 1 = Divisor Latch enabled.
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TXn output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no break condition (normal default condition) logic 1 = forces the transmitter output (TXn) to a logic 0 for alerting the remote receiver to a line break condition
5:3	LCR[5:3]	programs the parity conditions (see Table 14)
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 15). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 16). logic 0 or cleared = default condition

Table 14. LCR[5:3] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
X	0	1	odd parity
0	1	1	even parity
0	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 15. LCR[2] stop bit length

LCR[2]	Word length	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 16. LCR[1:0] word length

LCR[1]	LCR[0]	Word length
0	0	5
0	1	6
1	0	7
1	1	8

7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 17. Modem Control Register bits description

Bit	Symbol	Description
7:5	MCR[7:5]	reserved; set to '0'
4	MCR[4]	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output (TXn) and the receiver input (RXn), $\overline{\text{CTSn}}$, $\overline{\text{DSRn}}$, $\overline{\text{CDn}}$, and $\overline{\text{RIn}}$ pins are disconnected from the SC68C2550B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 4). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3	MCR[3]	$\overline{\text{OP2}}$ control logic 0 = forces $\overline{\text{OP2n}}$ output pin to HIGH state logic 1 = forces $\overline{\text{OP2n}}$ output pin to LOW state. In Loopback mode, controls MSR[7].
2	MCR[2]	($\overline{\text{OP1}}$). $\overline{\text{OP1A}}$/$\overline{\text{OP1B}}$ are not available as an external signal in the SC68C2550B. This bit is instead used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem $\overline{\text{RIn}}$ interface signal.
1	MCR[1]	$\overline{\text{RTS}}$ logic 0 = force $\overline{\text{RTSn}}$ output pin to a logic 1 (normal default condition) logic 1 = force $\overline{\text{RTSn}}$ output pin to a logic 0
0	MCR[0]	$\overline{\text{DTR}}$ logic 0 = force $\overline{\text{DTRn}}$ output pin to a logic 1 (normal default condition) logic 1 = force $\overline{\text{DTRn}}$ output pin to a logic 0

7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC68C2550B and the CPU.

Table 18. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when there are no remaining error flags associated with the remaining data in the FIFO.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the Transmit Holding Register and the Transmit Shift Register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to '1' whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmit Shift Register. The bit is reset to a logic 0 concurrently with the loading of the Transmit Holding Register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RXn was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error logic 0 = no parity error (normal default condition) logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the Receive Shift Register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready logic 0 = no data in Receive Holding Register or FIFO (normal default condition) logic 1 = data has been received and is saved in the Receive Holding Register or FIFO

7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC68C2550B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 19. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	CD. During normal operation, this bit is the complement of the $\overline{CDn}$ input pin. Reading this bit in the Loopback mode produces the state of MCR[3] ($\overline{OP2}$).
6	MSR[6]	RI. During normal operation, this bit is the complement of the $\overline{RIn}$ input pin. Reading this bit in the Loopback mode produces the state of MCR[2] ($\overline{OP1}$).
5	MSR[5]	DSR. During normal operation, this bit is the complement of the $\overline{DSRn}$ input pin. During the Loopback mode, this bit is equivalent to the state of MCR[0].
4	MSR[4]	CTS. During normal operation, this bit is the complement of the $\overline{CTSn}$ input pin. During the Loopback mode, this bit is equivalent to the state of MCR[1].
3	MSR[3]	$\Delta\overline{CD}$ [1] logic 0 = no change of state on $\overline{CDn}$ pin (normal default condition) logic 1 = the $\overline{CDn}$ input pin to the SC68C2550B has changed state since the last time it was read. A Modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] logic 0 = no change of state on $\overline{RIn}$ pin (normal default condition) logic 1 = the $\overline{RIn}$ input pin to the SC68C2550B has changed from a logic 0 to a logic 1. A Modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] logic 0 = no change of state on $\overline{DSRn}$ pin (normal default condition) logic 1 = the $\overline{DSRn}$ input pin to the SC68C2550B has changed state since the last time it was read. A Modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no change of state on $\overline{CTSn}$ pin (normal default condition) logic 1 = the $\overline{CTSn}$ input pin to the SC68C2550B has changed state since the last time it was read. A Modem Status Interrupt will be generated.

[1] Whenever any MSR bit 0 to bit 3 is set to logic 1, a Modem Status Interrupt will be generated.

7.9 Scratchpad Register (SPR)

The SC68C2550B provides a temporary data register to store 8 bits of user information.

7.10 SC68C2550B external reset condition

Table 20. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
FCR	FCR[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
SPR	SFR[7:0] = 1
DLL	DLL[7:0] = X
DLM	DLM[7:0] = X

Table 21. Reset state for outputs

Output	Reset state
TXA, TXB	logic 1
$\overline{OP2A}$, $\overline{OP2B}$	logic 1
$\overline{RTSA}$, $\overline{RTSB}$	logic 1
$\overline{DTRA}$, $\overline{DTRB}$	logic 1
$\overline{IRQ}$	3-state condition

8. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0	GND − 0.3	V_{CC} + 0.3	V
		at any input only pin	GND − 0.3	5.3	V
T_{amb}	ambient temperature	operating	−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

9. Static characteristics

Table 23. Static characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage		−0.3	0.45	−0.3	0.6	−0.5	0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage		1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage	except X1 clock	−0.3	0.65	−0.3	0.8	−0.5	0.8	V
V_{IH}	HIGH-level input voltage	except X1 clock	1.6	-	2.0	-	2.2	-	V
V_{OL}	LOW-level output voltage	on all outputs [1]							
		I_{OL} = 5 mA (data bus)	-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)	-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (data bus)	-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)	-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −5 mA (data bus)	-	-	-	-	2.4	-	V
		I_{OH} = −1 mA (other outputs)	-	-	2.0	-	-	-	V
		I_{OH} = −800 µA (data bus)	1.85	-	-	-	-	-	V
		I_{OH} = −400 µA (other outputs)	1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current		-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current		-	±30	-	±30	-	±30	µA
I_{CC}	supply current	f = 5 MHz	-	3.5	-	4.5	-	4.5	mA
C_i	input capacitance		-	5	-	5	-	5	pF

[1] Except XTAL2, V_{OL} = 1 V typical.

10. Dynamic characteristics

Table 24. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %, unless specified otherwise.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V and 5 V		Unit
			Min	Max	Min	Max	
t_{d1}	R/$\overline{W}$ to chip select		10	-	10	-	ns
t_{d2}	read cycle delay	25 pF load	20	-	20	-	ns
t_{d3}	delay from $\overline{CS}$ to data	25 pF load	-	77	-	26	ns
t_{d4}	data disable time	25 pF load	-	15	-	15	ns
t_{d6}	write cycle delay		25	-	25	-	ns
t_{d7}	delay from write to output	25 pF load	-	100	-	33	ns
t_{d8}	delay to set interrupt from modem input	25 pF load	-	100	-	24	ns
t_{d9}	delay to reset interrupt from read	25 pF load	-	100	-	24	ns
t_{d10}	delay from stop to set interrupt		-	$1T_{RCLK}$[1]	-	$1T_{RCLK}$[1]	ns
t_{d11}	delay from read to reset interrupt	25 pF load	-	100	-	29	ns
t_{d12}	delay from start to set interrupt		-	100	-	100	ns
t_{d13}	delay from write to transmit start		$8T_{RCLK}$[1]	$24T_{RCLK}$[1]	$8T_{RCLK}$[1]	$24T_{RCLK}$[1]	ns
t_{d14}	delay from write to reset interrupt		-	100	-	70	ns
t_{d15}	delay from stop to set $\overline{RXRDY}$		-	$1T_{RCLK}$[1]	-	$1T_{RCLK}$[1]	ns
t_{d16}	delay from read to reset $\overline{RXRDY}$		-	100	-	75	ns
t_{d17}	delay from write to set $\overline{TXRDY}$		-	100	-	70	ns
t_{d18}	delay from start to reset $\overline{TXRDY}$		-	$16T_{RCLK}$[1]	-	$16T_{RCLK}$[1]	ns
t_{h2}	R/$\overline{W}$ hold time from $\overline{CS}$		10	-	10	-	ns
t_{h3}	data hold time		15	-	15	-	ns
t_{h4}	address hold time		15	-	15	-	ns
t_{WH}	pulse width HIGH		10	-	6	-	ns
t_{WL}	pulse width LOW		10	-	6	-	ns
f_{XTAL}	clock speed	[2][3]	-	48	-	80	MHz
$t_{(RESET)}$	$\overline{RESET}$ pulse width	[4]	200	-	200	-	ns
t_{su1}	address set-up time		10	-	10	-	ns
t_{su2}	data set-up time		16	-	16	-	ns
$t_{w(CS)}$	$\overline{CS}$ pulse width		77	-	30	-	ns

[1] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[2] Applies to external clock; crystal oscillator maximum = 24 MHz.

[3] $f_{XTAL} = \frac{1}{t_{w(clk)}}$

[4] Reset pulse must happen when $\overline{CS}$ is inactive.

10.1 Timing diagrams

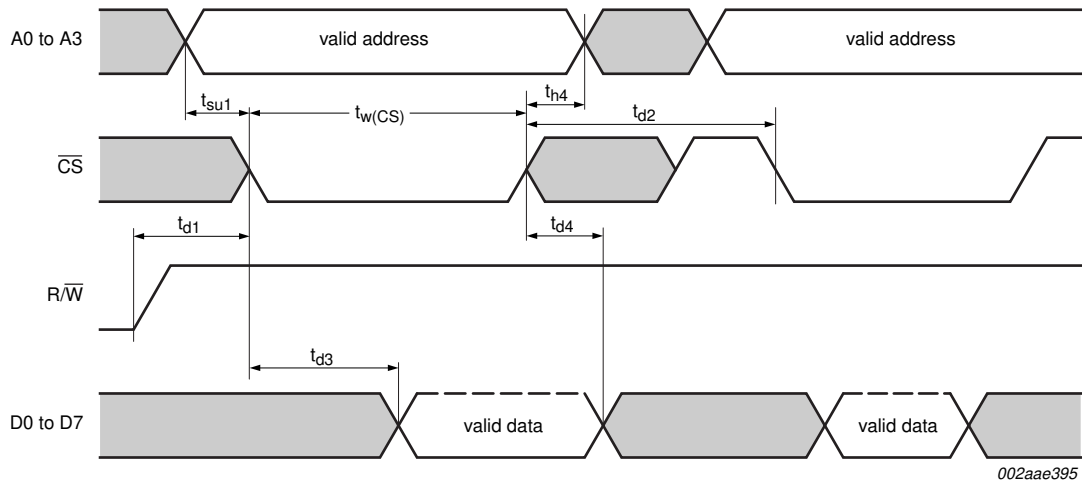

Fig 5. General read timing

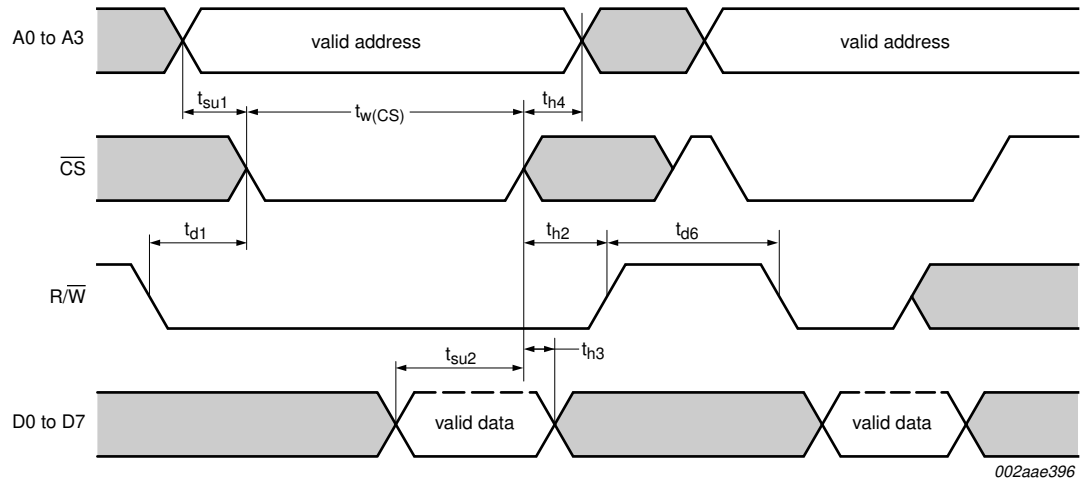

Fig 6. General write timing