Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

FAIRCHILD

SEMICONDUCTOR ™

October 1991
Revised May 2000

SCAN18373T
Transparent Latch with 3-STATE Outputs

General Description

The SCAN18373T is a high speed, low-power transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).
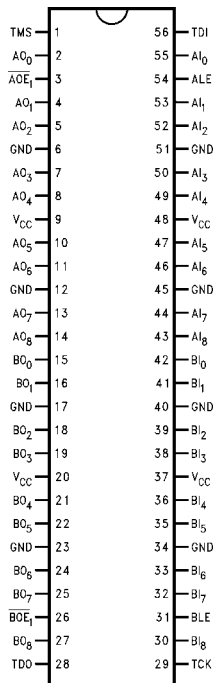
Features

■ IEEE 1149.1 (JTAG) Compliant
■ Buffered active-low latch enable
■ 3-STATE outputs for bus-oriented applications
■ 9-bit data busses for parity applications
■ Reduced-swing outputs source 32 mA/sink 64 mA
■ Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
■ TTL compatible inputs
■ 25 mil pitch SSOP (Shrink Small Outline Package)
■ Includes CLAMP and HIGHZ instructions
■ Member of Fairchild's SCAN Products

Ordering Code:

Order Number	Package Number	Package Description
SCAN1837TSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin		Pin	
TMS	1	56	TDI
AO_0	2	55	AI_0
$\overline{AOE}_1$	3	54	ALE
AO_1	4	53	AI_1
AO_2	5	52	AI_2
GND	6	51	GND
AO_3	7	50	AI_3
AO_4	8	49	AI_4
V_{CC}	9	48	V_{CC}
AO_5	10	47	AI_5
AO_6	11	46	AI_6
GND	12	45	GND
AO_7	13	44	AI_7
AO_8	14	43	AI_8
BO_0	15	42	BI_0
BO_1	16	41	BI_1
GND	17	40	GND
BO_2	18	39	BI_2
BO_3	19	38	BI_3
V_{CC}	20	37	V_{CC}
BO_4	21	36	BI_4
BO_5	22	35	BI_5
GND	23	34	GND
BO_6	24	33	BI_6
BO_7	25	32	BI_7
$\overline{BOE}_1$	26	31	BLE
BO_8	27	30	BI_8
TDO	28	29	TCK

Pin Descriptions

Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	3-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	3-STATE Latch Outputs

Truth Tables

Inputs			$AO_{(0-8)}$
ALE	$\overline{AOE}_1$	$AI_{(0-8)}$	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

| Inputs			$BO_{(0-8)}$
BLE	$\overline{BOE}_1$	$BI_{(0-8)}$	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE

Functional Description

The SCAN18373T consists of two sets of nine D-type latches with 3-STATE standard outputs. When the Latch Enable (ALE or BLE) input is HIGH, data on the inputs ($AI_{(0-8)}$ or $BI_{(0-8)}$) enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its input changes. When Latch Enable is LOW, the latches store the information that was present on the inputs a set-up time preceding the HIGH-to-LOW transition of the Latch Enable. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{AOE}_1$ or $\overline{BOE}_1$) input. When Output Enable is LOW, the standard outputs are in the 2-state mode. When Output Enable is HIGH, the standard outputs are in the high impedance mode, but this does not interfere with entering new data into the latches.
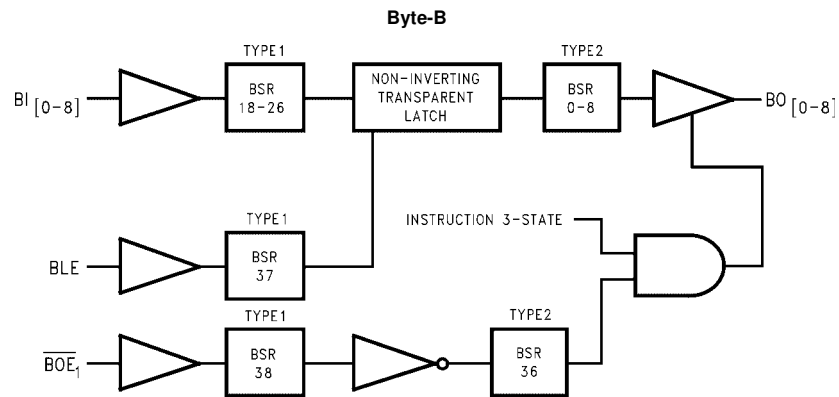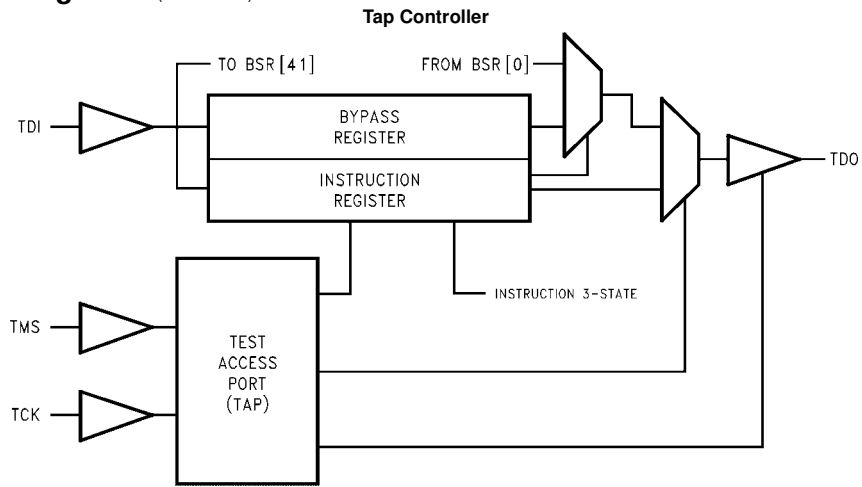
Logic Diagram
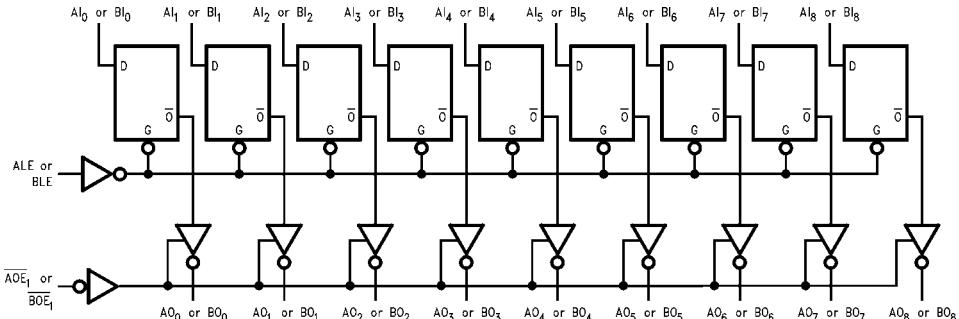
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams

Byte-A
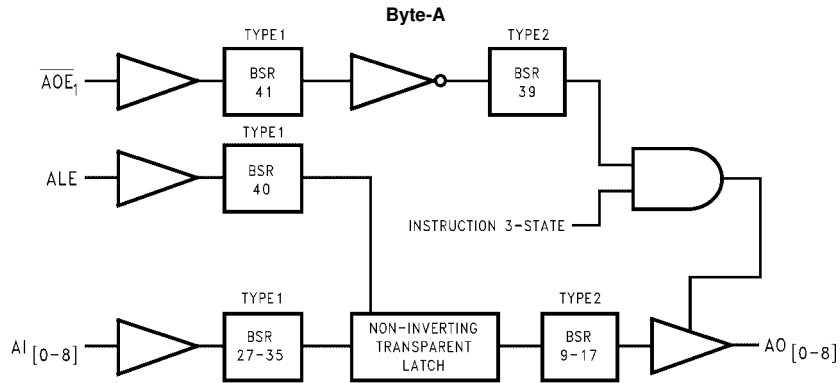
Block Diagrams (Continued)

Tap Controller

Byte-B

**Note:** BSR stands for Boundary Scan Register.

Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data.

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition Logic 0
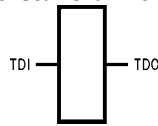
The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18373T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition
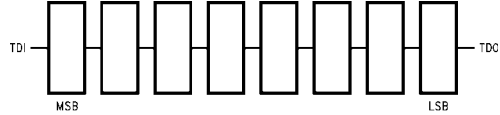
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Scan Cell TYPE1

Scan Cell TYPE2

Description of Boundary-Scan Circuitry (Continued)
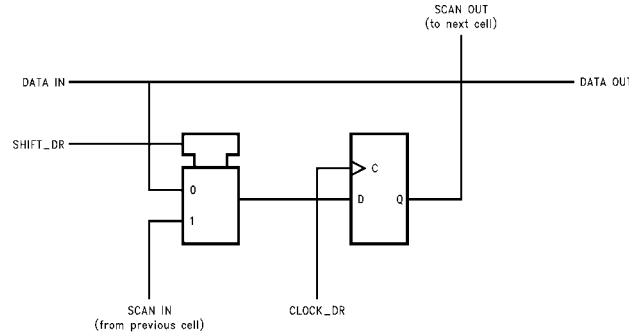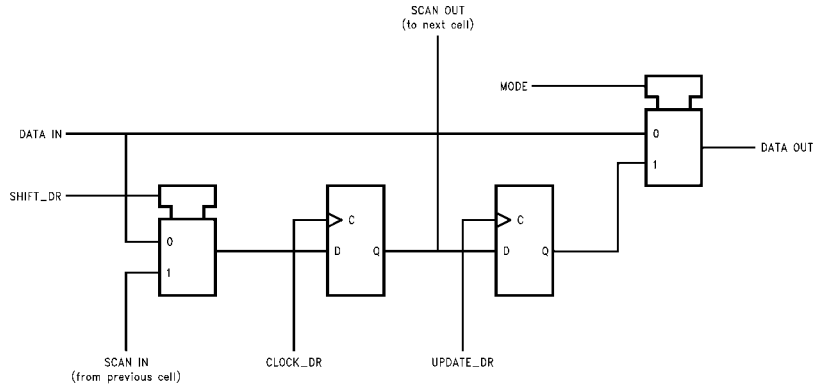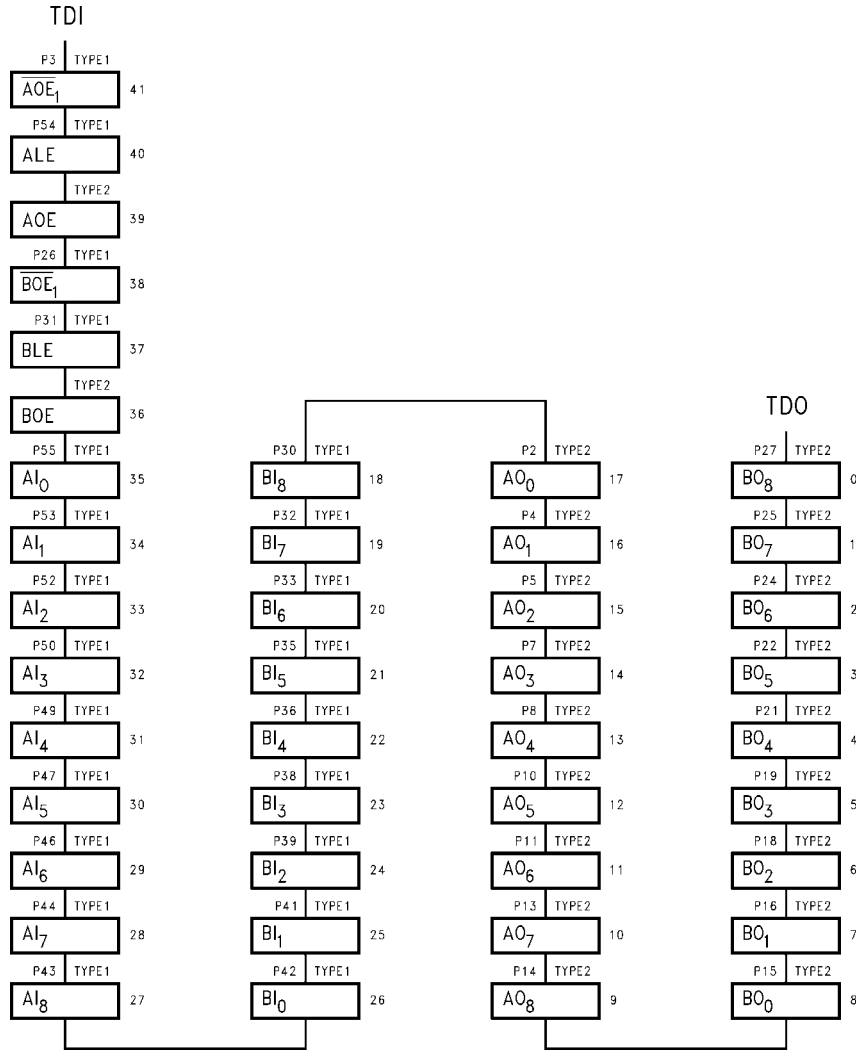
Boundary-Scan Register
Scan Chain Definition (42 Bits in Length)

TDI

| P3 | TYPE1 |
| $\overline{AOE}_1$ | 41 |

| P54 | TYPE1 |
| ALE | 40 |

| | TYPE2 |
| AOE | 39 |

| P26 | TYPE1 |
| $\overline{BOE}_1$ | 38 |

| P31 | TYPE1 |
| BLE | 37 |

| | TYPE2 |
| BOE | 36 |

TDO

| P55 | TYPE1 | | P30 | TYPE1 | | P2 | TYPE2 | | P27 | TYPE2 |
| AI_0 | 35 | | BI_8 | 18 | | AO_0 | 17 | | BO_8 | 0 |

| P53 | TYPE1 | | P32 | TYPE1 | | P4 | TYPE2 | | P25 | TYPE2 |
| AI_1 | 34 | | BI_7 | 19 | | AO_1 | 16 | | BO_7 | 1 |

| P52 | TYPE1 | | P33 | TYPE1 | | P5 | TYPE2 | | P24 | TYPE2 |
| AI_2 | 33 | | BI_6 | 20 | | AO_2 | 15 | | BO_6 | 2 |

| P50 | TYPE1 | | P35 | TYPE1 | | P7 | TYPE2 | | P22 | TYPE2 |
| AI_3 | 32 | | BI_5 | 21 | | AO_3 | 14 | | BO_5 | 3 |

| P49 | TYPE1 | | P36 | TYPE1 | | P8 | TYPE2 | | P21 | TYPE2 |
| AI_4 | 31 | | BI_4 | 22 | | AO_4 | 13 | | BO_4 | 4 |

| P47 | TYPE1 | | P38 | TYPE1 | | P10 | TYPE2 | | P19 | TYPE2 |
| AI_5 | 30 | | BI_3 | 23 | | AO_5 | 12 | | BO_3 | 5 |

| P46 | TYPE1 | | P39 | TYPE1 | | P11 | TYPE2 | | P18 | TYPE2 |
| AI_6 | 29 | | BI_2 | 24 | | AO_6 | 11 | | BO_2 | 6 |

| P44 | TYPE1 | | P41 | TYPE1 | | P13 | TYPE2 | | P16 | TYPE2 |
| AI_7 | 28 | | BI_1 | 25 | | AO_7 | 10 | | BO_1 | 7 |

| P43 | TYPE1 | | P42 | TYPE1 | | P14 | TYPE2 | | P15 | TYPE2 |
| AI_8 | 27 | | BI_0 | 26 | | AO_8 | 9 | | BO_0 | 8 |

www.fairchildsemi.com

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41 $\overline{AOE}_1$		3	Input	TYPE1	
40 ACP		54	Input	TYPE1	
39 AOE			Internal	TYPE2	Control Signals
38 $\overline{BOE}_1$		26	Input	TYPE1	
37 BCP		31	Input	TYPE1	
36 BOE			Internal	TYPE2	
35 AI_0		55	Input	TYPE1	
34 AI_1		53	Input	TYPE1	
33 AI_2		52	Input	TYPE1	
32 AI_3		50	Input	TYPE1	
31 AI_4		49	Input	TYPE1	A–in
30 AI_5		47	Input	TYPE1	
29 AI_6		46	Input	TYPE1	
28 AI_7		44	Input	TYPE1	
27 AI_8		43	Input	TYPE1	
26 BI_0		42	Input	TYPE1	
25 BI_1		41	Input	TYPE1	
24 BI_2		39	Input	TYPE1	
23 BI_3		38	Input	TYPE1	
22 BI_4		36	Input	TYPE1	B–in
21 BI_5		35	Input	TYPE1	
20 BI_6		33	Input	TYPE1	
19 BI_7		32	Input	TYPE1	
18 BI_8		30	Input	TYPE1	
17 AO_0		2	Output	TYPE2	
16 AO_1		4	Output	TYPE2	
15 AO_2		5	Output	TYPE2	
14 AO_3		7	Output	TYPE2	
13 AO_4		8	Output	TYPE2	A–out
12 AO_5		10	Output	TYPE2	
11 AO_6		11	Output	TYPE2	
10 AO_7		13	Output	TYPE2	
9 AO_8		14	Output	TYPE2	
8 BO_0		15	Output	TYPE2	
7 BO_1		16	Output	TYPE2	
6 BO_2		18	Output	TYPE2	
5 BO_3		19	Output	TYPE2	
4 BO_4		21	Output	TYPE2	B–out
3 BO_5		22	Output	TYPE2	
2 BO_6		24	Output	TYPE2	
1 BO_7		25	Output	TYPE2	
0 BO_8		27	Output	TYPE2	

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
$V_I = V_{CC}$ + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
$V_O = V_{CC}$ +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current	
Per Output Pin	±70 mA
Junction Temperature	
SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of SCAN circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C		Units	Conditions
				Guaranteed Limits			
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum HIGH	4.5		3.15	3.15	V	I_{OUT} = −50 μA
	Output Voltage	5.5		4.15	4.15		
	(Note 2)	4.5		2.4	2.4	V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		2.4	2.4		I_{OH} = −32 mA
		4.5		2.4		V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		2.4			I_{OH} = −24 mA
V_{OL}	Maximum LOW	4.5		0.1	0.1	V	I_{OUT} = 50 μA
	Output Voltage	5.5		0.1	0.1		
	(Note 2)	4.5		0.55	0.55	V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		0.55	0.55		I_{OL} = 64 mA
		4.5		0.55		V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		0.55			I_{OL} = 48 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.6	μA	$V_I = V_{CC}$
				−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	μA	V_I = GND
I_{OLD}	Minimum Dynamic	5.5		94	94	mA	V_{OLD} = 0.8V Max
I_{OHD}	Output Current (Note 3)			−40	−40	mA	V_{OHD} = 2.0V Min
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	mA Min	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	820	μA	V_O = Open TDI, TMS = GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_CC (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
I_{CCt}	Maximum I_{CC} per Input	5.5	2.0	2.0	mA	$V_I = V_{CC} − 2.1V$
		5.5	2.15	2.15	mA	$V_I = V_{CC} − 2.1V$ TDI/TMS Pin, Test One with the Other Floating

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications

Symbol	Parameter	V_CC (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units
V_{OLP}	Maximum HIGH Output Noise (Note 4)(Note 5)	5.0	1.0	1.5		V
V_{OLV}	Minimum LOW Output Noise (Note 4)(Note 5)	5.0	−0.6	−1.2		V
V_{OHP}	Maximum Overshoot (Note 5)(Note 6)	5.0	$V_{OH} + 1.0$	$V_{OH} + 1.5$		V
V_{OHV}	Minimum V_{CC} Droop (Note 5)(Note 6)	5.0	$V_{OH} − 1.0$	$V_{OH} − 1.8$		V
V_{IHD}	Minimum HIGH Dynamic Input Voltage Level (Note 6)(Note 7)	5.5	1.6	2.0	2.0	V
V_{ILD}	Maximum LOW Dynamic Input Voltage Level (Note 6)(Note 7)	5.5	1.4	0.8	0.8	V

Note 4: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched LOW and one output held LOW.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched HIGH and one output held HIGH.

Note 6: Worst case package.

Note 7: Maximum number of data inputs (n) switching. (n−1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Normal Operation

Symbol	Parameter	V_CC (V) (Note 8)	T_A= +25°C C_L = 50 pF Min	Typ	Max	T_A= −40°C to +85°C C_L = 50 pF Min	Max	Units
t_{PLH},	Propagation	5.0	2.5		9.0	2.5	9.8	ns
t_{PHL}	Delay, D to Q		2.5		9.0	2.5	9.8	
t_{PLH},	Propagation	5.0	2.5		10.0	2.5	10.5	ns
t_{PHL}	Delay, LE to Q		2.5		10.5	2.5	11.3	
t_{PLZ},	Disable Time	5.0	1.5		9.0	1.5	9.5	ns
t_{PHZ}			1.5		9.5	1.5	10.0	
t_{PZL},	Enable Time	5.0	2.0		10.9	2.0	11.9	ns
t_{PZH}			2.0		9.0	2.0	9.7	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Normal Operation

Symbol	Parameter	V_CC (V) (Note 9)	$T_A = +25°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, H or L Data to LE	5.0	3.0	3.0	ns
t_H	Hold Time, H or L LE to Data	5.0	1.5	1.5	ns
t_W	LE Pulse Width	5.0	5.0	5.0	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics

Scan Test Operation

Symbol	Parameter	V_CC (V) (Note 10)	$T_A = +25°C$ $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	14.5 14.5	ns
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	11.9 11.9	ns
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	15.8 15.8	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	19.8 19.8	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	20.2 20.2	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	21.5 21.5	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	18.2 18.2	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	20.8 20.8	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	21.5 21.5	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	20.9 20.9	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	24.2 24.2	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	25.7 25.7	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

Note: All propagation delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 11)	$T_A = +25°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, Data to TCK (Note 12)	5.0	3.0	3.0	ns
t_H	Hold Time, TCK to Data (Note 12)	5.0	4.5	4.5	ns
t_S	Setup Time, H or L $\overline{AOE}_1$, $\overline{BOE}_1$ to TCK (Note 13)	5.0	3.0	3.0	ns
t_H	Hold Time, H or L TCK to $\overline{AOE}_1$, $\overline{BOE}_1$ (Note 13)	5.0	4.5	4.5	ns
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 14)	5.0	3.0	3.0	ns
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 14)	5.0	3.0	3.0	ns
t_S	Setup Time ALE, BLE (Note 15) to TCK	5.0	3.0	3.0	ns
t_H	Hold Time TCK to ALE, BLE (Note 15)	5.0	3.5	3.5	ns
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	ns
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	ns
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	ns
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	ns
t_W	Pulse Width TCK H L	5.0	15.0 5.0	15.0 5.0	ns
f_{MAX}	Maximum TCK Clock Frequency	5.0	25	25	MHz
T_{pu}	Wait Time, Power Up to TCK	5.0	100	100	ns
T_{dn}	Power Down Delay	0.0	100	100	ms

Note 11: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 12: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 13: Timing pertains to BSR 38 and 41 only.

Note 14: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 15: Timing pertains to BSR 37 and 40 only.

Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = 25°C$ $V_{CC} = 5.0V$ $C_L = 50\ pF$ 18 Outputs Switching (Note 16)			$T_A = -40°C\ to\ +85°C$ $V_{CC} = 5.0V \pm 0.5V$ $C_L = 250\ pF$ (Note 17)		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0		12.0	4.0	13.5	ns
t_{PHL}	Latch Enable to Output	3.0		12.8	4.0	16.0	
t_{PLH}	Propagation Delay	3.0		11.5	4.0	13.0	ns
t_{PHL}	Data to Output	3.0		11.5	4.0	14.5	
t_{PZH}	Output Enable Time	2.5		10.5	(Note 18)		ns
t_{PZL}		2.5		12.5			
t_{PHZ}	Output Disable Time	2.0		10.5	(Note 19)		ns
t_{PLZ}		2.0		10.5			
t_{OSHL} (Note 20)	Pin to Pin Skew HL Data to Output		0.5	1.0		1.0	ns
t_{OSLH} (Note 20)	Pin to Pin Skew LH Data to Output		0.5	1.0		1.0	ns

Note 16: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 17: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.
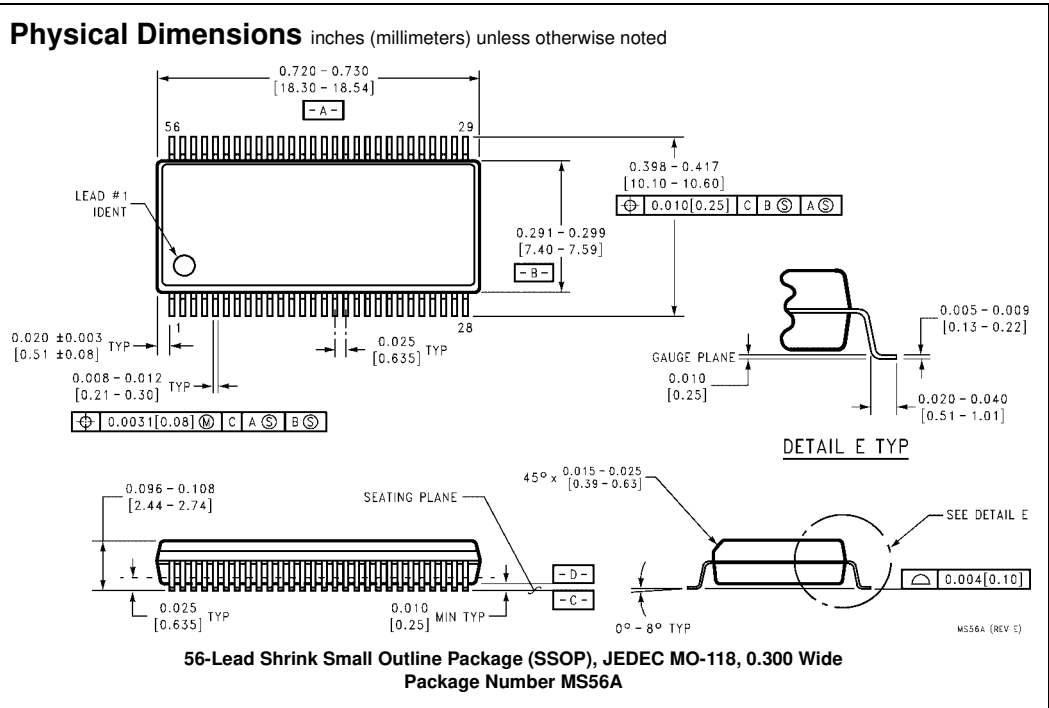
Note 18: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 19: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 20: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	13.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	34.0	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted

56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com