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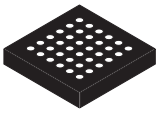
Document Number: SC900842
Rev. 2.0, 11/2010

RoHS

Buck-Boost DC/DC and LDO Power Management IC

900842

POWER MANAGEMENT



3.064 X 3.064
98ASA00004D
36-PIN WLCSP

The 900842 is comprised of a fully integrated, 4-switch synchronous Buck-Boost DC/DC regulator and a low noise, low dropout linear regulator (LDO).

The 900842 is supplied from a single Li-Ion battery cell, and steps up or down an input voltage range of 3.0 to 4.4 V to provide a fixed output voltage of 3.3 V. It provides two pins to monitor the status of the IC: a digital status signal, and an analog voltage proportional to the average output current.

The 900842 is housed in a 3x3 mm, Pb-free, wafer level chip scale package (WLCSP) with a 0.4 mm pitch.

Features

- Operates from a single Li-Ion cell 3.0 V ≤ V_{IN} ≤ 4.4 V
- Fixed 3.3 V output voltage
- Uses internal MOSFETS
- 1.625 MHz PWM switching frequency
- Seamless transition between Buck and Boost modes
- Peak current limiting and output current reporting
- Uses internal compensation
- Low-power operating mode

Applications

- Mobile internet devices
- Tablet PCs
- Netbooks

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
SCCSP900842/R2	-40 °C to 85 °C	36-PIN WLCSP

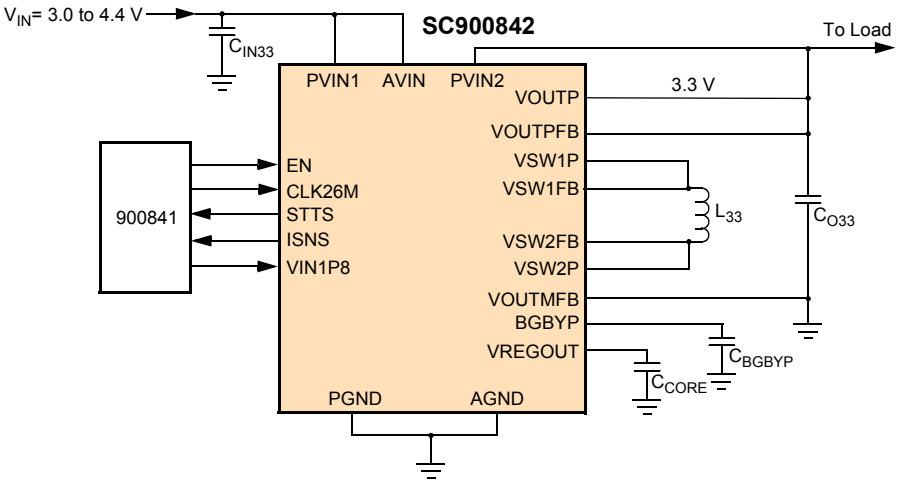


Figure 1. 900842 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

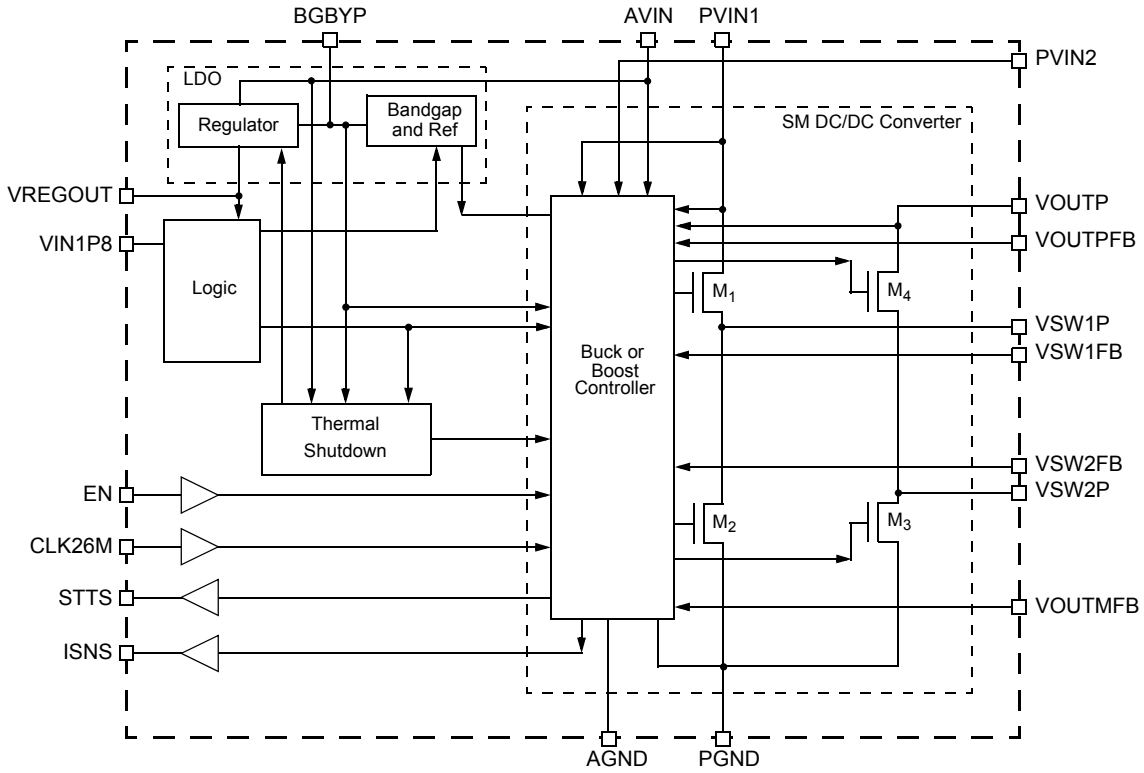
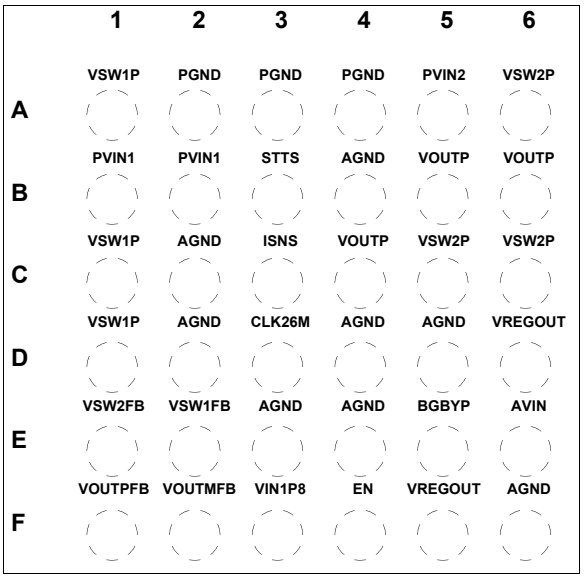
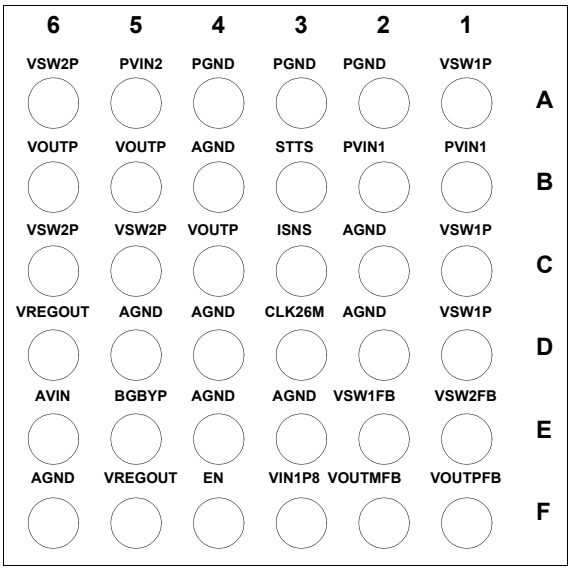


Figure 2. 900842 Internal Block Diagram

PIN CONNECTIONS



Solder Ball
Down View
(Transparent Top View)



Solder Ball
Up View
(Bottom View)

Figure 3. 900842 Pin Connections

Table 1. 900842 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Name	Type	I/O	Definition	Voltage
A1	VSW1P	Analog	O	Switching Node 1	0 - 4.7 V
A2	PGND	Ground	G	Power Ground	0 V
A3	PGND	Ground	G	Power Ground	0 V
A4	PGND	Ground	G	Power Ground	0 V
A5	PVIN2	Supply	P	Power VIN	2.8 - 4.7 V
A6	VSW2P	Analog	O	Switching Node 2	0 - 4.7 V
B1	PVIN1	Supply	P	Power VIN	2.8 - 4.7 V
B2	PVIN1	Supply	P	Power VIN	2.8 - 4.7 V
B3	STTS	Digital	O	Power Good Signal - Active Low	1.8 V
B4	AGND	Ground	G	Analog Ground	0 V
B5	VOUTP	Analog	O	Output Voltage	3.3 V
B6	VOUTP	Analog	O	Output Voltage	3.3 V
C1	VSW1P	Analog	O	Switching Node 1	0 - 4.7 V
C2	AGND	Ground	G	Analog Ground	0 V
C3	ISNS	Analog	O	Current Sense Signal	0 - 4.7 V
C4	VOUTP	Analog	O	Output Voltage	3.3 V
C5	VSW2P	Analog	O	Switching Node 2	0 - 4.7 V

Table 1. 900842 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Name	Type	I/O	Definition	Voltage
C6	VSW2P	Analog	O	Switching Node 2	0 - 4.7 V
D1	VSW1P	Analog	O	Switching Node 1	0 - 4.7 V
D2	AGND	Ground	G	Analog Ground	0 V
D3	CLK26M	Digital	I	26 MHz Clock input	1.8 V
D4	AGND	Ground	G	Analog Ground	0 V
D5	AGND	Ground	G	Analog Ground	0 V
D6	VREGOUT	Analog	O	LDO Output	2.775 V
E1	VSW2FB	Analog	I	Switching Node 2 Feedback	0 - 4.7 V
E2	VSW1FB	Analog	I	Switching Node 1 Feedback	0 - 4.7 V
E3	AGND	Ground	G	Analog Ground	0 V
E4	AGND	Ground	G	Analog Ground	0 V
E5	BGBYP	Analog	O	Reference Bypass Cap	1.2 V
E6	AVIN	Supply	P	Analog VIN	2.8 - 4.7 V
F1	VOUTPFB	Analog	I	Output Voltage Differential Feedback, Positive	3.3 V
F2	VOUTMFB	Analog	I	Output Voltage Differential Feedback, Reference	0 V
F3	VIN1P8	Supply	P	1.8 V Supply	1.8 V
F4	EN	Digital	I	Enable Signal	1.2 V / 1.8 V
F5	VREGOUT	Analog	O	LDO Output	2.775 V
F6	AGND	Ground	G	Analog Ground	0 V

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Pin / Parameter	Min	Max	Unit
Maximum Voltage			V
PVIN1, PVIN2, VSW1P, VSW2P, VOUTP, VSW1FB, and VSW2FB	-0.3	+7.5	
AVIN, VOUTPFB, STTS, ISNS	-0.3	+5.5	
VREGOUT	-0.3	+3.1	
BGBYP, EN, VIN1P8, and CLK26M	-0.3	+2.5	
All other pins	-0.3	+2.5	
ESD Voltage, All Pins[1]			
Human Body Model	-2	+2	kV
Machine Model	-200	+200	V
Charge Device Model	-500	+500	V

THERMAL RATINGS

Ambient Operating Temperature	-40	+85	°C
Operating Junction Temperature	-40	+150	°C
Storage Temperature	-65	+150	°C
Peak Package Reflow Temperature[2],[3]		+260	°C
Maximum Power Dissipation (T_A = 25 °C), P_D[4]		940	mW

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance			
Junction to Ambient (Single Layer Board)	$R_{\Theta JA(1)}$	144	°C/W
Junction to Ambient (Four Layer Board)	$R_{\Theta JA(4)}$	69	°C/W
Junction to Board	$R_{\Theta JB}$	27	°C/W

Notes:

1. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), the Machine Model (MM) (CZAP = 200 pF, RZAP = 0 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C for Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL).
4. For T_J=150 °C, T_A =85 °C and $R_{\Theta JA}$=69 °C/W, application with a 4-layer board.

ELECTRICAL CHARACTERISTICS

Table 3. System Electrical Characteristics

T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are characterized at VPWR = 3.6 V and 25°C

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL					
Typical Input Voltage Range	V_{IN}	3.0	3.6	4.4	V
Extended Input Voltage Range[5]	V_{IN}	2.8	3.6	4.7	V
Leakage Current EN=0	I_{LEAK}	- -	10 -	- -	µA
Bandgap Voltage[6]	V_{BGBYP}	-	1.2	-	V
BUCK/BOOST CONVERTER					
Output Voltage	V_{33}	-	3.3	-	V
Output Voltage Accuracy		-4.0	-	5.0	%
Continuous Output Load Current[7]	I_{33}	0	0.7	1.4	A
Short Circuit Output Current Limit[8] PVIN1 = 3.6 V	I_{LIM33}	- -	1.5 -	- -	A
Transient Load Change[9]	ΔI_{33}	-	-	0.5	A
Soft Start Time EN=1.8 V to STTS=0	t_{SS33}	- -	- -	- 700	µs
Turn Off Time EN=0 to STTS=1	t_{33OFF}	- -	- -	- 1.0	ms
Switching Frequency	f_{SW}	-	1.625	-	MHz
EN Input Voltage - Normal Mode			1.8		V
EN Input Voltage - Low Power Mode			1.2		V
LINEAR REGULATOR					
Output Voltage	V_{REGOUT}	-	2.775	-	V
Output Voltage Accuracy	V_{REGOUT}	-5.0	-	5.0	%
Load Current	I_L	0	-	100	mA
Maximum Short-circuit Output Current V_{IN}>V_{IN-MIN}, Short-circuit V_{REGOUT}	I_{LSC}	- 100	- -	- 200	mA
Load Regulation 1.0 mA < I_L < 100 mA		- -1.0	- -	- 0.5	mV/mA
Line Regulation 3.0 V < V_{IN}< 4.4 V		- -25	- -	- 25	mV

Notes

5. The IC will operate below 3.0 V, but will not meet the specifications.
6. No external DC loading is allowed at the BGBYP pin.
7. The maximum output current of 1.4 A is specified for V_{IN}=3.6 V, with the IC operating in Buck mode.
8. The IC has an input peak current limit in which M1 is the current sense device (Figure 2). This maximum current is different than the output current if the IC is in Boost mode
9. The maximum speed of change of a transient load should be 0.1 A/µs

Table 3. System Electrical Characteristics (continued)

T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are characterized at VPWR = 3.6 V and 25°C

Parameter	Symbol	Min	Typ	Max	Unit
EXTERNAL COMPONENTS					
Output Inductor	L_{33}	-	1.0	-	µH
Output Inductor DCR	L_{33DCR}	-	-	55	mΩ
Output Capacitor - Ceramic	C_{O33}	-	22		µF
Input Capacitor - Ceramic	C_{IN33}	-	10		µF
Internal Regulator Capacitor - Ceramic	C_{CORE}	-	1.0		µF
Bandgap Bypass Capacitor - Ceramic	C_{BGBYP}	-	0.1		µF

ELECTRICAL PERFORMANCE CURVES

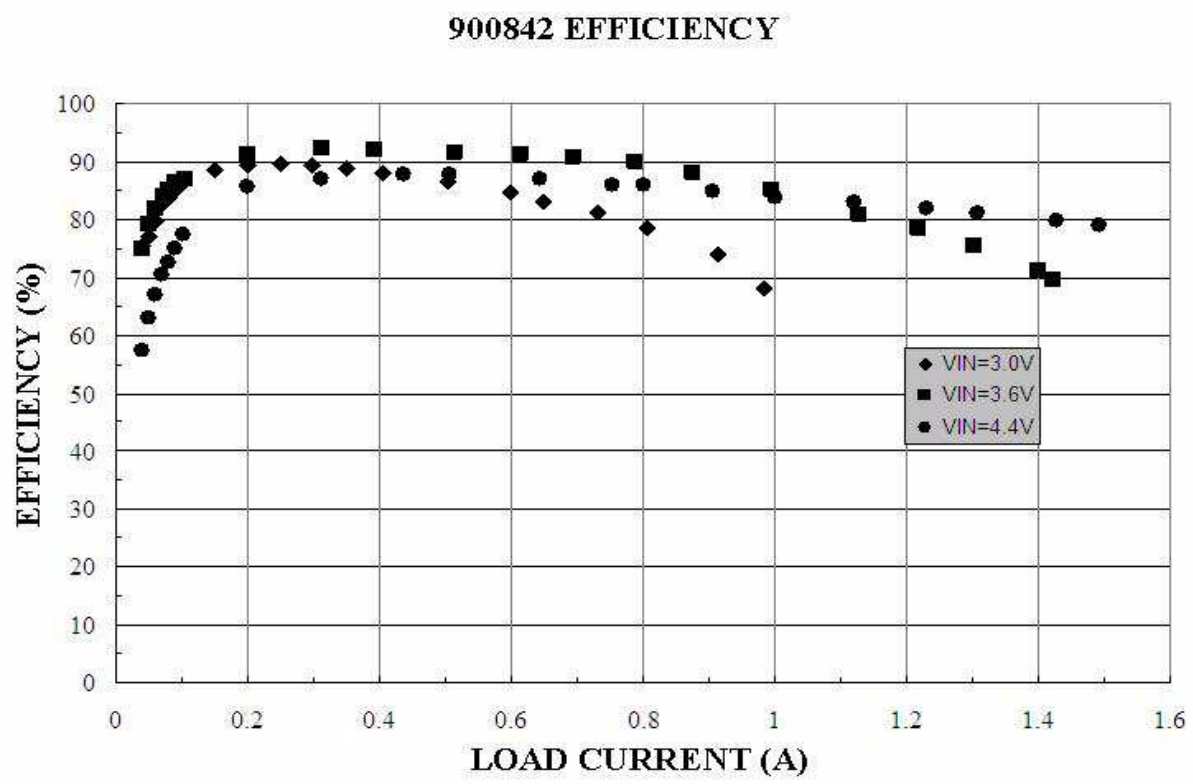


Figure 4. Switcher Efficiency vs. Output Current

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 900842 consists of an integrated switched-mode synchronous Buck-Boost DC/DC converter and its control circuit, a linear regulator, and a bandgap voltage reference.

The 900842 is supplied from a single Lithium-Ion battery cell, and steps down or up an input voltage range of 2.8 - 4.7 V, to a fixed output voltage of 3.3 V. A high switching frequency of 1.625 MHz enables the use of small passive filter components, and improves the dynamic response of the converter.

BUCK/BOOST CONVERTER

The integrated Buck-Boost converter is used to generate the fixed output voltage of 3.3 V. The IC operates in Buck mode when V_{IN} is greater that 3.3 V and in Boost mode otherwise.

When in Buck mode, M1 is used as a high side FET, M2 is used as a low side synchronous rectifier FET, M4 is on, and M3 is open (Figure 2). When in Boost mode, M1 is on, M2 is open, M3 is the switching FET, and M4 is the synchronous rectifier FET.

The IC transitions seamlessly between Buck and Boost mode following the variation in the input voltage, V_{IN}. The Buck-Boost converter is compensated internally.

There are 2 output pins that can be used to monitor the status of the IC:

STTS - Status output pin, active low.

STTS = 0 if the output voltage V_{OUTP} is up

STTS =1 if the IC is under thermal shutdown, IC is in current limit, or V_{OUTP} is too low.

ISNS - Current sense pin

The ISNS pin voltage is proportional to the average output current. When PVIN = 3.6 V, a typical ratio is 2.084 V/A.

Current Limiting

A peak current limit circuit protects the converter during overload conditions. If the current through the PMOS power switch M1 exceeds the I_{LIM33} value, M1 will turn off and the converter will skip the next cycle. This forces the inductor current to be reduced to a safe value. The PMOS power switch M1 is turned on again and the cycle is repeated until the load current is reduced.

Low Power Mode

A Low Power Mode is provided in the IC to minimize system power dissipation at low loads. In Low Power Mode, the IC operates as an LDO, with a quiescent current of 1mA.

To enter Low Power Mode, a voltage of 1.2 V must be applied to the EN pin. The Low Power Mode can only be entered after the Buck-Boost has started up in Normal Operation (EN = 1.8 V).

LOW DROPOUT LINEAR REGULATOR

The low dropout (LDO) linear regulator uses the bandgap as a reference and provides a low noise supply. The nominal regulator output voltage, V_{REGOUT}, is 2.775 V and is designed for a steady state maximum current of 100 mA. The V_{REGOUT} voltage will decrease when the load demands currents exceeding the current limit.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY INPUT VOLTAGE (PVIN1)

This is the input voltage for the Buck-Boost DC/DC converter. Input decoupling/filtering is required for proper operation.

POWER GROUND (PGND)

Power Ground connection.

OUTPUT VOLTAGE (VOUTP)

This is the 3.3 V output node.

SWITCHING NODE 1 (VSW1P)

This output pin is the switching node when the device operates in Buck mode. The inductor is connected between this pin and the VSW2P pin.

SWITCHING NODE 2 (VSW2P)

This output pin is the switching node when the device operates in Boost mode. The inductor is connected between this pin and the VSW1P pin.

SWITCHING NODE 1 FEEDBACK (VSW1FB)

Feedback voltage from Switching Node 1. This pin must be directly connected to the inductor terminal.

SWITCHING NODE 2 FEEDBACK (VSW2FB)

Feedback voltage from Switching Node 2. This pin must be directly connected to the inductor terminal.

OUTPUT VOLTAGE POSITIVE FEEDBACK (VOUTPFB)

This input must be connected to the positive end of the output capacitor.

OUTPUT VOLTAGE NEGATIVE FEEDBACK (VOUTMFB)

This input must be connected to the negative end (ground) of the output capacitor.

ANALOG SUPPLY INPUT VOLTAGE (AVIN)

Supply voltage for the Buck-or-Boost Controller and LDO regulator.

ANALOG GROUND (AGND)

Analog ground of the IC.

BOOST GATE DRIVE SUPPLY (PVIN2)

This pin is connected to the output pin, VOUTP.

LDO REGULATED OUTPUT (VREGOUT)

2.775 V LDO regulated output voltage.

REFERENCE BYPASS CAPACITOR (BGBYP)

Connect a 0.1 μF decoupling filter capacitor between this pin and GND.

1.8 V SUPPLY INPUT VOLTAGE (VIN1P8)

1.8 V supply for digital sub-circuits.

26 MHz CLOCK INPUT (CLK26M)

A 26 MHz clock input reference signal.

ENABLE (EN)

Active high enable input signal to turn on the 3.3 V output.

- EN = 1.8 V to enter Normal Operation Mode.
- EN = 1.2 V to enter Low Power Mode.

The Low Power Mode can only be entered after the Buck-Boost has started up in Normal Operation.

POWER GOOD STATUS SIGNAL (STTS)

This is an active low output signal that indicates the status of the output voltage. This signal will be high if the IC is under thermal shutdown, IC is in current limit, or V_{OUTP} is too low.

CURRENT SENSE SIGNAL (ISNS)

This output pin provides an analog voltage proportional to the average output current.

TYPICAL APPLICATIONS

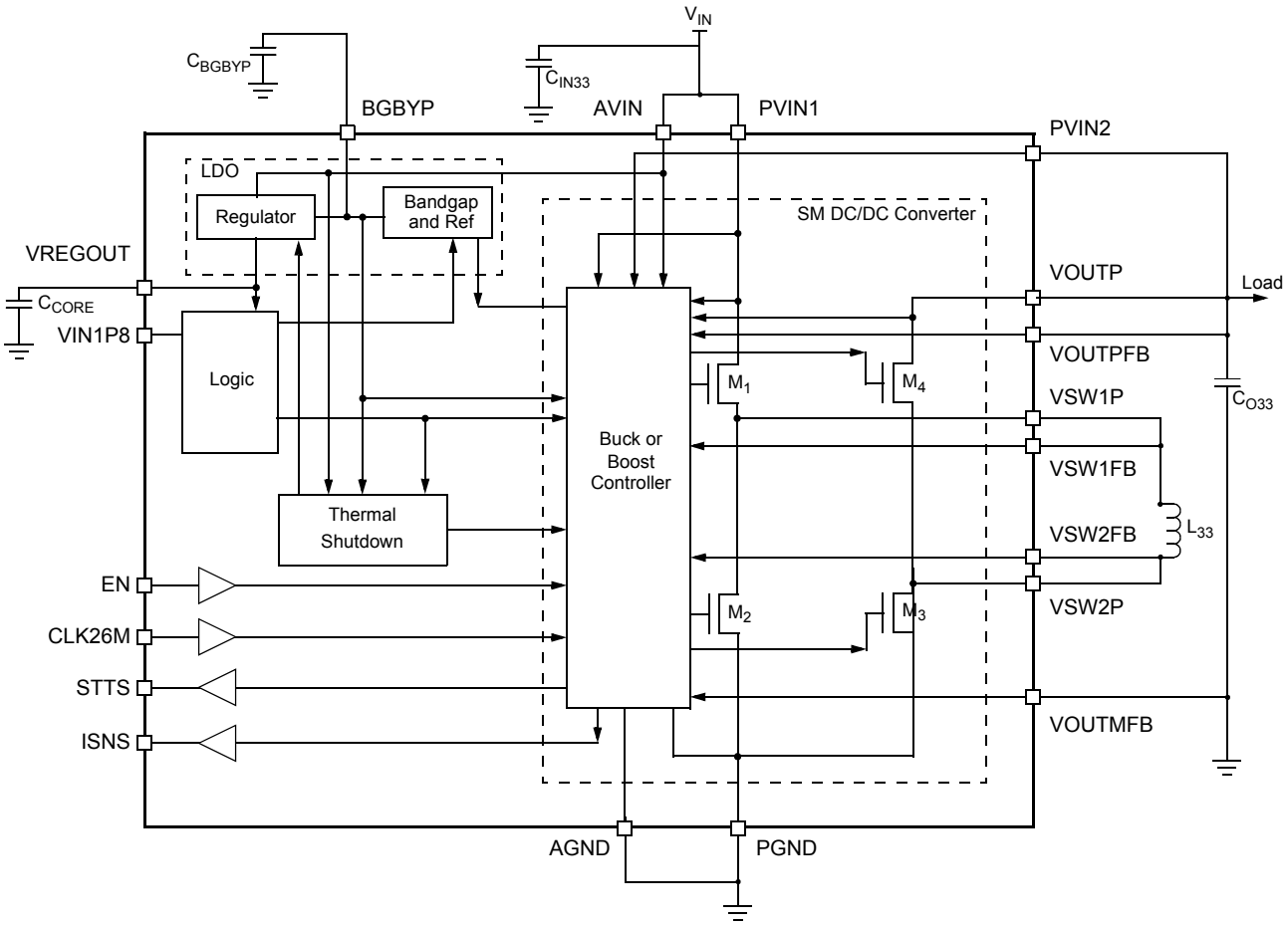


Figure 5. 900842 Typical Applications

TYPICAL CIRCUIT

Figure 5, 900842 Typical Applications, shows the schematic for a typical application. A 1-µH inductor with saturation current rating over 2.5 A is recommended for the SM DC/DC converter. The inductor series DC resistance (DCR) should be less than 55 mohm to achieve good efficiency and a low drop-out voltage. If a smaller inductance is used, the 900842 may become unstable under line and load transients and the transient response time may be affected. The 900842 is designed for ceramic capacitor in its input and output filters. The input filter capacitor, CIN33, reduces the voltage ripple on VIN, by providing the AC current drawn to the M1 switch during the first part of each switching cycle. A 10 µF ceramic capacitor should be used for CIN33 as close as possible to the PVIN1 and PGND pins of the IC. The triangular AC component of the inductor current passes through the output filter capacitor, CO33, which reduces the output voltage ripple and maintains a constant output voltage during load and line transients. A 22 µF ceramic capacitor should be used for CO33 as close as possible to the VOUTP and PGND pins. A 100 nF ceramic capacitor should be used for CBGBYP as close as possible to the BGBYP and AGND pins. A 1.0 µF ceramic capacitor should be used for CCORE as close as possible to the VREGOUT and AGND pins. Ceramic capacitor types such as X5R and X7R are recommended.

PACKAGING

PACKAGE DIMENSIONS

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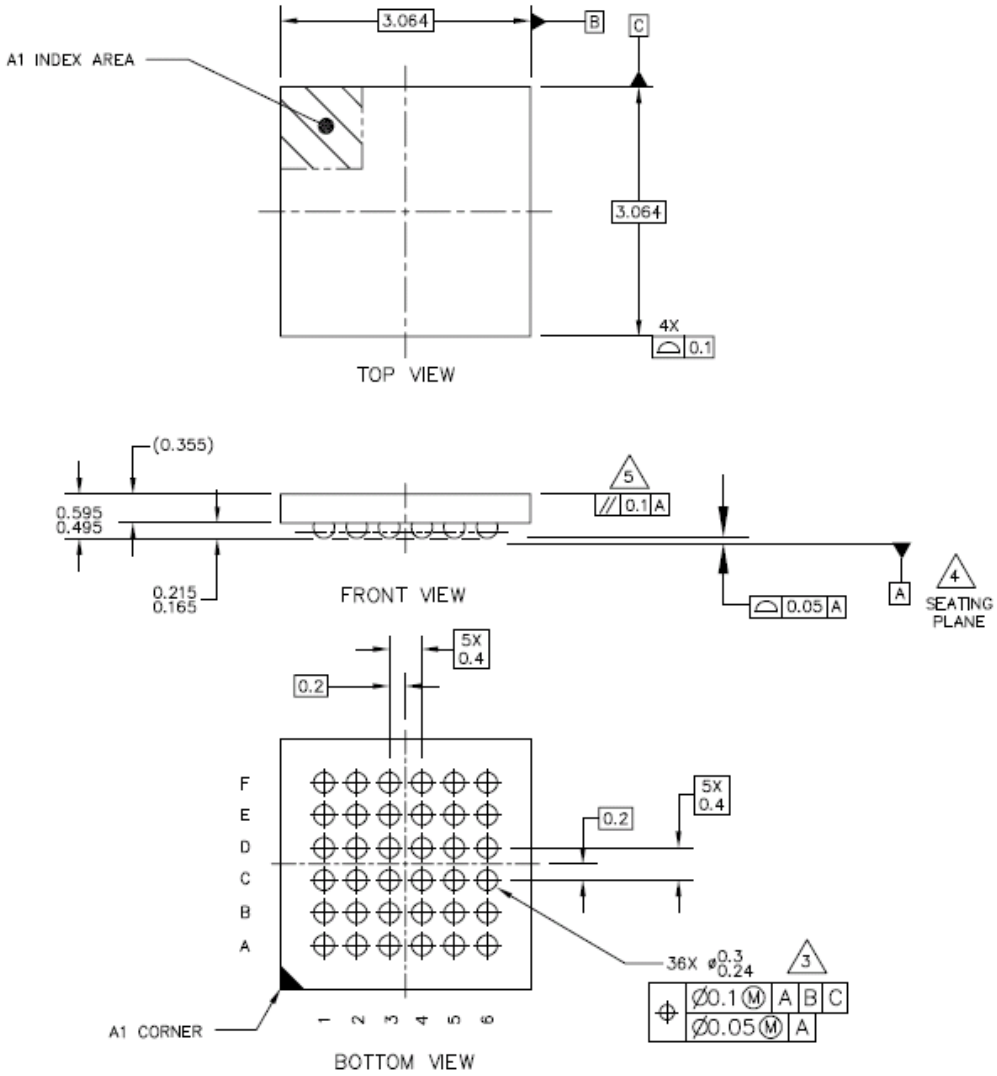

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36-PIN
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900842

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	CASE NUMBER: 2047–01	10 NOV 2008	
	STANDARD: NON–JEDEC		

36-PIN
98ASA00004D
REVISION 0

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	3/2010	• Initial Release
2.0	11/2010	• Corrected format and typos • Removed Bill of Materials and Board Layout sections

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