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SCG4500 Series Synchronous Clock Generators

PLL

CONNOR WINFIELD

2111 Comprehensive Drive

Aurora, Illinois 60505

Phone: 630-851-4722

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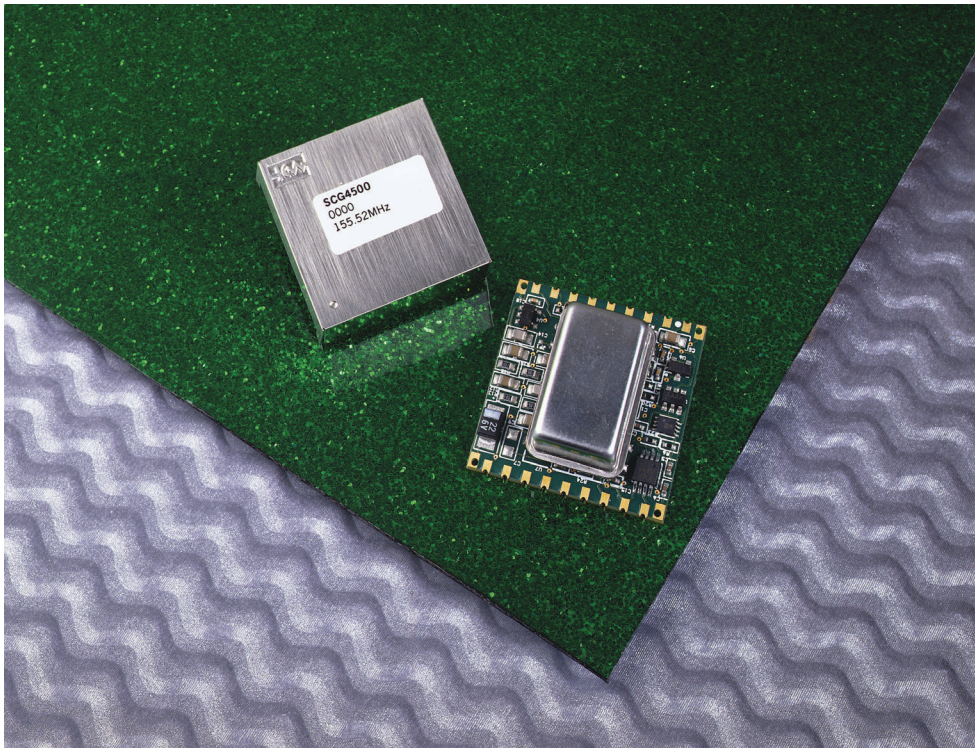
www.conwin.com



Features

- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- LVPECL Outputs with Disable Function
- Dual Input References
- LOR & LOL combined alarm output
- Force Free Run Function
- Automatic Free Run operation on loss of both References A & B
- Input Duty Cycle Tolerant
- 3.3V dc Power Supply
- Small Size: 1 Square Inch

Bulletin	**SG026**
Page	**1 of 16**
Revision	**P08**
Date	**08 Oct 02**
Issued By	**MBatts**

General Description

The SCG4500 Series is a mixed-signal phase locked loop generating LVPECL outputs from an intrinsically low jitter, voltage controlled, crystal oscillator. The LVPECL outputs may be disabled.

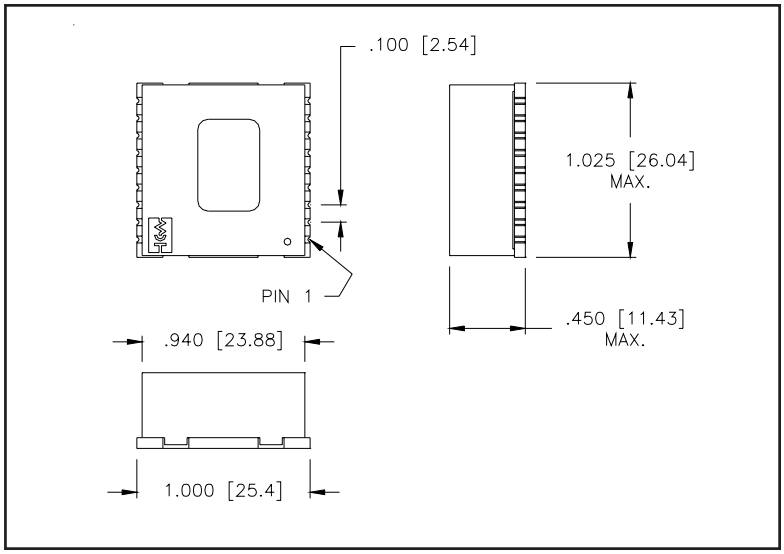
The SCG4500 Series can lock to one of two external references, which is selectable using the SEL_{AB} input select pin. The unit has a fast acquisition time of about 1.5 seconds and it is tolerant of different reference duty cycles.

The SCG4500 Series includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 ppm. Additionally the Free Run mode may be entered manually.

The package dimensions are 1" x 1.025" x .45" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloys, 180°C surface mount reflow processes.

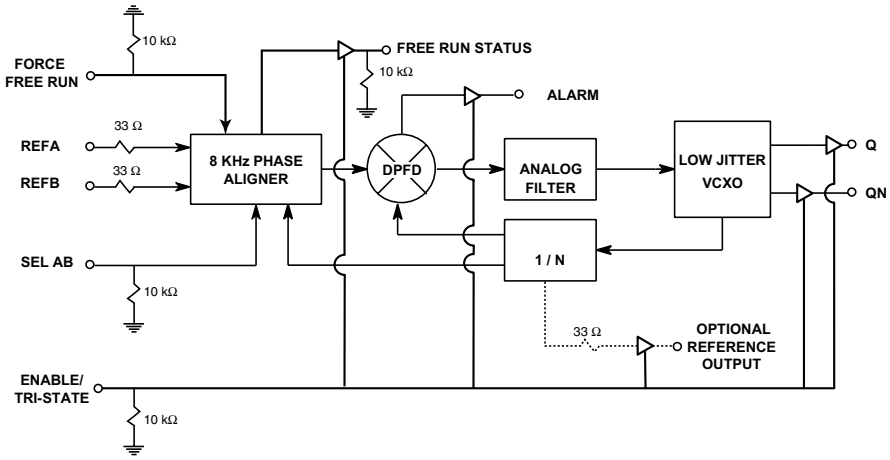
Maximum Dimension Package Outline

Figure 1



Block Diagram

Figure 2



Model Comparison Table

Table 1

Model	Dual Input Ref Freq	Max Duty Cycle	LVPECL Oscillator Output (Pins 16 & 18)	Notes
SCG4500	8 kHz/8 kHz	40/60	77.76 MHz,155.52 MHz,125 MHz	Basic Model
SCG4510	**1.544MHz/1.544MHz**	40/60	155.52 MHz	
SCG4520	**19.44 MHz/19.44 MHz**	40/60	77.76 MHz,155.52 MHz	

*Features which differentiate a model from the base model (SCG4500) are highlighted in boldface color and in the notes column.

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Absolute Maximum Rating

Table 1 — All SCG4500 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+100	°C	1.0

Operating Specifications

Table 2 — All SCG4500 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	2.0
I_{cc}	Power Supply Current	170	230	280	mA	5.0
T_o	Temperature Range	0	-	70	°C	
F_{fr}	Free Run Frequency	-20	-	20	ppm	
F_{cap}	Capture/pull-in range	-25	-	25	ppm	
F_{bw}	Jitter Filter Bandwidth	-	-	10	Hz	3.0
T_{jtol}	Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	31.25 1	- -	- -	µs µs	8 kHz Ref. units 19.44 MHz Ref. units
T_{aq}	Acquisition Time	-	1	-	s	4.0
T_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	5.0
DC	Output Duty Cycle	40	50	60	%	
$MTIE_{sr}$	MTIE at Synchronization Rearrangement		GR-253-CORE.1999 R5-136			6.0, 7.0
	Dynamic Offset Range (0°- 25°)	-50	-	50	ns	
	Dynamic Offset Range (25°- 70°)	-50	-	50	ns	

Output Jitter Specifications

Table 4 — All SCG4500 Models

Frequency (MHz)	Jitter BW 10 Hz - 1 MHz pS (RMS)	Jitter BW 10 Hz - 1 MHz m UI	SONET Jitter BW 12 kHz - 20 MHz pS (RMS)	SONET Jitter BW 12 kHz - 20 MHz m UI
77.76	10 Typ.	0.776 Typ.	1 Max.	0.076 Max.
125.00	10 Typ.	1.250 Typ.	1 Max.	0.125 Max.
155.52	10 Typ.	1.556 Typ.	1 Max.	0.156 Max.

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (22 uF, 330 pF)

3.0 3db loop response.

4.0 From a 20 PPM step in reference frequency at 25°C @ 3.3V

5.0 50-ohm load biased to 1.3 volts.

6.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

7.0 If the selected reference is removed system response to the ALARM must be less than 10µs.

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Input And Output Characteristics

Table 3 — All SCG4500 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input and Output Characteristics						
V_{ih}	High Level Input Voltage	2.0	-	5.5	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage	-	-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
PECL Output Characteristics						
V_{oh}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{ol}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_l	Output Capacitance	-	-	10	pF	
T_{skew}	Differential Output Skew	-	50	-	ps	

Input Selection / Output Response

Table 4 — All SCG4500 Models

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	X	X	X	FR
X	1	X	X	X	X	X	X	0	1	
0	0	X	X	X	1	1	X	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:
A Active
FR Free Run Mode
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

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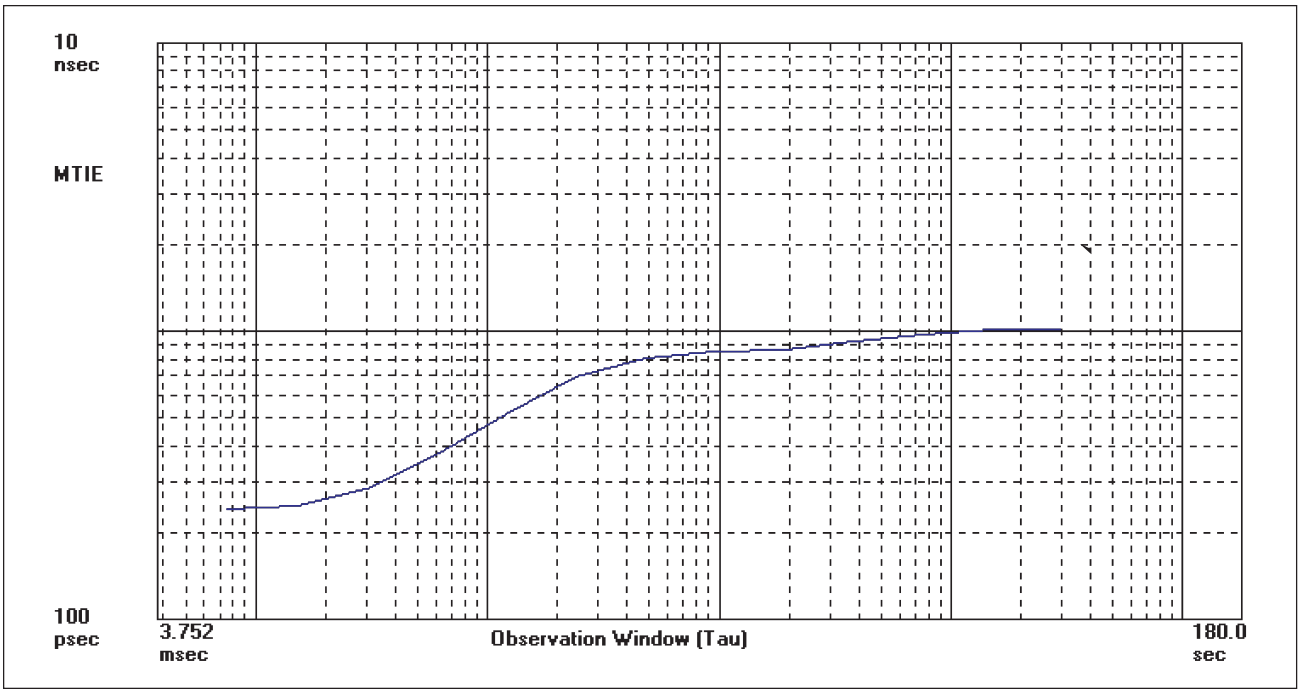
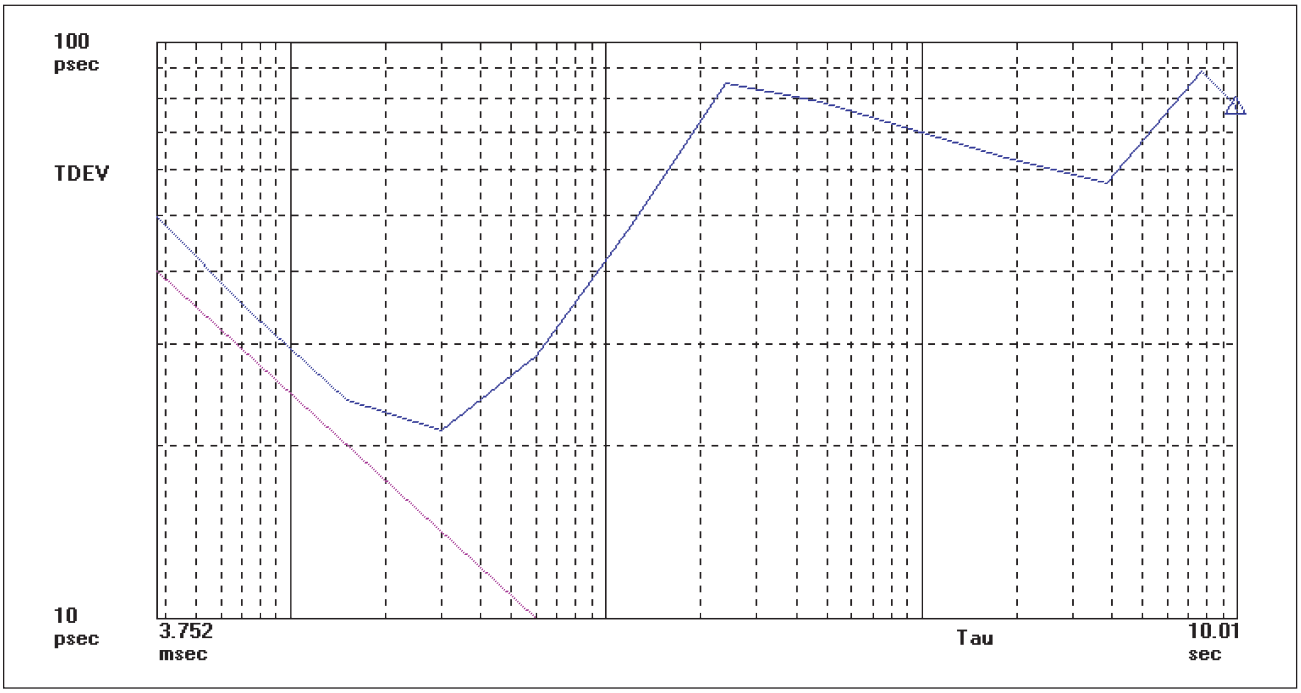
Typical MTIE Measurement

Figure 3



Typical TDEV Measurement

Figure 4



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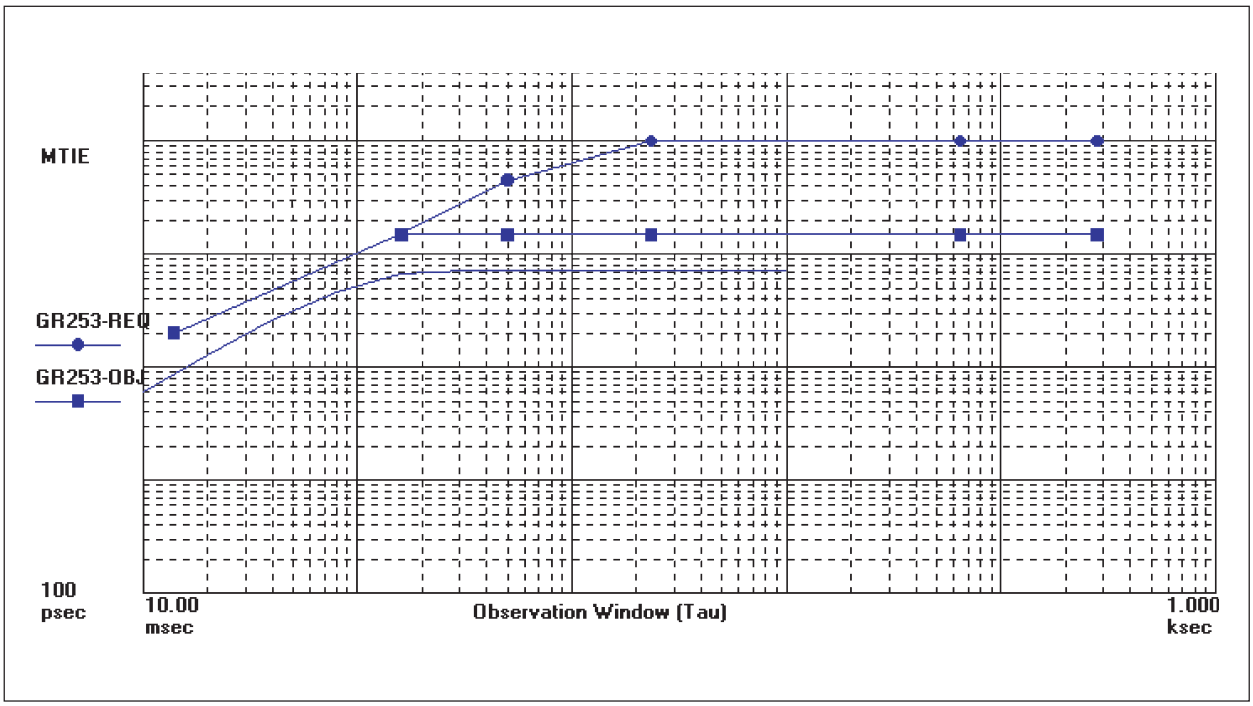
Typical MTIE at Synchronization Rearrangement. Reference B Equal to Inverse of Reference A, No Modulation.

Figure 5



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Pin Description

Table 5 — All SCG4500 Models

Pin #	Pin Name	Pin Information	Note
1	ENABLE/TRI-STATE	VCXO Enable. (Enable = 0, Disable = 1 = CMOS Outputs Tri-stated)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	CMOS Reference Frequency Input.	
5	SEL_{AB}	Input Reference Select Pin. (REFA = 0, REFB = 1)	9.0
6	RESET	RESET. (RESET = 1)	9.0
7	REF_B	CMOS Reference Frequency Input.	
8	V_{ee}	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	N/C	No Connection. (Optional Reference Output Available)	8.0, 8.1
12	ALARM	Loss of Reference / Lock alarm. (Alarm = 1)	
13	FR	Force Free Run. (Phase Lock = 0, Free Run = 1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	LVPECL Complementary Output.	
17	V_{ee}	Ground.	
18	Q	LVPECL Output.	

NOTES

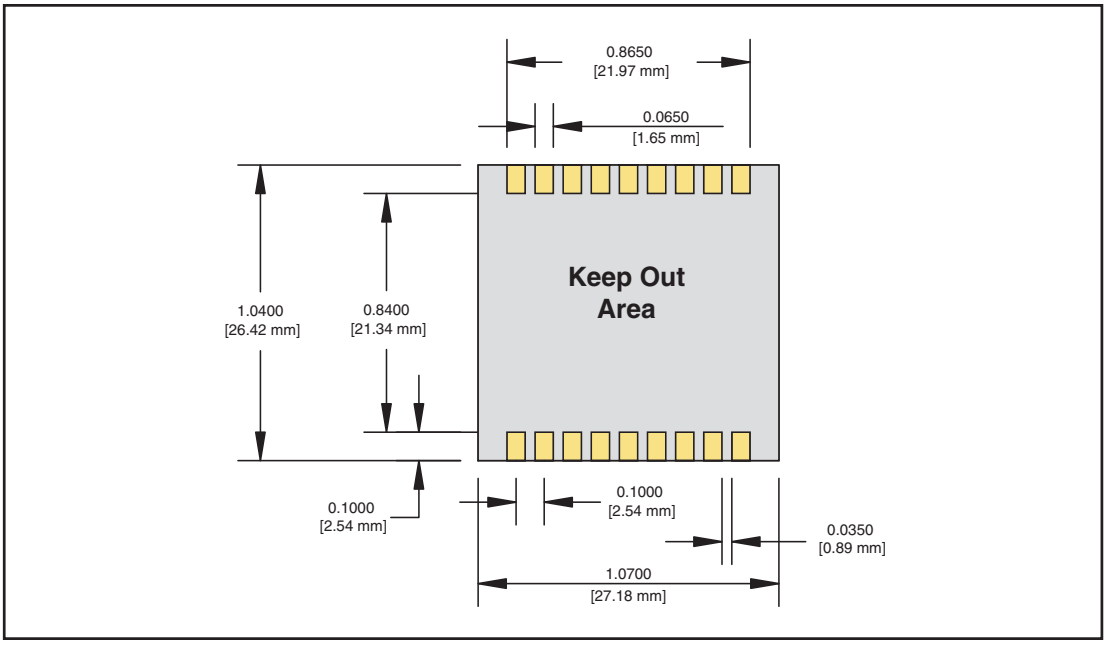
8.0 Do not connect pin

8.1 Contact a Sales Representative for availibilty and use of optional reference output

9.0 Input pulled to ground

Circuit Board Footprint & Keepout Recommendations

Figure 6



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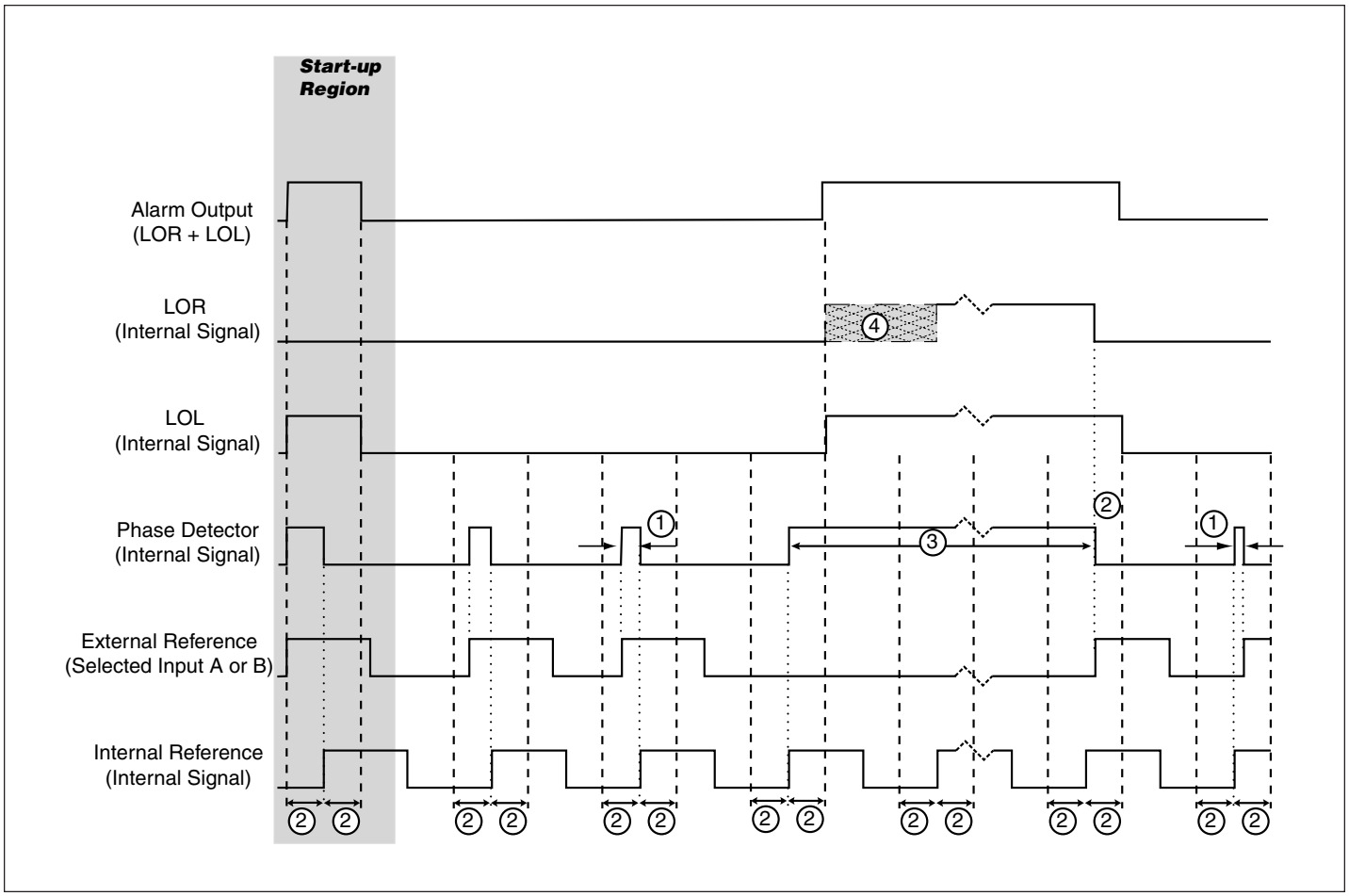
Loss of Reference Condition Alarm Timing

Figure 7



AlarmTiming Legend

Use for all alarm timing diagrams

Table 6

	19.44 MHz Reference Input Units	8 kHz Reference Input Units
1	< 1 µsec	< 31.25 µsec
2	1 µsec	31.25 µsec
3	> 1 µsec	> 31.25 µsec
4	LOR is active when LOL is active	125 µsec wide range
5	Minimum pulse width = 2 µsec	Minimum pulse width = 62.5 µsec
Start-up Region	During Start-up, The LOL Alaram will pulse during the few seconds of operation	

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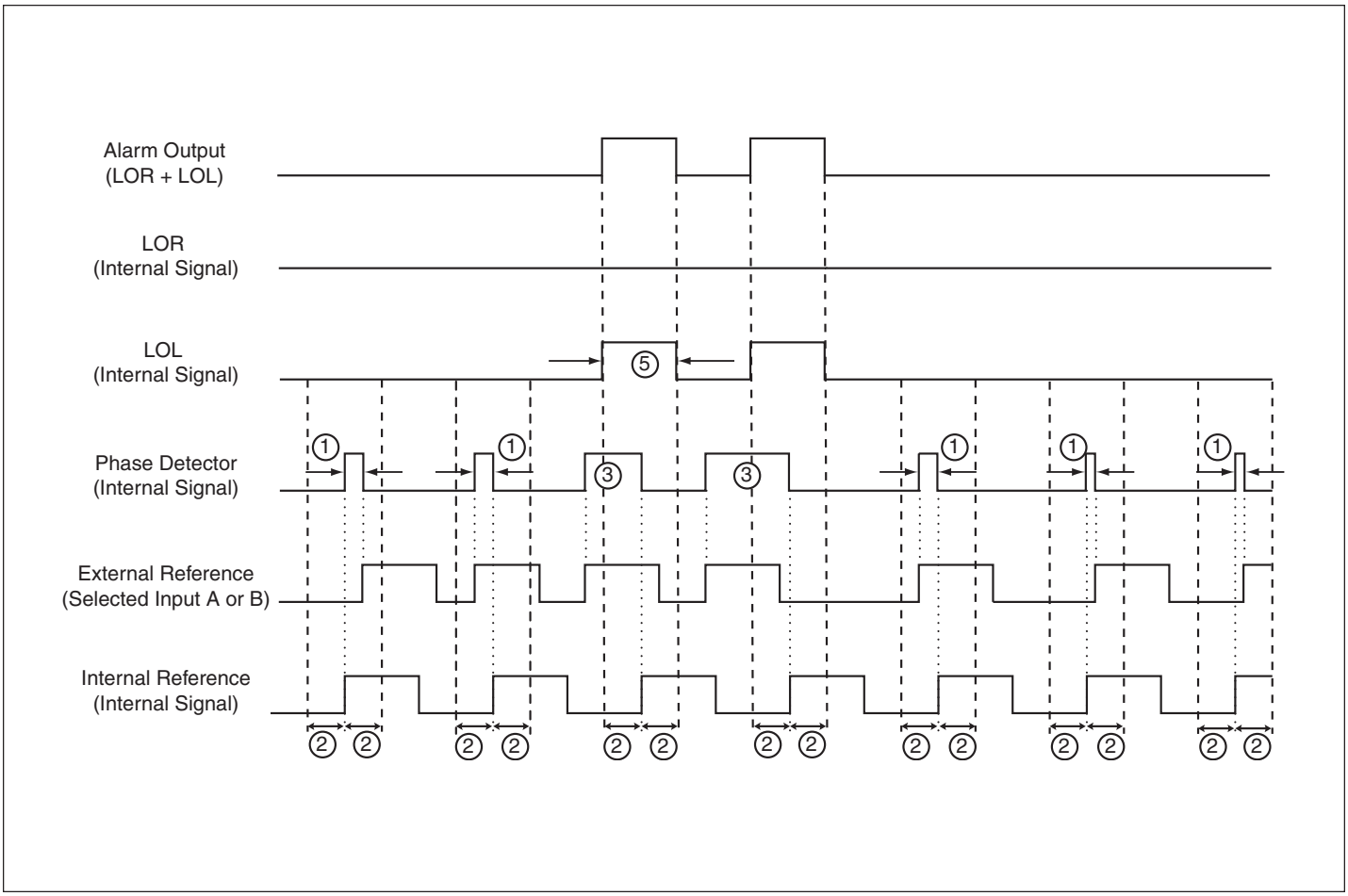
Loss of Lock Condition Alarm Timing

Figure 8



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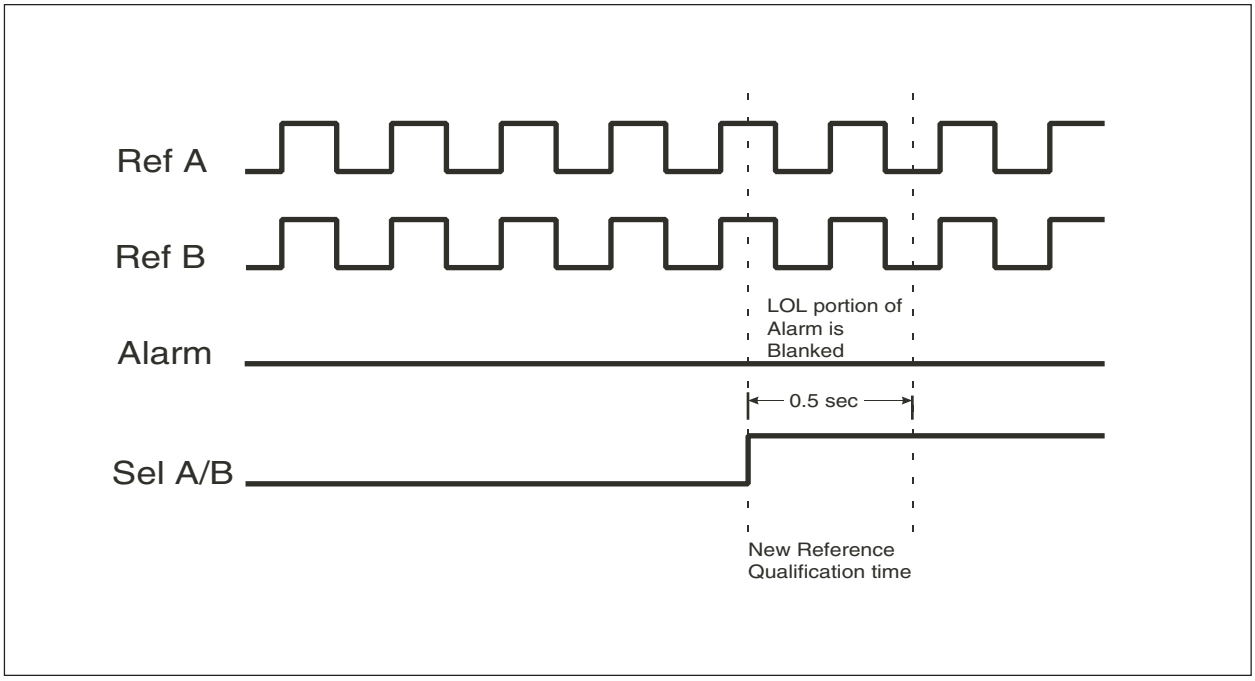
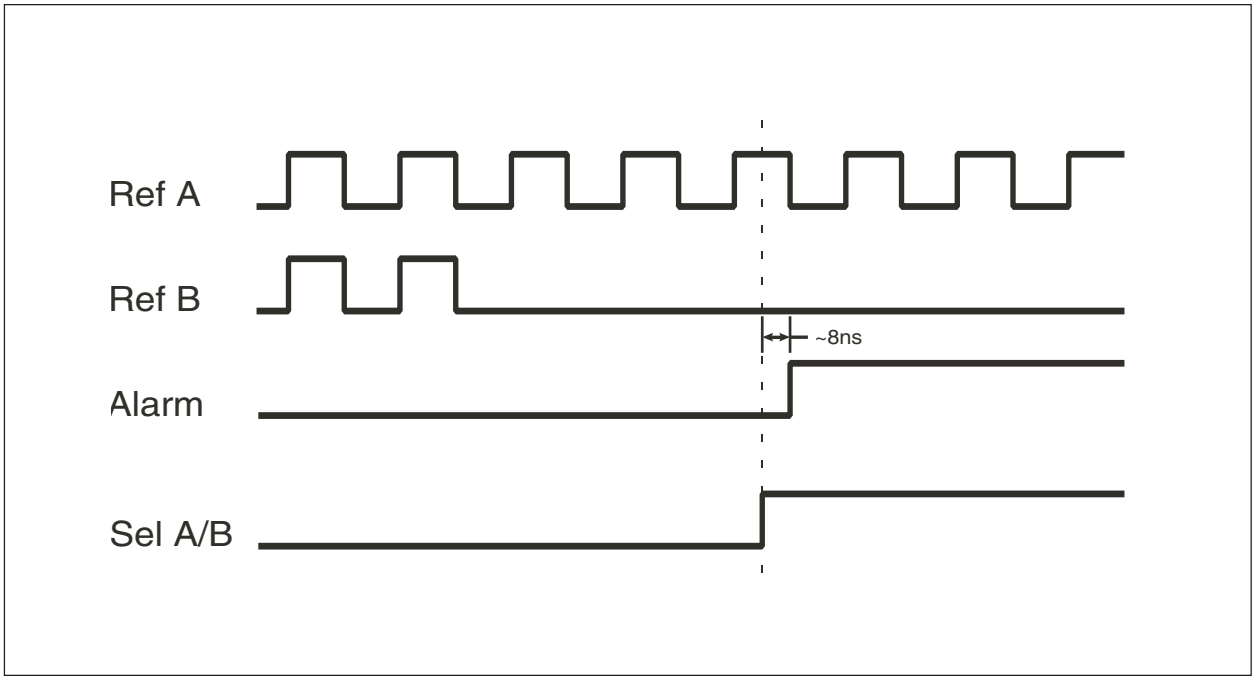
Switch from A to B when both are good signals

Figure 9



Switch from A to B when Reference B is lost

Figure 10



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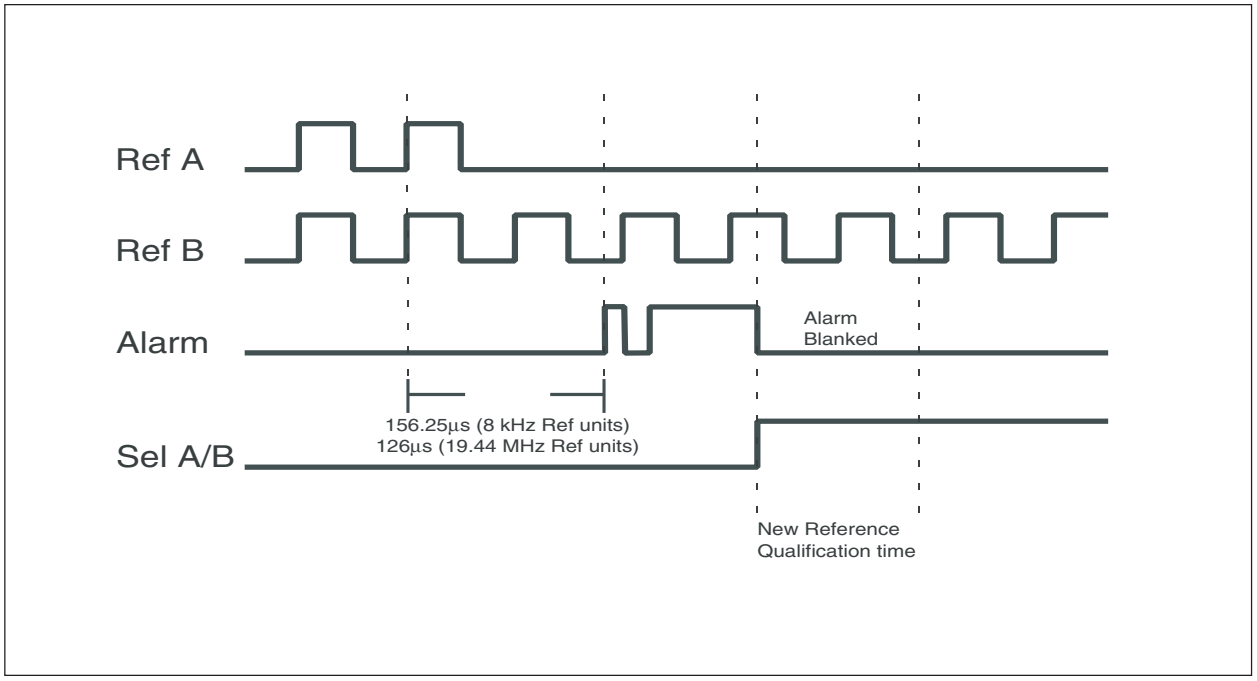
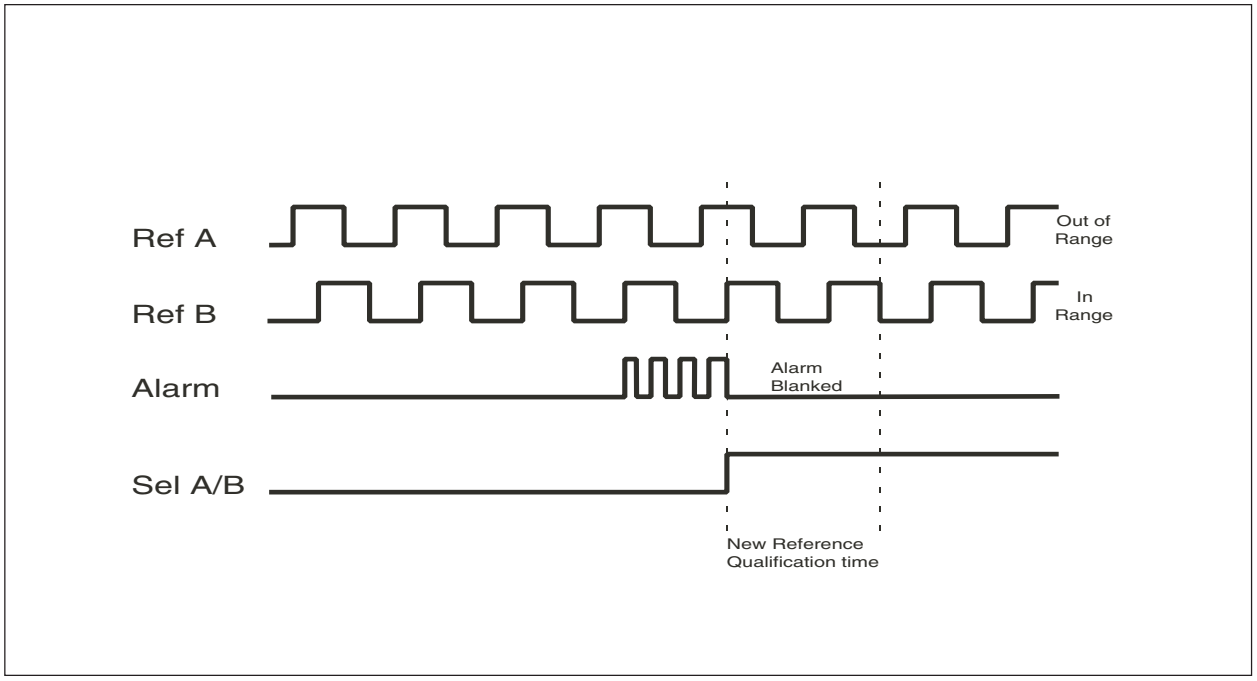
Switch from A to B after Reference A is lost

Figure 11



Switch from A to B when A is out of range

Figure 12



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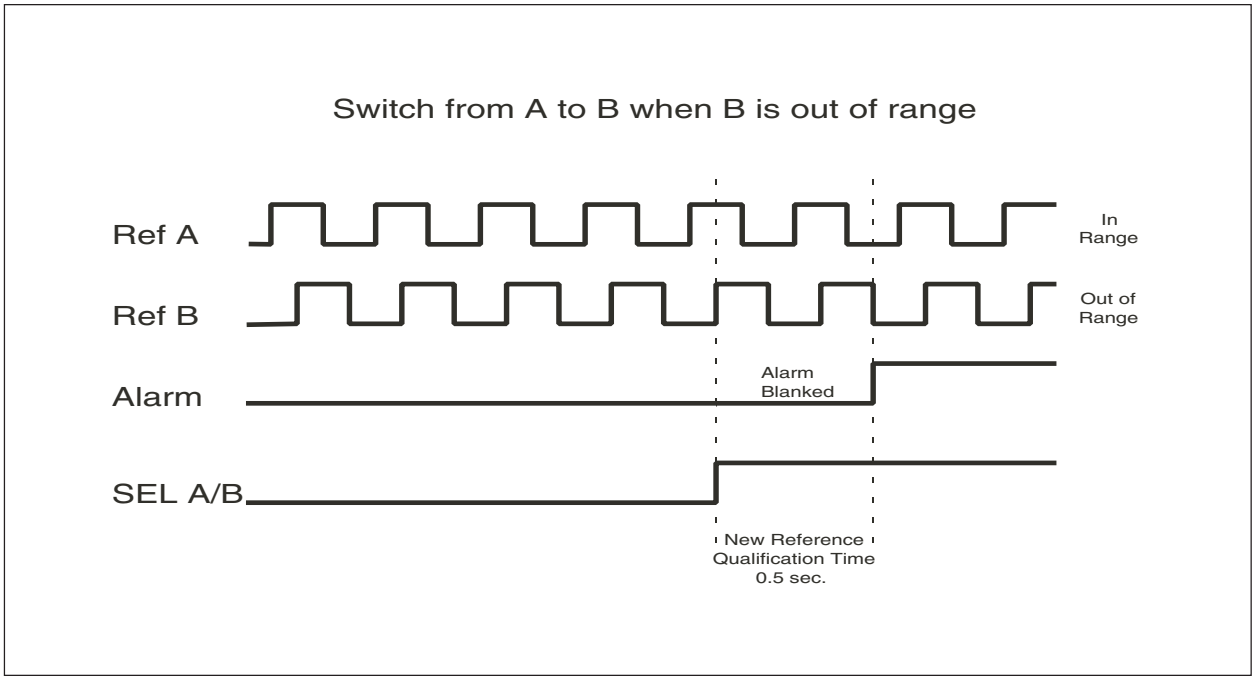
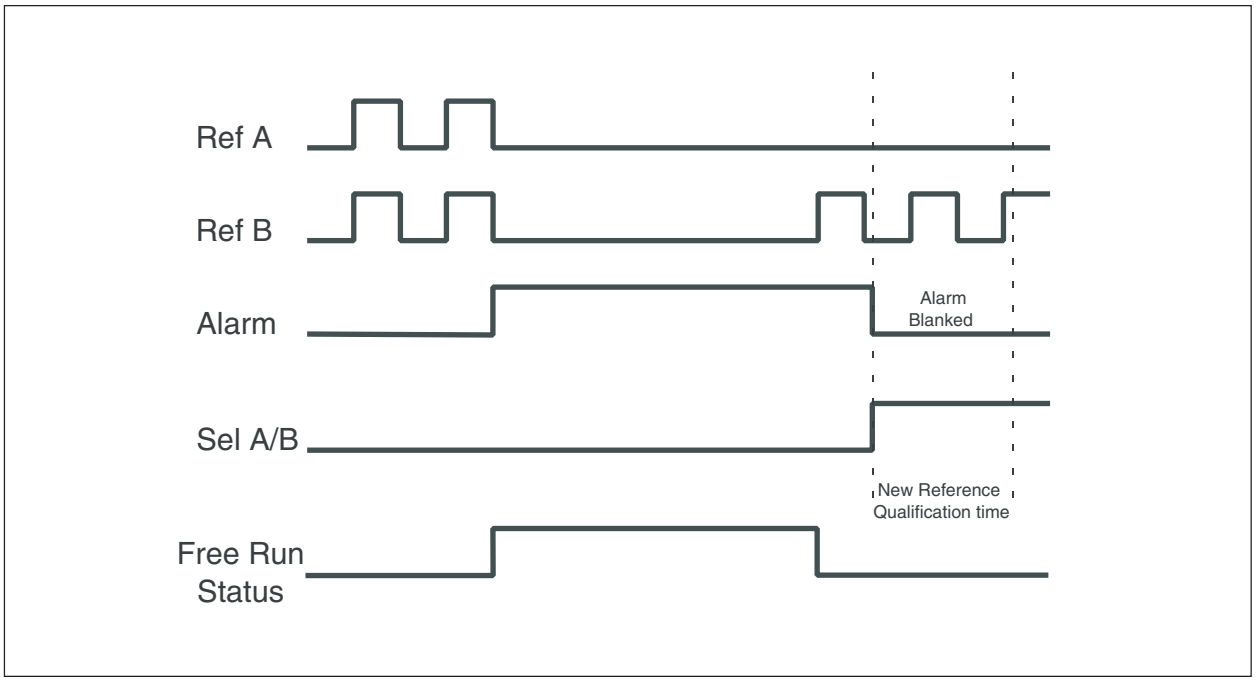
Switch from A to B when B is out of range

Figure 13



Switch from A to B when B is out of range

Figure 14



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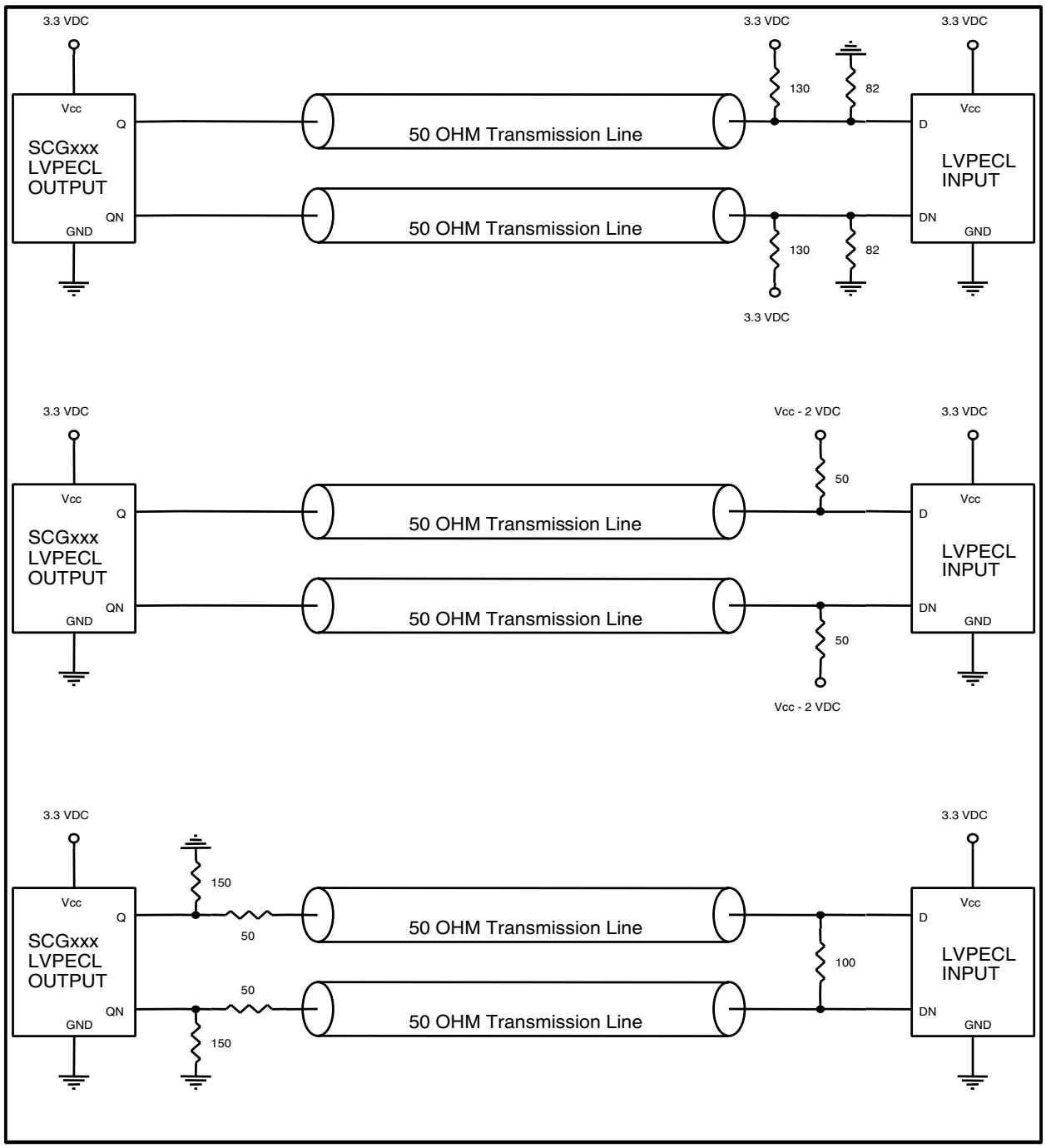
Recommended PECL Termination

Figure 15



If PECL outputs do not drive a long line (< 0.5”),
a single 150Ω termination resistor to ground may be used for each pin.

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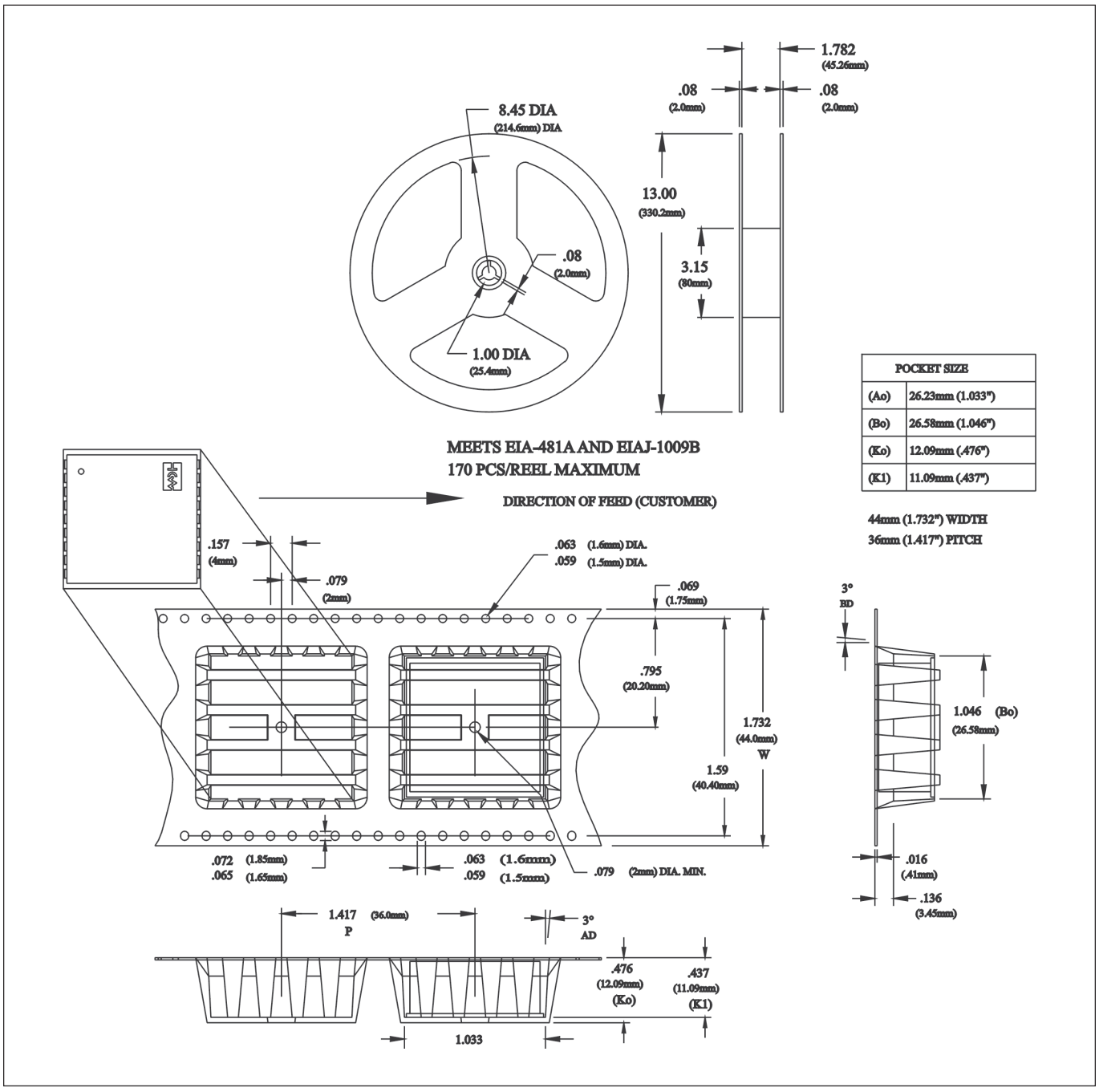
Tape and Reel Packaging

Figure 16



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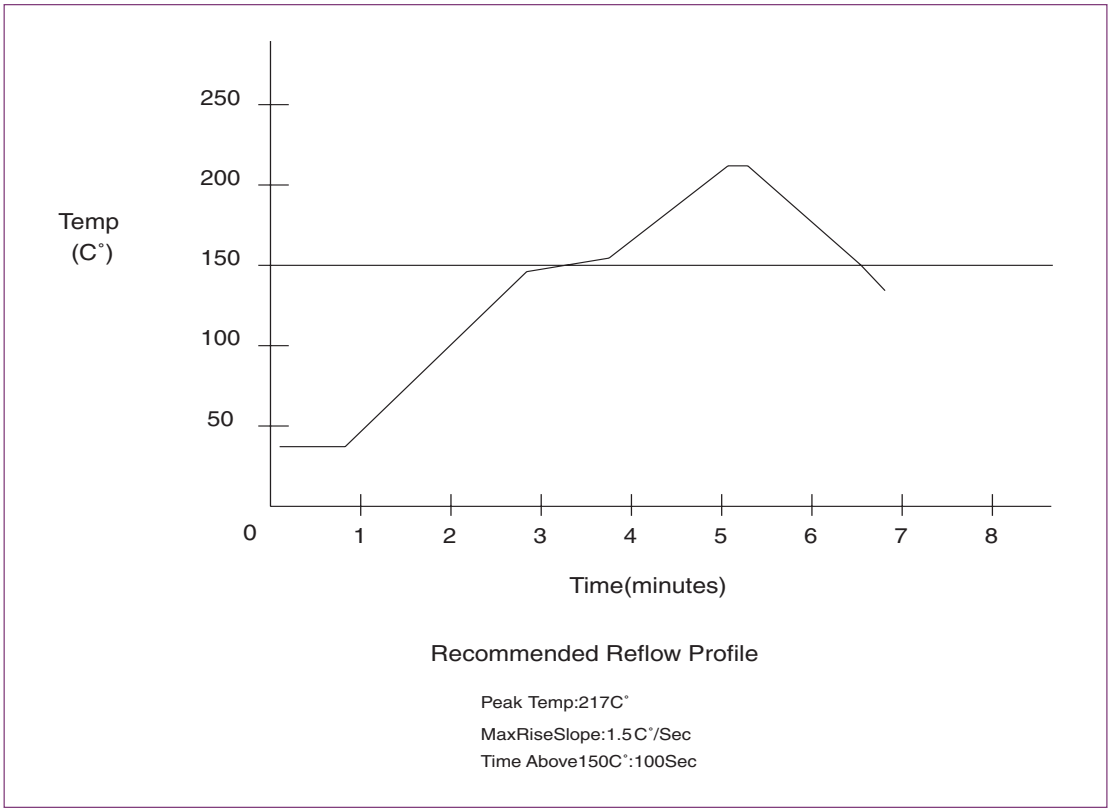
Solder Profile

Figure 17



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Revision	Revision Date	Note
P00	03/26/01	Preliminary informational release
P01	06/20/01	Added new products to Table 1
P02	07/10/01	Added new frequency to SCG4500
P03	07/30/01	Added new frequency to SCG4520
P04	09/06/01	Corrected mech. drawing and supply current
P05	10/18/01	Added 77.76 MHZ to SCG4500 model
P06	02/19/02	Changed dimension to maximums
P07	03/20/02	Updated alarm diagrams
P08	10/08/02	Revised mech. dimensions and drawings