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SCH3221

LPC I/O with Quad UARTs, GPIO and Wake

Product Features

- General Features
  - 3.3 Volt Operation (5 Volt Tolerant)
  - PC99, PC2001 Compliant
  - ACPI Compliant
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - Two Address Options for Power On Configuration Port
  - System Management Interrupt (SMI)
- Low Pin Count Bus (LPC) Interface
- 33 General Purpose I/O pins
- Programmable Wake-up Event (PME) Interface
  - Serial Modem RI Inputs
  - GPIOs
  - Watchdog
- 4 Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ, and 4 DMA Options
- Two LED Drivers with Blinking Options
- Watchdog Timer
- Temperature Ranges Available
  - Industrial (+85°C to -40°C)
  - Commercial (+70°C to 0°C)
- 64-Ball WFBGA RoHS Compliant Package

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Table of Contents

1.0 INTRODUCTION

1.1 Description

The SCH3221 is a 3.3V (5V tolerant) PC99/PC2001 compliant I/O controller with an LPC interface. The SCH3221 includes 4 Full-Function Serial Ports, IrDA and Consumer IR capability, GPIOs, and extensive PME Wake support from these features.

The SCH3221 is ACPI compatible and supports multiple low power-down modes.

I/O functionality includes four serial ports. The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 460 Kbps. They all have the full 8 pin interface.

The PME Wake logic includes the ability to wake from a watchdog timer, any of the UART Ring Indicator (RI) Inputs, or GPIOs.

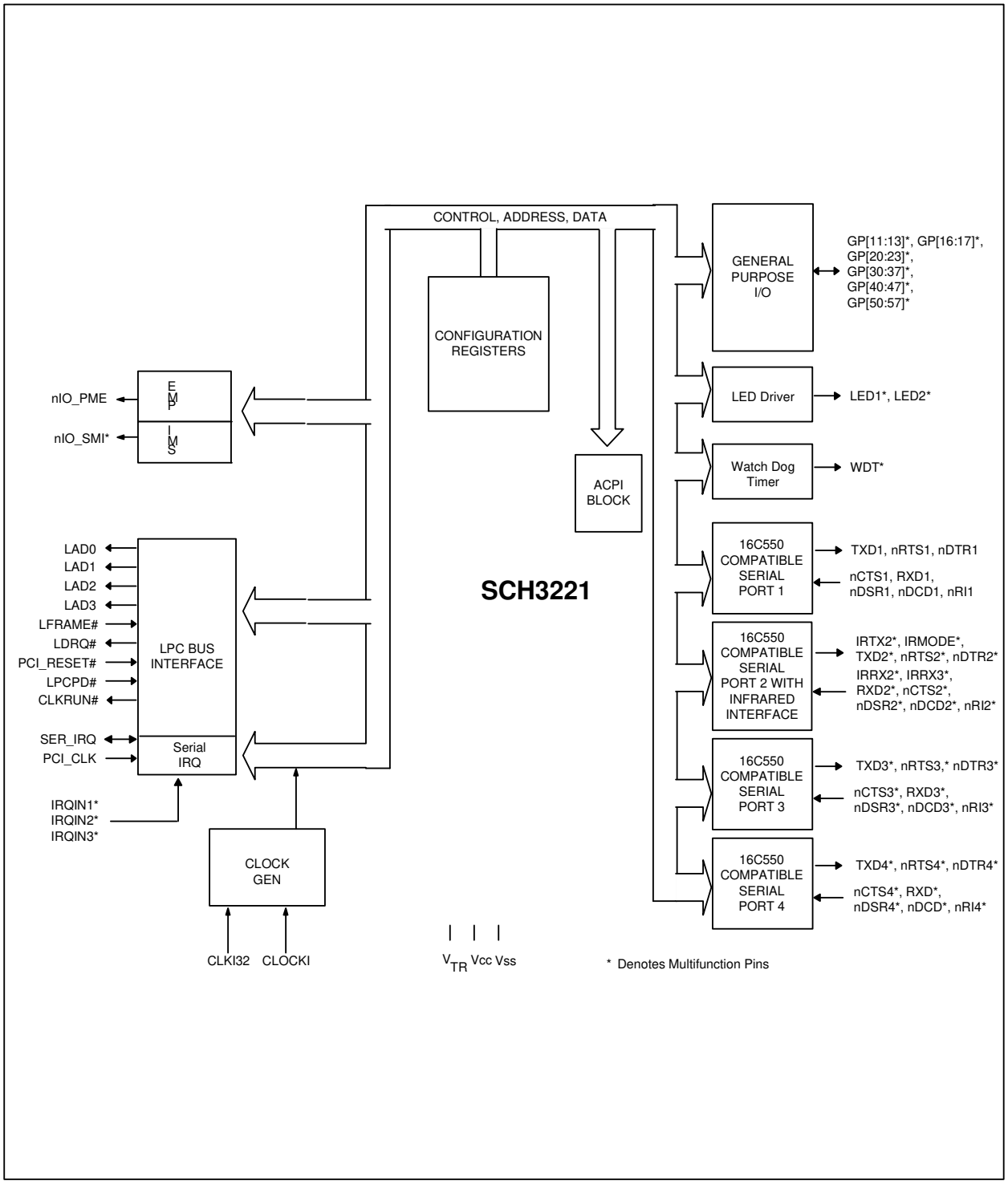
SMI Generation is also supported.

System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, a Watchdog Timer, and control of two LED's.

CAUTION: This device contains circuits which must not be used because their pins are not brought out of the package, and are pulled to known states internally. Any features, and especially SIO blocks that are not listed in this document, must not be activated or accessed. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.
As part of this, it is also necessary to pull the GP57/nDTR2 pin low, as a strap, to disable LPC Memory cycle handling. See Note 3-12 on page 13.

1.2 Block Diagram

FIGURE 1-1: SCH3221 BLOCK DIAGRAM



1.3 References

1. SMSC Infrared Communications Controller (IrCC) Specification, dated 5/10/96
2. PCI Bus Power Management Interface Specification, Revision 1.0, Draft, March 18, 1997
3. Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document
4. Advanced Configuration and Power interface Specification, Revision 1.0

2.0 PIN LAYOUT

Figure 2-1 shows the ball footprint for the SCH3221. See Table 2-1 below it for the pin function assignments.

FIGURE 2-1: SCH3221 FOOTPRINT DIAGRAM, TOP VIEW

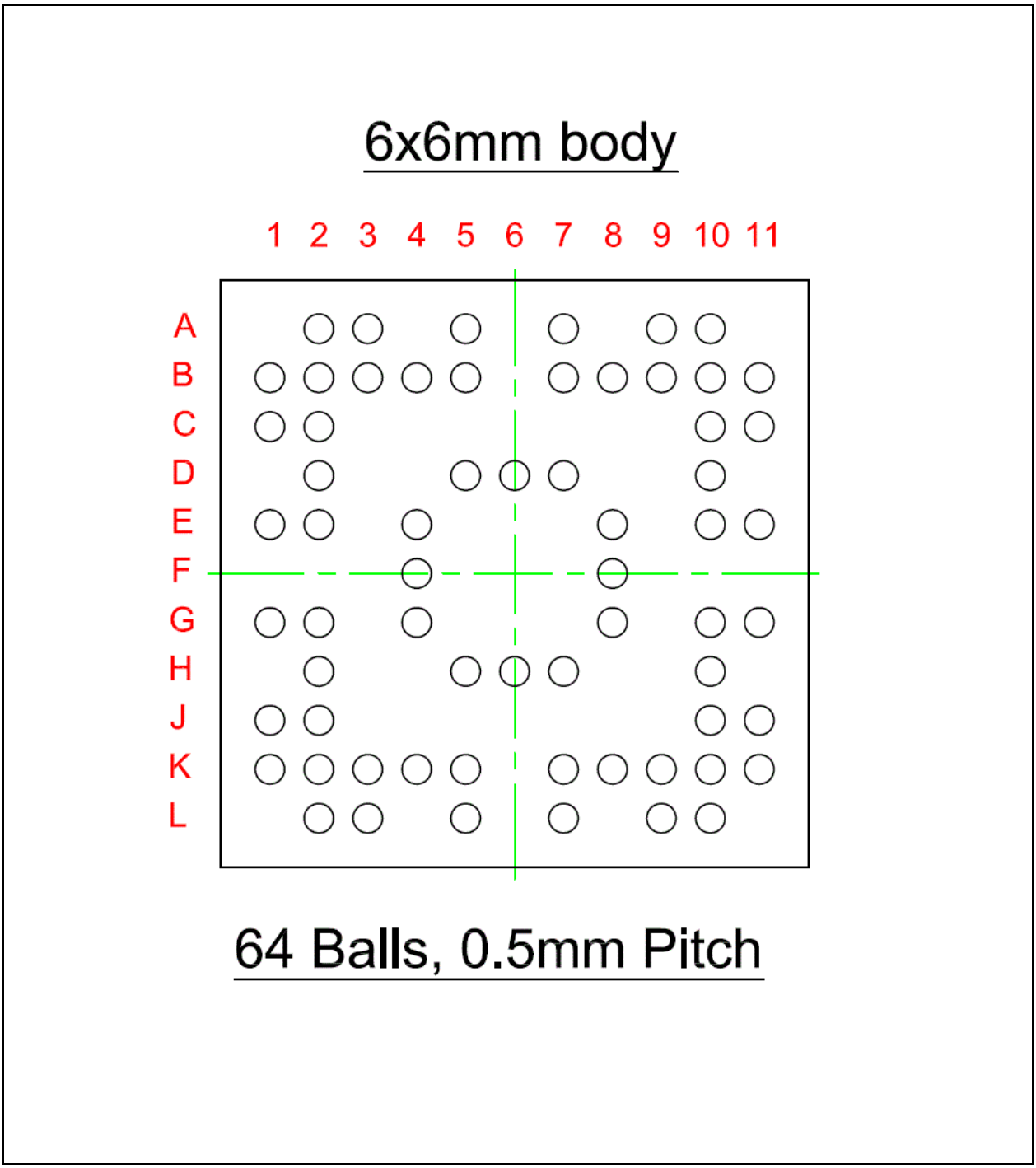


TABLE 2-1: SCH3221 SUMMARY

BALL#	FUNCTION
B3	GP11
A3	TEST=VSS
B5	CLOCKI
D6	VSS
B2	CLKI32
B1	IO_PME#
F4	VTR
C1	GP23 / nLED2 / IRQIN2
E2	LAD0
D2	LAD1
E1	LAD2
G1	LAD3
E4	VCC
G2	LFRAME#
H5	VSS
B4	LDRQ#
A2	PCI_RESET#
J1	LPCPD#
J2	CLKRUN#
K1	PCI_CLK
K2	SER_IRQ
K3	GP30 / nRI3
L2	GP31 / nDCD3
L3	GP32 / RXD3
K4	GP33 / TXD3
H2	GP34 / nDSR3
L5	GP35 / nRTS3
K5	GP36 / nCTS3
L7	GP37 / nDTR3
G4	GP40 / nRI4
A5	GP41 / nDCD4
C2	GP42 / RXD4
L9	GP43 / TXD4
F8	GP44 / nDSR4
H6	GP45 / nRTS4
G8	GP46 / nCTS4
E8	VCC
K7	GP47 / nDTR4
J11	GP12 / IO_SMI#
H7	VSS
L10	GP13 / IRQIN1 / nLED1
K11	GP16
K8	GP17
K9	GP20 / IRRX2 / IRQIN3

TABLE 2-1: SCH3221 SUMMARY (CONTINUED)

BALL#	FUNCTION
J10	GP21 / IRTX2 / WDT
K10	GP22 / IRMODE / IRRX3
G11	RXD1
G10	TXD1
H10	nDSR1
A7	nRTS1 / SYSOPT
B7	nCTS1
E10	nDTR1
B8	nRI1
E11	nDCD1
C11	GP50 / nRI2
D10	GP51 / nDCD2
B9	GP52 / RXD2 / IRRX
C10	GP53 / TXD2 / IRTX
B10	GP54 / nDSR2
B11	GP55 / nRTS2
A10	GP56 / nCTS2
A9	GP57 / nDTR2
D5	VCC
D7	VSS

3.0 DESCRIPTION OF PIN FUNCTIONS

The following section describes the functionality of the pins for the SCH3221.

TABLE 3-1: PIN FUNCTIONS

Name	Function	Buffer Type (Note 3-1)	Power Well
POWER PINS			
VCC	+3.3 Volt Supply Voltage (Note 3-8)		
VTR	+3.3 Volt Standby Supply Voltage (Note 3-8)		
VSS	Ground		
CLOCK PINS			
CLKI32	32.768kHz Standby Clock Input (Note 3-3)	IS	VTR
CLOCKI	14.318MHz Clock Input	IS	VCC
SERIAL PORT 1 INTERFACE			
RXD1	Receive Data 1	IS	VCC
TXD1	Transmit Data 1	O12	VCC
nDSR1	Data Set Ready 1	I	VCC
nRTS1 /SYSOPT	Request to Send 1 /(System Option) (Note 3-4)	OP14	VCC
nCTS1	Clear to Send 1	I	VCC
nDTR1	Data Terminal Ready 1	OP14	VCC
nRI1	Ring Indicator 1	I	VCC (Note 3-13)
nDCD1	Data Carrier Detect 1	I	VCC
SERIAL PORT 2 INTERFACE			
GP50 /nRI2	General Purpose I/O /Ring Indicator 2	IO8	VCC (Note 3-13)
GP51 /nDCD2	General Purpose I/O /Data Carrier Detect 2	IO8	VCC
GP52 /RXD2 /IRRX	General Purpose I/O /Receive Data 2 /IRRX	IS/O8	VCC
GP53 /TXD2 /IRTX	General Purpose I/O /Transmit Data 2 /IRTX (Note 3-6, Note 3-7)	IO12	VCC
GP54 /nDSR2	General Purpose I/O /Data Set Ready 2	IO8	VCC
GP55 /nRTS2	General Purpose I/O /Request to Send 2	IO8	VCC
GP56 /nCTS2	General Purpose I/O /Clear to Send 2	IO8	VCC
GP57 /nDTR2	General Purpose I/O /Data Terminal Ready 2 **CAUTION:** External pull-down is required on this pin (Note 3-12).	IOP14	VCC
SERIAL PORT 3 INTERFACE			
GP30 /nRI3	General Purpose I/O (Note 3-11) /Ring Indicator 3	IO8	VCC (Note 3-13)
GP31 /nDCD3	General Purpose I/O (Note 3-11) /Data Carrier Detect 3	IO8	VCC (Note 3-13)
GP32 /RXD3	General Purpose I/O (Note 3-11) /Receive Data 3	IS/O8	VCC (Note 3-13)

TABLE 3-1: PIN FUNCTIONS (CONTINUED)

Name	Function	Buffer Type (Note 3-1)	Power Well
GP33 /TXD3	General Purpose I/O (Note 3-11) /Transmit Data 3	IO12	VCC (Note 3-13)
GP34 /nDSR3	General Purpose I/O (Note 3-11) /Data Set Ready 3	IO8	VCC (Note 3-13)
GP35 /nRTS3	General Purpose I/O (Note 3-11) /Request to Send 3	IO8	VCC (Note 3-13)
GP36 /nCTS3	General Purpose I/O (Note 3-11) /Clear to Send 3	IO8	VCC (Note 3-13)
GP37 /nDTR3	General Purpose I/O (Note 3-11) /Data Terminal Ready 3	IO8	VCC (Note 3-13)
SERIAL PORT 4 INTERFACE			
GP40 /nRI4	General Purpose I/O (Note 3-11) /Ring Indicator 4	IO8	VCC (Note 3-13)
GP41 /nDCD4	General Purpose I/O (Note 3-11) /Data Carrier Detect 4	IO8	VCC
GP42 /RXD4	General Purpose I/O (Note 3-11) /Receive Data 4	IS/O8	VCC
GP43 /TXD4	General Purpose I/O (Note 3-11) /Transmit Data 4	IO12	VCC
GP44 /nDSR4	General Purpose I/O (Note 3-11) /Data Set Ready 4	IO8	VCC
GP45 /nRTS4	General Purpose I/O (Note 3-11) /Request to Send 4	IO8	VCC
GP46 /nCTS4	General Purpose I/O (Note 3-11) /Clear to Send 4	IO8	VCC
GP47 /nDTR4	General Purpose I/O (Note 3-11) /Data Terminal Ready 4	IO8	VCC
IR INTERFACE			
GP20 /IRRX2 /IRQIN3	General Purpose I/O /IR Receive /IRQ Input 3	IS/O8	VCC (Note 3-13)
GP21 /IRTX2 /WDT	General Purpose I/O (Note 3-11) /IR Transmit (Note 3-5, Note 3-7) /Watch Dog Timer	IO12	VCC (Note 3-13)
MISCELLANEOUS AND GPIO PINS			
GP11	General Purpose I/O	IO12	VCC (Note 3-13)
GP12 /IO_SMI#	General Purpose I/O /System Mgt. Interrupt	IO12	VCC (Note 3-13)
GP13 /IRQIN1 /nLED1	General Purpose I/O / IRQ Input 1 /nLED1 (Note 3-9)	IO12	VCC (Note 3-13)
GP16	General Purpose I/O	IO8	VTR (Note 3-13)
GP17	General Purpose I/O	IO8	VCC
GP22 /IRMODE /IRRX3	General Purpose I/O (Note 3-11) /IR Mode /IR Receive 3	IS/O8	VCC (Note 3-13)

TABLE 3-1: PIN FUNCTIONS (CONTINUED)

Name	Function	Buffer Type (Note 3-1)	Power Well
GP23 /nLED2 /IRQIN2	General Purpose I/O /nLED2 (Note 3-10) /IRQ Input 2	IO12	VTR (Note 3-13)
TEST	Test Input **Tie to VSS except in Test modes.**	IS	VCC
LPC AND ASSOCIATED INTERFACE PINS			
IO_PME#	Power Management Event Output	OD12	VTR
PCI_CLK	PCI Clock	PCI_ICLK	VCC
SER_IRQ	Serial IRQ	PCI_IO	VCC
LAD0	Multiplexed Command Address and Data 0	PCI_IO	VCC
LAD1	Multiplexed Command Address and Data 1	PCI_IO	VCC
LAD2	Multiplexed Command Address and Data 2	PCI_IO	VCC
LAD3	Multiplexed Command Address and Data 3	PCI_IO	VCC
LFRAME#	Frame	PCI_I	VCC
LDRQ#	Encoded DMA Request	PCI_O	VCC
PCI_RESET#	PCI Reset	PCI_I	VCC
LPCPD#	Power Down (Note 3-1)	PCI_I	VCC
CLKRUN#	PCI Clock Controller	PCI_OD	VCC

Note: The "n" as the first letter of a signal name or the “#” as the suffix of a signal name indicates an "Active Low" signal.

Note 3-1 Pins that have input buffers must always be held to either a logical low or a logical high state when powered. Bi-directional buses that may be tristated should have either weak external pull-ups or pull-downs to prevent the pins from floating.

Note 3-2 The LPCPD# pin may be tied high. The LPC interface will function properly if the PCI_RESET# signal follows the protocol defined for the LRESET# signal in the “Low Pin Count Interface Specification”.

Note 3-3 If the 32kHz input clock is not used the CLKI32 pin must be grounded. There is a bit in the configuration register at CR1E that determines whether the 32KHz clock input is used as the clock source for the WDT and the LED’s. Set this bit to ‘1’ if the clock is not connected.

Note 3-4 The nRTS1/SYSOPT pin requires an external pulldown resistor to put the base I/O address for configuration at 0x02E. An external pullup resistor is required to move the base I/O address for configuration to 0x04E.

Note 3-5 The GP21/IRTX2/WDT pin is tristate when VCC=0. The pin comes up as an output and low following a VCC POR and Hard Reset if configured for IRTX2 function. The GP21/IRTX2/WDT pin will remain low following a power-up (VCC POR) if configured for IRTX2 until serial port 2 is enabled by setting the UART2 Power bit to ‘1’. Once the power has been applied the pin will reflect the state of the IR transmit output of the IRCC block. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 3-6 The GP53/TXD2/IRTX pin defaults to tristate when the part is under VTR power (VCC=0). The pin comes up tristate following a VTR POR, VCC POR, and Hard Reset. If the pin is configured for alternate functions TXD2 or IRTX the GP53/TXD2/IRTX pin will remain tristate following a power-up (VCC POR) until the UART2 Power bit is set to ‘1’. Once the power has been applied to the UART, the pin will reflect the current state of the output transmit buffer. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 3-7 VTR can be connected to VCC if no wakeup functionality is required.

Note 3-8 VCC must not be greater than 0.5V above VTR.

Note 3-9 The nLED1 pin is powered by VCC and can only be controlled when the part is under VCC power.

Note 3-10 The nLED2 pin is powered by VTR so that the LED can be controlled when the part is under VTR power.

Note 3-11 These GPIO pins only have push-pull buffers. They cannot be configured for open drain outputs.

Note 3-12 **CAUTION:** This pin floats during VCC POR and must be pulled low externally during this time for correct LPC bus operation. A weak external pull-down resistor may be used for this. Failure to provide this may cause this device to improperly react to LPC Memory traffic, and this in turn can cause excessive current, unpredictable system operation, and damage to the device.

Note 3-13 These pins have input buffers into the wakeup logic that are powered by VTR.

Note 3-14 This buffer type is different from the buffer types shown per function because it is a pin that supports alternate functions that require additional buffer types.

3.1 Buffer Type Description

I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
IPD	Input with 30uA Integrated Pull-Down
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 3-15)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 3-16)

Note 3-15 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.

Note 3-16 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

3.2 Design Guidelines for Implemented Buffer Types

The characteristics of the I/O buffers implemented in this device are defined in Section 9.2, "DC Electrical Characteristics," on page 102. Care should be taken to ensure that external devices maintain acceptable voltage levels on all inputs and open drain outputs. It is not advisable to allow input buffers to float or remain in an indeterminate state.

Note:	It is important not to cross power domains when attaching pull-ups to pins. Pins that are located on the VCC power well must be pulled either to ground or to VCC. This includes GPIO pins with wakeup capability that are located on the VCC power well (see Table 3-1, “Pin Functions,” on page 10).

Pins that are located on the VTR power well must be pulled either to ground or to VTR.

The following is a list of design guidelines to help identify which pins require external pull-up/pull-down resistors:

1. Input buffers that are of type I or IS must be driven to a logic high or a logic low when power is applied to the buffer. If the external device controlling the input buffer tristates while power is applied to the buffer, an external pull-up/pull-down resistor should be added to prevent the pin from floating.
2. All output pins that are implemented as open drain outputs, must be pulled through an external resistor to the proper VCC or VTR power plane.
3. All GPIO registers default to a GPIO input on a VTR POR. On a cold boot, a VCC POR will implement these pins as GPIO inputs. It is suggested that these pins are pulled to their inactive state (either to the proper VCC or VTR power plane or ground) depending on the function being implemented on the pin.

4.0 3.3 VOLT OPERATION / 5 VOLT TOLERANCE

The SCH3221 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- LFRAME#
- LDRQ#
- LPCPD#

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- PCI_RESET#
- PCI_CLK
- SER_IRQ
- CLKRUN#
- IO_PME#

5.0 POWER FUNCTIONALITY

The SCH3221 has two power planes: VCC and VTR.

5.1 VCC Power

The SCH3221 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

5.2 VTR Support

The SCH3221 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and the Maximum Current Values subsection. If the SCH3221 is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. The VTR pin generates a VTR Power-on-Reset signal to initialize these components.

Note:	If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 s before VCC begins a power-on cycle. When VTR and VCC are fully powered, the potential difference between the two supplies must not exceed 500mV.

5.3 32.768 kHz Trickle Clock Input

The SCH3221 utilizes a 32.768 kHz trickle input to supply a clock signal for the Watchdog Timer (WDT) and LED blink function.

Note:	LED1 has a VCC powered output pin and will only generate a signal when the device is powered by VCC. LED2 has a VTR powered output pin and may be used under VTR power.

The SCH3221 has two different methods of deriving a 32.768kHz signal:

- From an external single-input clock source driven on the CLKI32 pin
- From an internal PLL that divides down the14MHz clock input to make the 32kHz signal

If the 32kHz input clock is not used the CLKI32 pin must be grounded and the CLK32_PRSN bit should be set to '1'. This bit in the configuration register block at register index CR1E determines whether the internal 32KHz clock is derived from the CLKI32 pin or the 14MHz clock input. This clock input is used as the clock source for the WDT and the LEDs. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32kHz clock is connected to the CLKI32 pin (default)

1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the LED blink logic and the WDT. When the external 32kHz clock is connected, bit[0] should be set to '0' so that the external clock will be the source for the LED blink logic and the WDT. When the external 32kHz clock is not connected, bit[0] should be set to '1' so that an internal 32kHz clock source will be derived from the 14MHz clock for the LED blink logic and the WDT.

The following functions will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. These functions will work under VCC power even if the external 32kHz clock is not connected.

- LED blink
- WDT

5.4 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as VCC cycles on and off. When the internal PWRGOOD signal is "1" (active), VCC > 2.3V (nominal), and the SCH3221 host interface is active. When the internal PWRGOOD signal is "0" (inactive), VCC 2.3V (nominal), and the SCH3221 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The SCH3221 device pins IO_PME#, nRI1, nRI2, nRI3, nRI4, and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided VTR is powered. See Trickle Power Functionality section.

5.5 Trickle Power Functionality

When the SCH3221 is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the IO_PME# pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- UART 3 Ring Indicator
- UART 4 Ring Indicator
- WDT
- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup inputs are GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50. These GPIOs function as follows:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function).

See the Table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- CLKI32
- WDT block
- LED block
- LED2 pin
- Runtime register block (includes all PME, SMI, WDT, LED, and GP data registers)
- Pins for PME Wakeup:
  - GPIOs (GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50)
  - IO_PME#
  - nRI1, nRI2, nRI3, nRI4

5.6 Maximum Current Values

See Section 9.0, "Operational Description" for the maximum current values.

The maximum VTR current, ITR, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pins that are powered by VTR (as output) are IO_PME#, LED2 and nPME. These pins, if configured as a push-pull output, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, ICC, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

5.7 Power Management Events (PME/SCI)

The SCH3221 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the "PME Support" section.

6.0 FUNCTIONAL DESCRIPTION

6.1 Super I/O Registers

The address map, shown below in Table 6-1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the serial ports, runtime register block and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

6.2 Host Processor Interface

The host processor communicates with the SCH3221 through a series of read/write registers via the host processor interface. The port addresses for these registers are shown in Table 6-1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

TABLE 6-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name
Base+(0-7)	Serial Port Com 1
Base1+(0-7) Base2+(0-7)	Serial Port Com 2 (IR Support)
Base+(0-7)	Serial Port Com 3
Base+(0-7)	Serial Port Com 4
Base + (0-F)	Runtime Registers
Base + (0-1)	Configuration

Note 6-1 Refer to the configuration register descriptions for setting the base address.

6.3 LPC Interface

The SCH3221 communicates with the host over a Low Pin Count (LPC) interface. For a complete description of the LPC interface, see the Intel Low Pin Count Specification, Rev 1.0. The following sections define the LPC signals implemented, the cycles supported, and protocols implemented that are specific to this device.

Note: The LPC interface uses 3.3V signaling. For electrical specifications see the Intel Low Pin Count Specification, Rev 1.0 and the PCI Local Bus Specification, Rev 2.2.

6.3.1 LPC INTERFACE SIGNAL DEFINITION

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

TABLE 6-2: LPC BUS INTERFACE SIGNALS

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset.
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.
IO_PME#	OD	Power Mgt Event signal. Allows the SCH3221 to request wakeup.
LPCPD#	Input	Powerdown Signal. Indicates that the SCH3221 should prepare for power to be shut on the LPC interface.
PCI_CLK	Input	PCI Clock
CLKRUN#	I/OD	Clock Run. Allows the SCH3221 to request the stopped PCI_CLK be started.
IO_SMI#	OD	System Mgt Interrupt signal. Allows the SCH3221 to notify the host system that an event has occurred.

Note 6-2 The IO_PME#, IO_SMI#, and PCI_CLK signals are considered part of the host interface.

6.3.2 LPC CYCLES

The following cycle types are supported by the LPC protocol.

TABLE 6-3: LPC CYCLE TYPES

Cycle Type (Note 6-3)	Transfer Size
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

Note 6-3 The SCH3221 ignores cycles that it does not support.
CAUTION: A pull-down strap is necessary on the GP57/nDTR2 pin to ensure this, as well as to prevent chip damage. See Note 3-12 on page 13.

6.3.3 LFRAME# USAGE

LFRAME# is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the SCH3221 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the SCH3221 monitors the bus to determine whether the cycle is intended for it. The use of LFRAME# allows the SCH3221 to enter a lower power state internally. There is no need for the SCH3221 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the SCH3221 samples LFRAME# active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The LFRAME# signal functions as described in the Low Pin Count (LPC) Interface Specification Revision 1.0.

6.3.4 FIELD DEFINITIONS

LPC transactions are defined as being comprised of multiple fields. These fields may be one or more nibbles in length (nibble=4 bits). All LPC transactions begin with a START field and a Cycle Type/Direction field. The START field is used to initiate/terminate LPC transactions. The Cycle Type/Direction field is used to define the cycle type (I/O, DMA) and direction (read/write) for LPC cycles. The remaining fields of data being transfered are based on specific fields that are used in various combinations, depending on the cycle type. These remaining fields are driven on to the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the SCH3221. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields. The following sections describe the supported cycle types.

Note: I/O and DMA cycles use a START field of 0000.

6.3.4.1 I/O Read and Write Cycles

The SCH3221 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

6.3.4.2 DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the SCH3221. DMA write cycles involve the transfer of data from the SCH3221 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the SCH3221 are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

6.3.4.3 DMA Protocol

DMA on the LPC bus is handled through the use of the LDRQ# lines from the SCH3221 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Specification Revision 1.0.

6.3.5 POWER MANAGEMENT

6.3.5.1 CLOCKRUN Protocol

See the Low Pin Count (LPC) Interface Specification Reference, Section 8.1.

6.3.5.2 LPCPD Protocol

The SCH3221 will function properly if the LPCPD# signal goes active and then inactive again without PCI_RESET# becoming active. This is a requirement for notebook power management functions.

Although the LPC Bus spec 1.0 section 8.2 states, "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#", this statement does not apply for mobile systems. LRST# (PCI_RESET#) will not occur if the LPC Bus power was not removed. For example, when exiting a "light" sleep state (ACPI S1, APM POS), LRST# (PCI_RESET#) will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRST# (PCI_RESET#) will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus in the SCH3221. It is not used as a global powergood for the chip. It is used to reset the LPC block and hold it in reset.

An internal powergood is implemented in SCH3221 to minimize power dissipation in the entire chip.

Prior to going to a low-power state, the system will assert the LPCPD# signal. It will go active at least 30 microseconds prior to the LCLK# (PCI_CLK) signal stopping low and power being shut to the other LPC I/F signals.

Upon recognizing LPCPD# active, the SCH3221 will drive the LDRQ# signal low or tri-state, and do so until LPCPD# goes back active.

Upon recognizing LPCPD# inactive, the SCH3221 will drive its LDRQ# signal high.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

6.3.5.3 SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

The SYNC pattern is used to add wait states. For read cycles, the SCH3221 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SCH3221 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SCH3221 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SCH3221 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. The SCH3221 uses a SYNC of 0110 for all wait states in an I/O transfer. The SYNC value is driven within 3 clocks.

6.3.5.4 SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The SCH3221 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

6.3.5.5 SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The SCH3221 has protection mechanisms to complete the cycle.

6.3.5.6 SYNC Error Indication

The SCH3221 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the SCH3221, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the SCH3221. If the host was writing data to the SCH3221, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

6.3.5.7 Reset Policy

The following rules govern the reset policy:

1. When PCI_RESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2. When PCI_RESET# goes active (low):
   a) the host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
   b) the SCH3221 ignores LFRAME#, tristate the LAD[3:0] pins and drive the LDRQ# signal inactive (high).

6.3.6 LPC TRANSFERS

6.3.6.1 Wait State Requirements

I/O Transfers

For I/O transfers in which long indeterminate wait states are required (i.e., IrCC transfers) the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

Note:	Wait states are required for all I/O transfers. Three wait states are required for an I/O read and two wait states are required for an I/O write. A SYNC of 0110 is used for all I/O_transfers.

DMA Transfers

The SCH3221 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

Note 6-4 Long sync cycles are always followed by one ready sync cycle (0\H).

See the example timing for the LPC cycles in Section 10.0, "Timing Diagrams".

6.4 Serial Port (UART)

The SCH3221 incorporates four full function UARTs. They are compatible with the 16450, the 16450 ACE registers and the 16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.2 (4Mbps), HP-SIR, ASK-IR and Consumer IR infrared modes of operation.

6.4.1 REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SCH3221 contains two serial ports, each of which contain a register set as described below.

TABLE 6-4: ADDRESSING THE SERIAL PORT

DLAB*	A2	A1	A0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note 6-5 DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

6.4.1.1 Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

6.4.1.2 Transmit Buffer Register (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

6.4.1.3 Interrupt Enable Register (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH3221. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic "0".

6.4.1.4 FIFO Control Register (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16). See the Configuration section for description on these registers.

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. DMA modes are not supported in this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

6.4.1.5 Interrupt Identification Register (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

TABLE 6-5: INTERRUPT CONTROL TABLE

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register