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# LPC IO with 8042 KBC, Reset Generation, HWM and Multiple Serial Ports

## Product Features

- General Features
  - 3.3 Volt Operation (SIO Block is 5 Volt Tolerant)
  - Programmable Wake-up Event (PME) Interface
  - PC99, PC2001 Compliant
  - ACPI 2.0 Compliant
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - ISA Plug-and-Play Compatible Register Set
  - Four Address Options for Power On Configuration Port
  - System Management Interrupt (SMI)
  - General Purpose I/O pins: 23 to 40
  - GPIOs with VID compatible inputs: 0 to 6
  - Support for power button on PS/2 Keyboard
  - Security Key Register (32 byte) for Device Authentication
- Low Pin Count Bus (LPC) Interface
  - Supports Bus frequencies of 19MHz to 33MHz
- Watchdog Timer
- Resume and Main Power Good Generator
- Programmable Clock Output to 16 Hz
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
  - Phoenix Keyboard BIOS ROM
- Multiple Serial Ports
  - 4 Full Function Serial Ports (SCH3227, SCH3226, SCH3222)
  - 2 Full Function Serial Ports (SCH3224)
  - Two additional 4-pin Serial Ports available by strap option (SCH3227, SCH3226)
  - Two additional 4-pin Serial Ports available always (SCH3224, SCH3222)
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k, 460k, 921k and 1.5M Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
  - Support IRQ Sharing among serial ports
  - RS485 Auto Direction Control Mode
- Infrared Port
  - Multiprotocol Infrared Interface
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - 480 Addresses, Up to 15 IRQ
- Multi-Mode™ Parallel Port with ChiProtect™
  - Available in SCH3227, SCH3224
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional ParallelPort
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Four DMA Options
- Hardware Monitor
  - Available in SCH3227, SCH3226, SCH3224
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp (processor voltage), VCC, Vbat and Vtr.
  - Remote Thermal Diode Sensing for Two External Temperature Measurements accurate to 1.5°C
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Programmable Automatic FAN control based on temperature
  - nHWM_INT Pin for out-of-limit Temperature or Voltage Indication
  - Thermtrip signal for over temperature indication
- IDE Reset Output and 3 PCI Reset Buffers with Software Control Capability (SCH3227 and SCH3226 by strap option)
- Power Button Control and AC Power Failure Recovery (SCH3227 and SCH3226 by strap option)
- Temperature Ranges Available
  - Industrial (-40°C to +85°C)
  - Commercial (0°C to +70°C)
- WFBGA RoHS Compliant Packages
  - 144-ball (SCH3227)
  - 100-ball (SCH3226, SCH3224)
  - 84-ball (SCH3222)

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# 1.0 GENERAL DESCRIPTION

The SCH3227/SCH3226/SCH3224/SCH3222 Product Family is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. The Product Family also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

## 1.1 Scope and Definitions

For the purposes of this document, the term “SCH322x Family” refers only to the parts numbered SCH3227, SCH3226, SCH3224 and SCH3222. Similarly-numbered parts may also exist, but they are outside the scope of this document.

## 1.2 Important New Usage Considerations

The SCH322x Family is the next generation of the SCH311x family components. They mainly differ in the number of pins brought out of the package. In some cases (SCH3227, SCH3226) a new pin called STRAPOPT is brought out, allowing a hard-wired selection between the legacy SCH3114 vs. SCH3116 features of 8 of the pins. This selection also affects the Device ID register, which will display the legacy SCH3114 or SCH3116 code. Other SCH322x members, which do not have a STRAPOPT pin, are hard-wired internally to identify themselves as the legacy SCH3116.

**CAUTION:** This device contains circuits and registers affecting pin functions which must not be used when they are not brought out of the package. These pins are pulled to known states internally. Any features, especially Logical Devices and GPIOs, that are not listed in this document for a particular family member must not be activated, accessed, or in any way changed from its default reset state. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system. See Table 2-1 SCH3227, Table 2-2 SCH3226, Table 2-3 SCH3224, or Table 2-4 SCH3222, for the pin features that are brought out.

## 1.3 Feature Sets

See Table 1-1 on page 5 for features available per family member.

The Product Family is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard.

The Product Family supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, hardware IRQ and DMA Channel of each Logical Device may be reprogrammed through the internal configuration registers. There are up to 480 I/O address location options (960 for the Parallel Port), a Serialized IRQ interface, and a choice of three Legacy DMA channel assignments.

Super I/O functionality includes an 8042 based keyboard and mouse controller, one IrDA 1.0 infrared port and multiple serial ports. Some family members (Table 1-1) also provide an IEEE 1284 EPP/ECP compatible parallel port.

The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 1.5 Mbps. There are both 8-pin Serial Ports and 4-pin Serial Ports. The reduced-pin serial ports have selectable input and output controls. The Serial Ports contain programmable direction control, which will automatically drive nRTS when the Output Buffer is loaded, then drive nRTS when the Output Buffer is empty.

Hardware Monitoring capability has programmable, automatic fan control. Three fan tachometer inputs and three pulse width modulator (PWM) fan control outputs are available.

Hardware Monitoring capability also includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans in response. There are four analog inputs for monitoring external voltages of +5V, +2.5V, +12V and Vccp (core processor voltage), as well as internal monitoring of the device’s internal VCC, VTR, and VBAT power supplies. Hardware Monitoring includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring local ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and fan speed conditions. Hardware Monitoring features are accessible via the LPC bus, and the same interrupt event reported on the nHWM_INT pin also creates PME wakeup events. A separate THERMTRIP output is available, which generates a pulse output on a programmed over-temperature condition. This can be used to generate a reset or shutdown indication to the system.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, a programmable Clock output, and reset generation. The reset generation includes a watchdog timer which can be used to generate a reset pulse. The width of this pulse is selectable via an external strapping option.

System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, and control of two LED's.

**TABLE 1-1: DEVICE SPECIFIC SUMMARY**

| Function | SCH3227 | SCH3226 | SCH3224 | SCH3222 |
|---|---|---|---|---|
| **LPC Bus Interface** | YES | YES | YES | YES |
| **PnP Config w/ 4 Port Addresses** | YES | YES | YES | YES |
| **Serial IRQ and SMI** | YES | YES | YES | YES |
| **Keyboard Controller** | YES | YES | YES | YES |
| **Watchdog Timer** | YES | YES | YES | YES |
| **Parallel Port** | YES | NO | YES | NO |
| **Reset Generator** | YES | YES | YES | YES |
| **Serial Ports, Full** | 4 | 4 | 2 | 4 |
| **Additional Serial Ports, 4-Pin** | 2 avail. (by strap option) | 2 avail. (by strap option) | 2 | 2 |
| **Infrared Port** | YES | YES | YES | YES |
| **Programmable Clock Output** | YES | YES | YES | YES |
| **IDE / PCI Reset Outputs** | By strap option (vs. 4-pin Serial Ports). | By strap option (vs. 4-pin Serial Ports). | NO | NO |
| **Power Button / AC Fail Support** | By strap option (vs. 4-pin Serial Ports). | By strap option (vs. 4-pin Serial Ports). | NO | NO |
| **GPIOs** | 40 | 40 | 24 | 23 |
| **GPIO with VID Compatible Inputs** | 6 | 6 | 0 | 6 |
| **Hardware Monitor** | YES | YES | YES | NO |
| **WFBGA Package** | 144-ball | 100-ball | 100-ball | 84-ball |

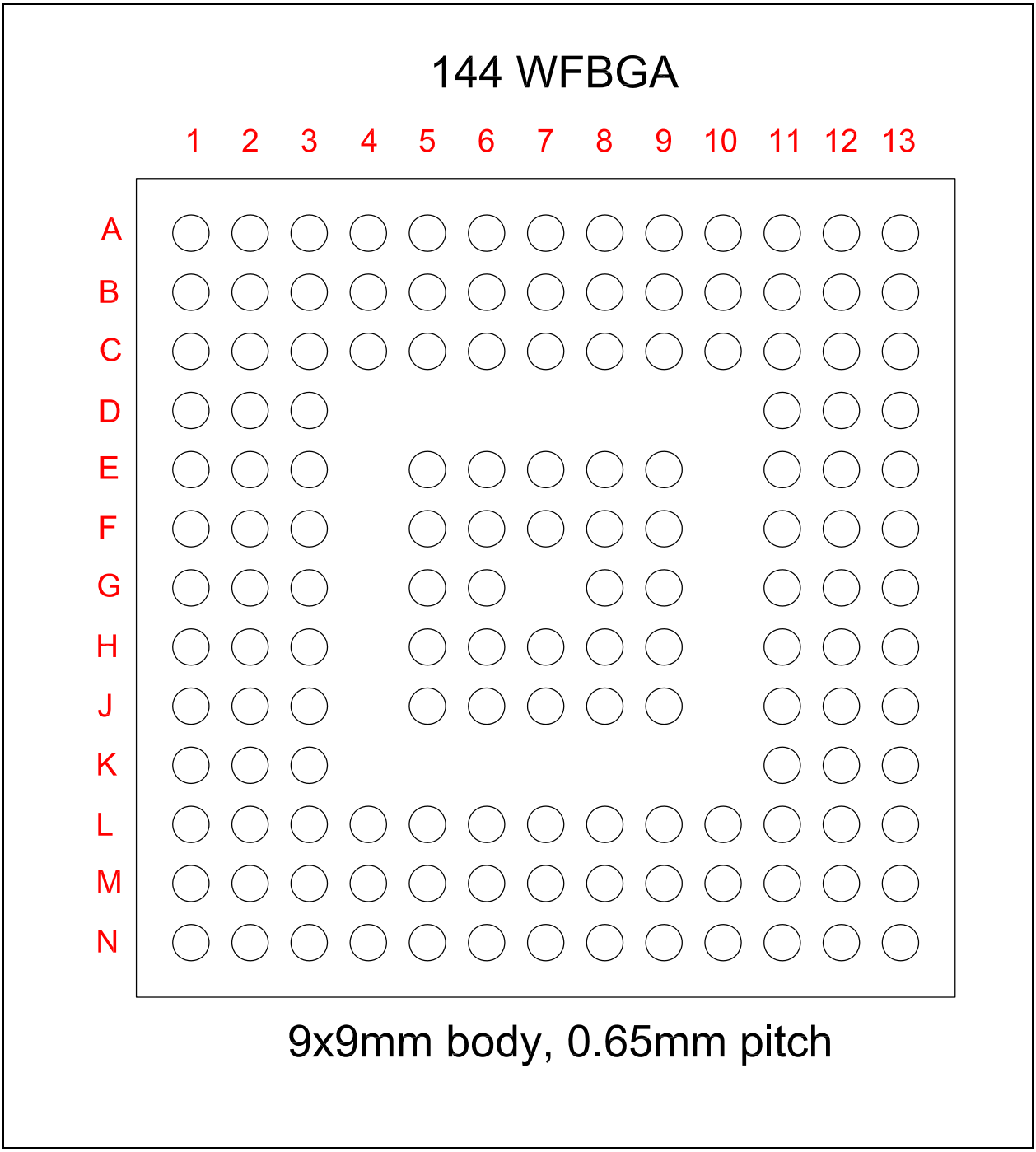
## 1.4 Reference Documents

1. Intel Low Pin Count Specification, Revision 1.0, September 29, 1997
2. PCI Local Bus Specification, Revision 2.2, December 18, 1998
3. Advanced Configuration and Power Interface Specification, Revision 1.0b, February 2, 1999
4. IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993
5. Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook
6. Application Note (AN 8-8) “Keyboard and Mouse Wakeup Functionality”, dated 03/23/02

## 2.0 PIN LAYOUTS

### 2.1 SCH322x Pin Layout Summary

**FIGURE 2-1: SCH3227 PIN DIAGRAM**



Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

**TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| K13 | STRAPOPT (=VTR[a]) | STRAPOPT (=VSS[a]) |
| M4 | RESERVED=VTR[b] | RESERVED=VTR[b] |
| C3 | +12V_IN | +12V_IN |
| D3 | +5V_IN | +5V_IN |
| E6 | GP40 | GP40 |
| E3 | VTR | VTR |
| E5 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| F8 | TEST=VSS[c] | TEST=VSS[c] |
| F7 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| F3 | VSS | VSS |
| F6 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| F5 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| G8 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| G6 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| H8 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| G5 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| H7 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| H6 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| H5 | RESERVED=VSS[c] | RESERVED=VSS[c] |
| D2 | CLOCKI | CLOCKI |
| E2 | LAD0 | LAD0 |
| D1 | LAD1 | LAD1 |
| E1 | LAD2 | LAD2 |
| F2 | LAD3 | LAD3 |
| F1 | LFRAME# | LFRAME# |
| G2 | LDRQ# | LDRQ# |
| H1 | PCI_RESET# | PCI_RESET# |
| G1 | PCI_CLK | PCI_CLK |
| H2 | SER_IRQ | SER_IRQ |
| H3 | VSS | VSS |
| J3 | VCC | VCC |
| J1 | GP44 / TXD6 | nIDE_RSTDRV / GP44 |
| J2 | GP45 / RXD6 | nPCIRST1 / GP45 |
| K3 | GP46 / nSCIN6 | nPCIRST2 / GP46 |
| L3 | GP47 / nSCOUT6 | nPCIRST3 / GP47 |
| K1 | AVSS | AVSS |
| L1 | VBAT | VBAT |
| K2 | GP27 / nIO_SMI / P17 | GP27 / nIO_SMI / P17 |
| L2 | KDAT / GP21 | KDAT / GP21 |
| M1 | KCLK / GP22 | KCLK / GP22 |
| M2 | MDAT / GP32 | MDAT / GP32 |
| N1 | MCLK / GP33 | MCLK / GP33 |
| M3 | GP36 / nKBDRST | GP36 / nKBDRST |

**TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| N2 | GP37 / A20M | GP37 / A20M |
| L5 | VSS | VSS |
| N3 | VTR | VTR |
| N4 | nINIT | nINIT |
| M5 | nSLCTIN | nSLCTIN |
| L6 | PD0 | PD0 |
| N5 | PD1 | PD1 |
| M6 | PD2 | PD2 |
| L7 | PD3 | PD3 |
| N6 | PD4 | PD4 |
| M7 | PD5 | PD5 |
| N7 | PD6 | PD6 |
| L8 | PD7 | PD7 |
| L9 | VSS | VSS |
| M8 | SLCT | SLCT |
| N8 | PE | PE |
| N9 | BUSY | BUSY |
| M9 | nACK | nACK |
| N10 | nERROR | nERROR |
| M10 | nALF | nALF |
| N11 | nSTROBE | nSTROBE |
| M11 | nRI1 | nRI1 |
| N12 | nDCD1 | nDCD1 |
| L11 | RXD1 | RXD1 |
| M12 | TXD1 / SIOXNOROUT | TXD1 / SIOXNOROUT |
| N13 | nDSR1 | nDSR1 |
| L12 | nRTS1 / SYSOPT0 | nRTS1 / SYSOPT0 |
| M13 | nCTS1 | nCTS1 |
| J12 | nDTR1 / SYSOPT1 | nDTR1 / SYSOPT1 |
| K12 | GP50 / nRI2 | GP50 / nRI2 |
| L13 | VTR | VTR |
| J13 | VSS | VSS |
| H11 | GP51 / nDCD2 | GP51 / nDCD2 |
| H12 | GP52 / RXD2(IRRX2) | GP52 / RXD2(IRRX2) |
| H13 | GP53 / TXD2(IRTX2) | GP53 / TXD2(IRTX2) |
| G13 | GP54 / nDSR2 | GP54 / nDSR2 |
| G12 | GP55 / nRTS2 / RESGEN | GP55 / nRTS2 / RESGEN |
| G11 | GP56 / nCTS2 | GP56 / nCTS2 |
| F13 | GP57 / nDTR2 | GP57 / nDTR2 |
| F12 | RXD5 | PB_OUT# |
| F11 | TXD5 | PS_ON# |
| E13 | nSCOUT5 | PB_IN# |
| E12 | nSCIN5 | SLP_SX# |
| D13 | GP10 / RXD3 | GP10 / RXD3 |

**TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| D12 | GP11 / TXD3 | GP11 / TXD3 |
| E11 | GP14 / nDSR3 | GP14 / nDSR3 |
| C13 | GP17 / nRTS3 | GP17 / nRTS3 |
| B13 | GP16 / nCTS3 | GP16 / nCTS3 |
| C12 | GP42 / nIO_PME | GP42 / nIO_PME |
| D11 | VTR | VTR |
| A13 | GP15 / nDTR3 | GP15 / nDTR3 |
| B12 | GP61 / nLED2 / CLKO | GP61 / nLED2 / CLKO |
| C11 | GP60 / nLED1 / WDT | GP60 / nLED1 / WDT |
| A12 | GP13 / nRI3 | GP13 / nRI3 |
| B11 | GP12 / nDCD3 | GP12 / nDCD3 |
| A11 | GP31 / nRI4 | GP31 / nRI4 |
| C10 | GP63 / nDCD4 | GP63 / nDCD4 |
| B10 | CLKI32 | CLKI32 |
| A10 | nRSMRST | nRSMRST |
| B9 | VSS | VSS |
| C9 | GP64 / RXD4 | GP64 / RXD4 |
| A9 | GP65 / TXD4 | GP65 / TXD4 |
| A8 | GP66 / nDSR4 | GP66 / nDSR4 |
| B8 | GP67 / nRTS4 | GP67 / nRTS4 |
| C8 | GP62 / nCTS4 | GP62 / nCTS4 |
| A7 | GP34 / nDTR4 | GP34 / nDTR4 |
| B7 | PWRGD_OUT | PWRGD_OUT |
| A6 | PWRGD_PS | PWRGD_PS |
| C7 | nFPRST / GP30 | nFPRST / GP30 |
| E8 | VTR | VTR |
| E7 | VSS | VSS |
| B6 | nTHERMTRIP | nTHERMTRIP |
| A5 | nHWM_INT | nHWM_INT |
| C6 | PWM3 | PWM3 |
| B5 | PWM2 | PWM2 |
| A4 | PWM1 | PWM1 |
| B4 | FANTACH3 | FANTACH3 |
| C5 | FANTACH2 | FANTACH2 |
| C4 | FANTACH1 | FANTACH1 |
| A3 | HVSS | HVSS |
| B3 | HVTR | HVTR |
| A2 | REMOTE2- | REMOTE2- |
| A1 | REMOTE2+ | REMOTE2+ |
| B1 | REMOTE1- | REMOTE1- |
| C1 | REMOTE1+ | REMOTE1+ |
| C2 | VCCP_IN | VCCP_IN |

**TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| B2 | +2.5V_IN | +2.5V_IN |
| -- | RESERVED=N/C[d]: E9, F9, G9, H9, J5, J6, J7, J8, J9, G3, J11, K11, L4, L10 | |

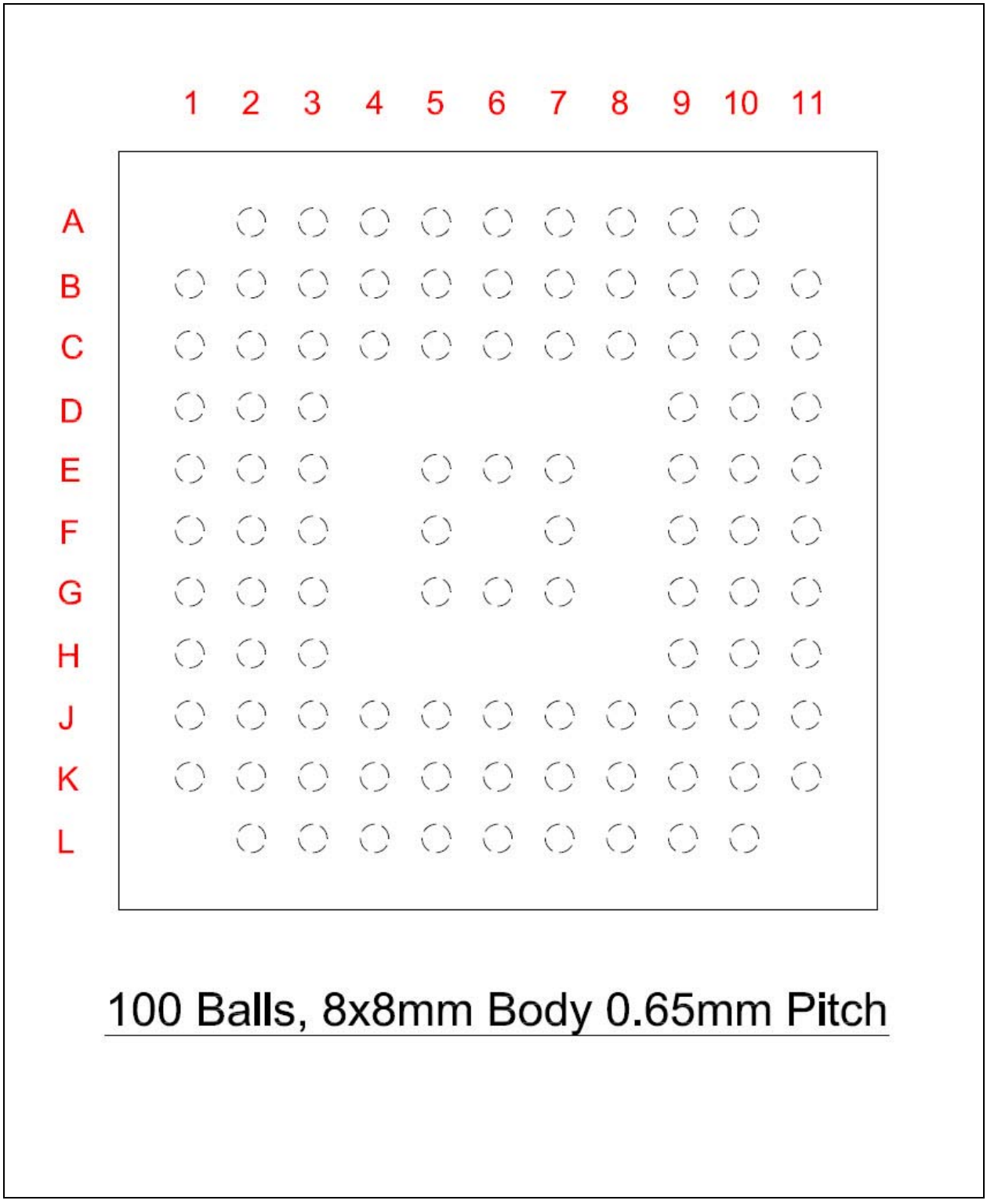
a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
When connected to VTR, the table column STRAPOPT=1 applies,
and Device ID = 0x7F.
When connected to VSS, the table column STRAPOPT=0 applies,
and Device ID = 0x7D.

b. For correct operation, this lead must always be connected to VTR.

c. For correct operation and minimal current consumption, this lead must always be connected to VSS.

d. Make No Connection to these leads.

**FIGURE 2-2: SCH3226 PIN DIAGRAM**



Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

**TABLE 2-2: SCH3226 SUMMARIES BY STRAP OPTION**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| L8 | STRAPOPT (=VTR[a]) | STRAPOPT (=VSS[a]) |
| C2 | +12V_IN | +12V_IN |
| C1 | +5V_IN | +5V_IN |
| C3 | GP40 / DRVDEN0(out) | GP40 / DRVDEN0(out) |
| D3 | VTR | VTR |
| G5 | TEST=VSS[b] | TEST=VSS[b] |
| D2 | VSS | VSS |
| E3 | CLOCKI | CLOCKI |
| F3 | LAD0 | LAD0 |
| E2 | LAD1 | LAD1 |
| D1 | LAD2 | LAD2 |
| F2 | LAD3 | LAD3 |
| E1 | LFRAME# | LFRAME# |
| G3 | LDRQ# | LDRQ# |
| F1 | PCI_RESET# | PCI_RESET# |
| G1 | PCI_CLK | PCI_CLK |
| G2 | SER_IRQ | SER_IRQ |
| H1 | VSS | VSS |
| H2 | VCC | VCC |
| H3 | GP44 / TXD6 | nIDE_RSTDRV / GP44 |
| J2 | GP45 / RXD6 | nPCIRST1 / GP45 |
| K2 | GP46 / nSCIN6 | nPCIRST2 / GP46 |
| J3 | GP47 / nSCOUT6 | nPCIRST3 / GP47 |
| J1 | AVSS | AVSS |
| K1 | VBAT | VBAT |
| K3 | GP27 / nIO_SMI / P17 | GP27 / nIO_SMI / P17 |
| J4 | KDAT / GP21 | KDAT / GP21 |
| L2 | KCLK / GP22 | KCLK / GP22 |
| L3 | MDAT / GP32 | MDAT / GP32 |
| K4 | MCLK / GP33 | MCLK / GP33 |
| L4 | GP36 / nKBDRST | GP36 / nKBDRST |
| L5 | GP37 / A20M | GP37 / A20M |
| G7 | VSS | VSS |
| G6 | VTR | VTR |
| K7 | nRI1 | nRI1 |
| L6 | nDCD1 | nDCD1 |
| K8 | RXD1 | RXD1 |
| J8 | TXD1 / SIOXNOROUT | TXD1 / SIOXNOROUT |
| K6 | nDSR1 | nDSR1 |
| K5 | nRTS1 / SYSOPT0 | nRTS1 / SYSOPT0 |
| J7 | nCTS1 | nCTS1 |
| J6 | nDTR1 / SYSOPT1 | nDTR1 / SYSOPT1 |
| J5 | GP50 / nRI2 | GP50 / nRI2 |

**TABLE 2-2: SCH3226 SUMMARIES BY STRAP OPTION (CONTINUED)**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| L9 | VTR | VTR |
| L7 | VSS | VSS |
| K9 | GP51 / nDCD2 | GP51 / nDCD2 |
| J9 | GP52 / RXD2(IRRX2) | GP52 / RXD2(IRRX2) |
| H9 | GP53 / TXD2(IRTX2) | GP53 / TXD2(IRTX2) |
| G9 | GP54 / nDSR2 | GP54 / nDSR2 |
| L10 | GP55 / nRTS2 / RESGEN | GP55 / nRTS2 / RESGEN |
| K10 | GP56 / nCTS2 | GP56 / nCTS2 |
| J10 | GP57 / nDTR2 | GP57 / nDTR2 |
| H10 | RXD5 | PB_OUT# |
| K11 | TXD5 | PS_ON# |
| J11 | nSCOUT5 | PB_IN# |
| H11 | nSCIN5 | SLP_SX# |
| F9 | GP10 / RXD3 | GP10 / RXD3 |
| G10 | GP11 / TXD3 | GP11 / TXD3 |
| E9 | GP14 / nDSR3 | GP14 / nDSR3 |
| F10 | GP17 / nRTS3 | GP17 / nRTS3 |
| G11 | GP16 / nCTS3 | GP16 / nCTS3 |
| F11 | GP42 / nIO_PME | GP42 / nIO_PME |
| E10 | VTR | VTR |
| E11 | GP15 / nDTR3 | GP15 / nDTR3 |
| D9 | GP61 / nLED2 / CLKO | GP61 / nLED2 / CLKO |
| D10 | GP60 / nLED1 / WDT | GP60 / nLED1 / WDT |
| D11 | GP13 / nRI3 | GP13 / nRI3 |
| C11 | GP12 / nDCD3 | GP12 / nDCD3 |
| C10 | GP31 / nRI4 | GP31 / nRI4 |
| C9 | GP63 / nDCD4 | GP63 / nDCD4 |
| B11 | CLKI32 | CLKI32 |
| B10 | nRSMRST | nRSMRST |
| A10 | VSS | VSS |
| C8 | GP64 / RXD4 | GP64 / RXD4 |
| B9 | GP65 / TXD4 | GP65 / TXD4 |
| A9 | GP66 / nDSR4 | GP66 / nDSR4 |
| B8 | GP67 / nRTS4 | GP67 / nRTS4 |
| A8 | GP62 / nCTS4 | GP62 / nCTS4 |
| C7 | GP34 / nDTR4 | GP34 / nDTR4 |
| A7 | PWRGD_OUT | PWRGD_OUT |
| B7 | PWRGD_PS | PWRGD_PS |
| E7 | nFPRST / GP30 | nFPRST / GP30 |
| F7 | VTR | VTR |
| C6 | VSS | VSS |
| B6 | nTHERMTRIP | nTHERMTRIP |
| E6 | nHWM_INT | nHWM_INT |
| A6 | PWM3 | PWM3 |

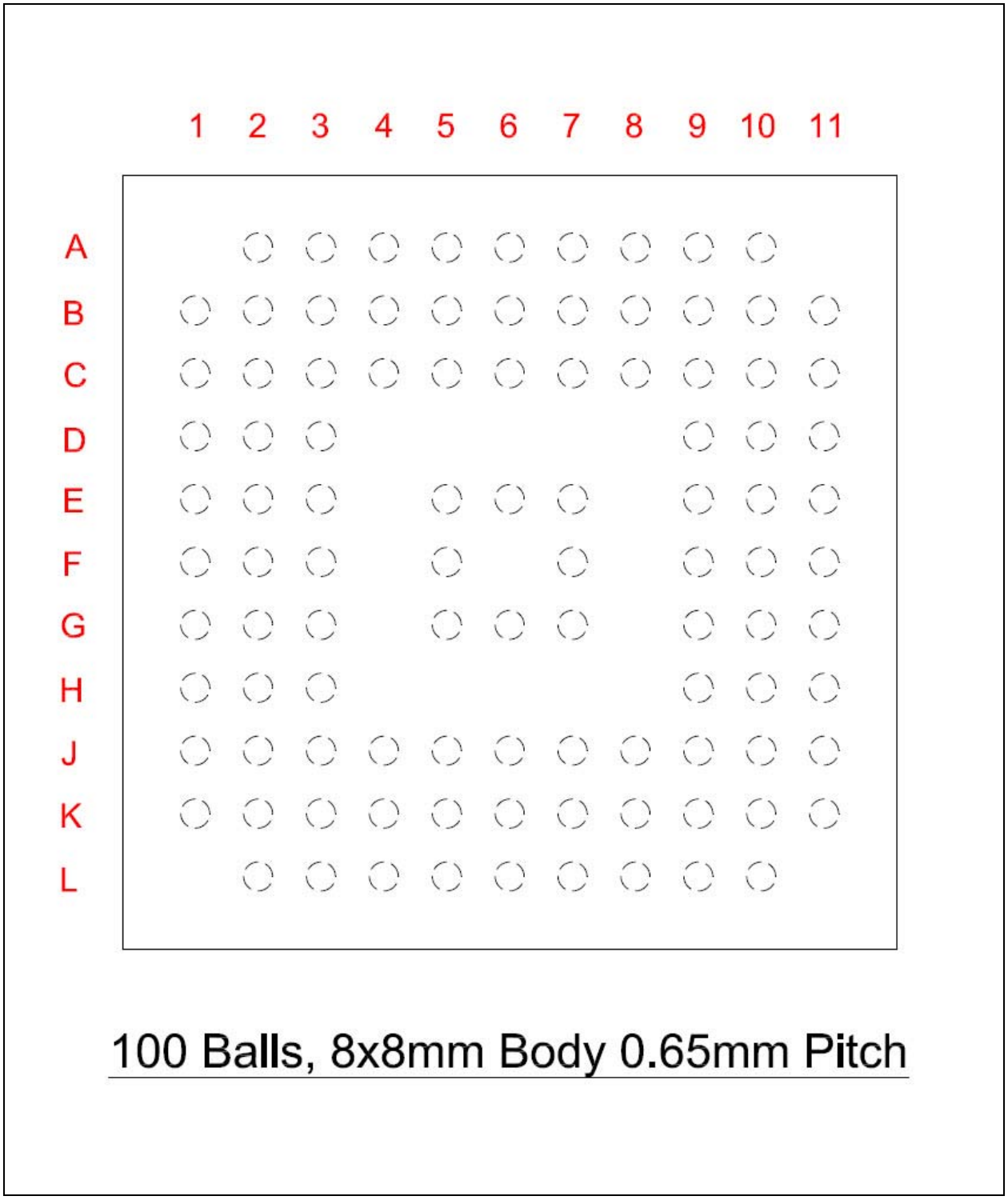
**TABLE 2-2: SCH3226 SUMMARIES BY STRAP OPTION (CONTINUED)**

| Ball# | Function: StrapOPT=1 | Function: StrapOPT=0 |
|---|---|---|
| F5 | PWM2 | PWM2 |
| A5 | PWM1 | PWM1 |
| E5 | FANTACH3 | FANTACH3 |
| B5 | FANTACH2 | FANTACH2 |
| C5 | FANTACH1 | FANTACH1 |
| B4 | HVSS | HVSS |
| C4 | HVTR | HVTR |
| A4 | REMOTE2- | REMOTE2- |
| A3 | REMOTE2+ | REMOTE2+ |
| A2 | REMOTE1- | REMOTE1- |
| B1 | REMOTE1+ | REMOTE1+ |
| B3 | VCCP_IN | VCCP_IN |
| B2 | +2.5V_IN | +2.5V_IN |

a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
When connected to VTR, the table column STRAPOPT=1 applies,
and Device ID = 0x7F.
When connected to VSS, the table column STRAPOPT=0 applies,
and Device ID = 0x7D.

b. For correct operation, this lead must always be connected to VSS.

**FIGURE 2-3: SCH3224 PIN DIAGRAM**



Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

**TABLE 2-3: SCH3224 SUMMARY**

| Ball# | Function[a] |
|---|---|
| C3 | +12V_IN |
| C2 | +5V_IN |
| D3 | VTR |
| E6 | TEST=VSS[b] |
| D2 | VSS |
| F2 | CLOCKI |
| E2 | LAD0 |
| D1 | LAD1 |
| E3 | LAD2 |
| F3 | LAD3 |
| E1 | LFRAME# |
| G3 | LDRQ# |
| F1 | PCI_RESET# |
| G1 | PCI_CLK |
| G2 | SER_IRQ |
| H1 | VSS |
| H2 | VCC |
| H3 | GP44 / TXD6 |
| F5 | GP45 / RXD6 |
| E5 | GP46 / nSCIN6 |
| J2 | GP47 / nSCOUT6 |
| J1 | AVSS |
| K1 | VBAT |
| J3 | GP27 / nIO_SMI / P17 |
| J4 | KDAT / GP21 |
| K3 | KCLK / GP22 |
| K2 | MDAT / GP32 |
| L2 | MCLK / GP33 |
| L3 | GP36 / nKBDRST |
| J5 | GP37 / A20M |
| K4 | RESERVED=N/C (Make no connection.) |
| G6 | VTR |
| K5 | nINIT |
| G5 | nSLCTIN |
| J6 | PD0 |
| L5 | PD1 |
| K6 | PD2 |
| L4 | PD3 |
| L6 | PD4 |
| C10 | PD5 |
| K7 | PD6 |
| J7 | PD7 |
| G7 | VSS |

**TABLE 2-3: SCH3224 SUMMARY (CONTINUED)**

| Ball# | Function[a] |
|---|---|
| C7 | SLCT |
| E7 | PE |
| L8 | BUSY |
| K8 | nACK |
| J8 | nERROR |
| G11 | nALF |
| K9 | nSTROBE |
| L10 | nRI1 |
| J9 | nDCD1 |
| K10 | RXD1 |
| K11 | TXD1 / SIOXNOROUT |
| J10 | nDSR1 |
| J11 | nRTS1 / SYSOPT0 |
| H9 | nCTS1 |
| H10 | nDTR1 / SYSOPT1 |
| H11 | GP50 / nRI2 |
| L9 | VTR |
| L7 | VSS |
| G9 | GP51 / nDCD2 |
| G10 | GP52 / RXD2(IRRX2) |
| F11 | GP53 / TXD2(IRTX2) |
| F10 | GP54 / nDSR2 |
| E11 | GP55 / nRTS2 / RESGEN |
| D11 | GP56 / nCTS2 |
| F9 | GP57 / nDTR2 |
| D10 | RXD5 |
| B11 | TXD5 |
| E9 | nSCOUT5 |
| D9 | nSCIN5 |
| C11 | GP42 / nIO_PME |
| E10 | VTR |
| B10 | GP61 / nLED2 / CLKO |
| C9 | GP60 / nLED1 / WDT |
| C1 | CLKI32 |
| B9 | nRSMRST |
| A10 | VSS |
| C8 | PWRGD_OUT |
| A9 | PWRGD_PS |
| B8 | nFPRST / GP30 |
| F7 | VTR |
| C6 | VSS |
| B7 | nTHERMTRIP |
| A8 | nHWM_INT |
| A7 | PWM3 |

**TABLE 2-3: SCH3224 SUMMARY (CONTINUED)**

| Ball# | Function[a] |
|---|---|
| B6 | PWM2 |
| A6 | PWM1 |
| A5 | FANTACH3 |
| B5 | FANTACH2 |
| C5 | FANTACH1 |
| B4 | HVSS |
| C4 | HVTR |
| A4 | REMOTE2- |
| A3 | REMOTE2+ |
| A2 | REMOTE1- |
| B1 | REMOTE1+ |
| B3 | VCCP_IN |
| B2 | +2.5V_IN |

a. Device ID register at Plug&Play Index 0x20 holds 0x7F.

b. For correct operation, this lead must always be connected to VSS.

**FIGURE 2-4: SCH3222 PIN DIAGRAM**

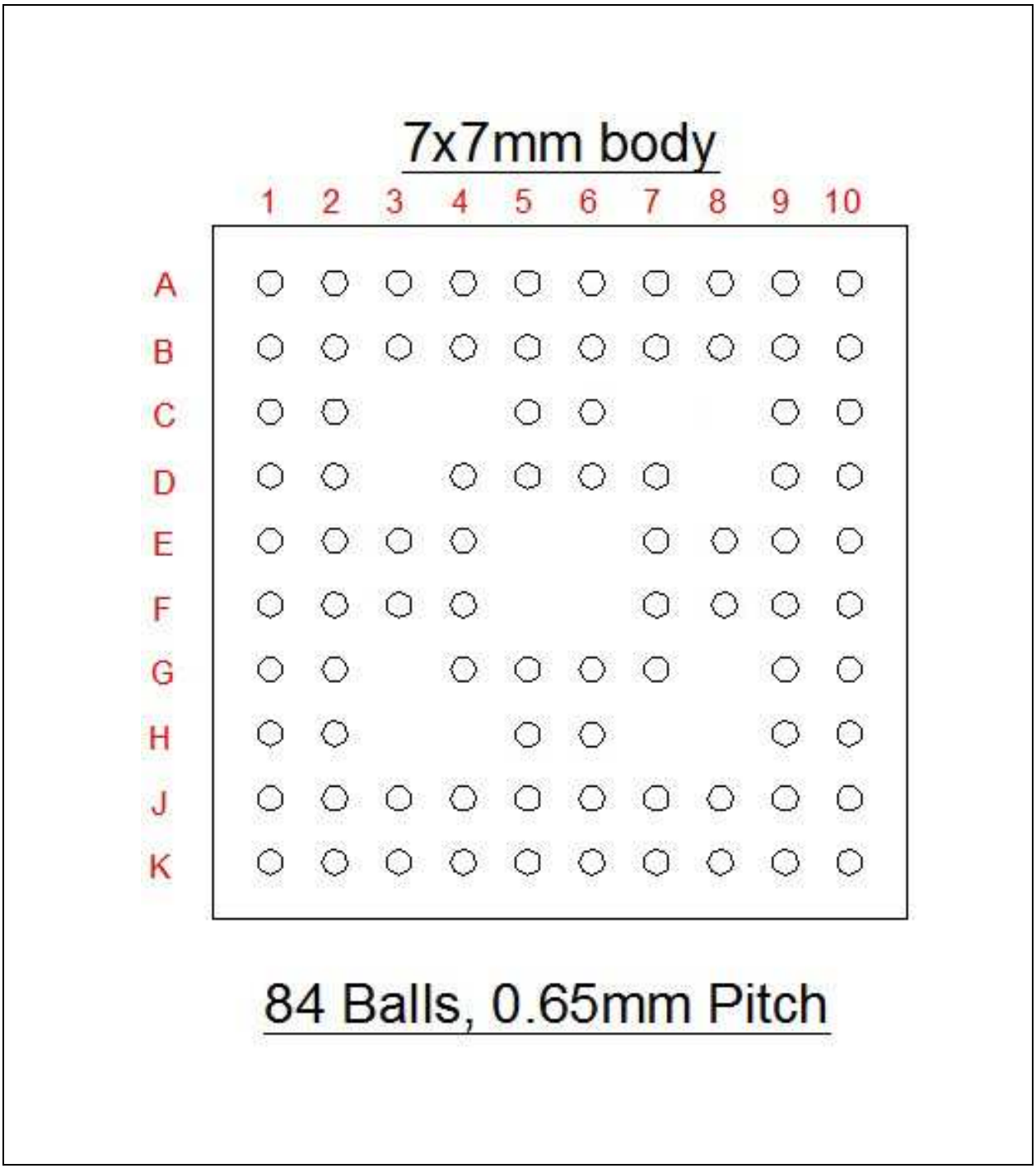


**TABLE 2-4: SCH3222 SUMMARY**

| BALL# | FUNCTION[a] |
|---|---|
| B1 | +5V_IN |
| A1 | GP40 |
| C1 | VTR |
| A2 | TEST=VSS[b] |
| D1 | VSS |
| E1 | CLOCKI |
| B2 | LAD0 |
| C2 | LAD1 |
| B3 | LAD2 |
| D2 | LAD3 |
| F1 | LFRAME# |
| F2 | PCI_RESET# |
| F3 | PCI_CLK |
| E3 | SER_IRQ |
| G2 | VSS |
| G1 | VCC |
| H1 | GP44 / TXD6 |
| J1 | GP45 / RXD6 |
| J2 | GP46 / nSCIN6 |
| K1 | GP47 / nSCOUT6 |
| K2 | AVSS |
| H2 | VBAT |
| K3 | GP27 / nIO_SMI / P17 |
| J3 | KDAT / GP21 |
| J4 | KCLK / GP22 |
| F4 | MDAT / GP32 |
| E4 | MCLK / GP33 |
| J5 | GP36 / nKBDRST |
| K4 | GP37 / A20M |
| K6 | VSS |
| K5 | VTR |
| K7 | VSS |
| K8 | nRI1 |
| H5 | nDCD1 |
| K10 | RXD1 |
| J10 | TXD1 / SIOXNOROUT |
| K9 | nDSR1 |
| J9 | nRTS1 / SYSOPT0 |
| H10 | nCTS1 |
| H9 | nDTR1 / SYSOPT1 |
| J8 | GP50 / nRI2 |
| G9 | VTR |
| J7 | VSS |
| G5 | GP51 / nDCD2 |

**TABLE 2-4: SCH3222 SUMMARY (CONTINUED)**

| BALL# | FUNCTION[a] |
|---|---|
| G10 | GP52 / RXD2(IRRX2) |
| F10 | GP53 / TXD2(IRTX2) |
| G7 | GP54 / nDSR2 |
| J6 | GP55 / nRTS2 / RESGEN |
| H6 | GP56 / nCTS2 |
| F9 | GP57 / nDTR2 |
| F8 | RXD5 |
| F7 | TXD5 |
| G6 | nSCOUT5 |
| E9 | nSCIN5 |
| E10 | GP10 / RXD3 |
| D10 | GP11 / TXD3 |
| G4 | GP14 / nDSR3 |
| E8 | GP17 / nRTS3 |
| E7 | GP16 / nCTS3 |
| D7 | GP42 / nIO_PME |
| D4 | VTR |
| C10 | GP15 / nDTR3 |
| D9 | GP61 / nLED2 / CLKO |
| C9 | GP60 / nLED1 / WDT |
| B9 | GP13 / nRI3 |
| B10 | GP12 / nDCD3 |
| A10 | GP31 / nRI4 |
| A9 | GP63 / nDCD4 |
| D6 | CLKI32 |
| B8 | nRSMRST |
| A4 | VSS |
| A8 | GP64 / RXD4 |
| A7 | GP65 / TXD4 |
| C6 | GP66 / nDSR4 |
| B7 | GP67 / nRTS4 |
| C5 | GP62 / nCTS4 |
| B6 | GP34 / nDTR4 |
| B5 | PWRGD_OUT |
| B4 | PWRGD_PS |
| A6 | nFPRST / GP30 |
| A3 | VTR |
| D5 | VSS |
| A5 | VSS |
| E2 | VSS |

a. Device ID register at Plug&Play Index 0x20 holds 0x7F.

b. For correct operation, this lead must always be connected to VSS.

## 2.2 Pin Functions

Table 2-5 lists all possible SCH322x pin functions. See Table 2-1 through Table 2-4 for the pins that apply to specific family members.

These functions are all available only on the SCH3227 device, and then certain functions require specific setting of the STRAPOPT pin, which is new to the SCH322x family. The STRAPOPT pin appears in the SCH3227 (Table 2-1) and SCH3226 (Table 2-2) family members only.

**TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION**

| Note | Name | Description | VCC Power Plane | VTR-POWER Plane | VCC=0 Operation (Note 2-14) | Buffer Modes (Note 2-1) |
|---|---|---|---|---|---|---|
| **PACKAGE PINOUT STRAP OPTION PIN (SCH3227 AND SCH3226 ONLY)** | | | | | | |
| | STRAPOPT | Pinout Strap Option | | STRAPOPT | No Gate | I |
| **POWER PINS** | | | | | | |
| 2-3, 2-4 | VCC | +3.3 Volt Supply Voltage | | | | |
| 2-3, 2-4 | VTR | +3.3 Volt Standby Supply Voltage | | | | |
| 2-8 | VBAT | +3.0 Volt Battery Supply) | | | | |
| | VSS | Ground | | | | |
| | AVSS | Analog Ground | | | | |
| 2-3 | HVTR | Analog Power. +3.3V VTR pin dedicated to the Hardware Monitoring block. HVTR is powered by +3.3V Standby power VTR. | | | | |
| 2-3 | HVSS | Analog Ground. Internally connected to all of the Hardware Monitoring Block circuitry. | | | | |
| **CLOCK PINS** | | | | | | |
| | CLKI32 | 32.768kHz Trickle Clock Input | | CLKI32 | No Gate | IS |
| | CLOCKI | 14.318MHz Clock Input | CLOCKI | | | IS |
| **LPC INTERFACE** | | | | | | |
| | LAD[3:0] | Multiplexed Command Address and Data | LAD[3:0] | | GATE/ Hi-Z | PCI_IO |
| | LFRAME# | Frame signal. Indicates start of new cycle and termination of broken cycle | LFRAME# | | GATE | PCI_I |
| | LDRQ# | Encoded DMA Request | LDRQ# | | GATE/Hi-Z | PCI_O |
| | PCI_RESET# | PCI Reset | PCI_RESET# | | NO GATE | PCI_I |
| | PCI_CLK | PCI Clock | PCI_CLK | | GATE | PCI_ICLK |
| | SER_IRQ | Serial IRQ | SER_IRQ | | GATE / Hi-Z | PCI_IO |
| **SERIAL PORT 1 INTERFACE** | | | | | | |
| | RXD1 | Receive Data 1 | RXD1 | | GATE | IS |
| | TXD1 /SIO XNOR_OUT | Transmit Data 1 / XNOR-Chain test mode Output for SIO block | TXD1 /SIO XNOR_OUT | | HI-Z | O12/O12 |
| | nDSR1 | Data Set Ready 1 | nDSR1 | | GATE | I |

**TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)**

| Note | Name | Description | VCC Power Plane | VTR-POWER Plane | VCC=0 Operation (Note 2-14) | Buffer Modes (Note 2-1) |
|---|---|---|---|---|---|---|
| 2-7 | nRTS1/ SYSOPT0 | Request to Send 1/ SYSOPT (Configuration Port Base Address Control) | nRTS1/ SYSOPT0 | | GATE/ Hi-Z | OP14 / I |
| | nCTS1 | Clear to Send 1 | nCTS1 | | GATE | I |
| | nDTR1 / SYSOPT1 | Data Terminal Ready 1 | nDTR1 / SYSOPT1 | | GATE/ Hi-Z | O6 / I |
| 2-9 | nRI1 | Ring Indicator 1 | | nRI1 | GATE | IS |
| | nDCD1 | Data Carrier Detect 1 | nDCD1 | | GATE | I |
| **SERIAL PORT 2 INTERFACE** | | | | | | |
| 2-9 | GP50 / nRI2 | Ring Indicator 2 | GP50 | nRI2 | NO GATE/ HI-Z | (I/OD8/OD8) / IS |
| 2-9 | GP51 / nDCD2 | Data Carrier Detect 2 | GP51 / nDCD2 | | NO GATE/ HI-Z | (I/OD8/OD8) / I |
| 2-9 | GP52 / RXD2 (IRRX2) | Receive Data 2 (IRRX2) | GP52 / RXD2 (IRRX2) | | NO GATE/ HI-Z | (I/OD8OD8) / IS |
| 2-11, 2-9 | GP53 / TXD2 (IRTX2) | Transmit Data 2 (IRTX2) | GP53 / TXD2 (IRTX2) | | NO GATE/ HI-Z | (I/O12/OD12) / (O12/OD12) / (O12/OD12) |
| 2-9 | GP54 / nDSR2 | Data Set Ready 2 | GP54 / nDSR2 | | NO GATE/ HI-Z | (I/OD8/OD8) / I |
| 2-9 2-15 | GP55 / nRTS2 / RESGEN | Request to Send 2 / Reset Generator Pulse Width Strap Option | GP55 / nRTS2 / RESGEN | | NO GATE/ HI-Z | (I/O8/OD8) / I / IOP8 |
| 2-9 | GP56 / nCTS2 | Clear to Send 2 | GP56 / nCTS2 | | NO GATE/ HI-Z | (I/OD8OD8) / I |
| 2-9 | GP57 / nDTR2 | Data Terminal Ready 2 | GP57 / nDTR2 | | NO GATE/ HI-Z | (I/OD8OD8) / O6 |
| **SERIAL PORT 3 INTERFACE** | | | | | | |
| 2-9 | GP13 / nRI3 | GPIO / Ring Indicator 3 | | GP13 / nRI3 | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP12 / nDCD3 | GPIO / Data Carrier Detect 3 | nDCD3 | GP12 | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP10 / RXD3 | GPIO / Receive Data 3 | GP10 / RXD3 | | / HI-Z | (IS/O8/OD8) / IS |
| 2-11, 2-9 | GP11 / TXD3 | GPIO / Transmit Data 3 | TXD3 | GP11 | / HI-Z | (I/O8/OD8) / O8 |
| 2-9 | GP14 / nDSR3 | GPIO / Data Set Ready 3 | nDSR3 | GP14 | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP17 / nRTS3/ | GPIO / Request to Send 3 | GP17 / nRTS3/ | | / HI-Z | (I/O8/OD8) / I |
| 2-9 | GP16 / nCTS3 | GPIO / Clear to Send 3 | GP16 / nCTS3 | | / HI-Z | (I/O8/OD8) / I |
| 2-9 | GP15 / nDTR3 | GPIO / Data Terminal Ready 3 | GP15 / nDTR3 | | / HI-Z | (I/O12/OD12) / O12 |
| **SERIAL PORT 4 INTERFACE** | | | | | | |
| 2-9 | GP31 / nRI4 | GPO (OD Only in Output Mode) / Ring Indicator 4 | | GP31 / nRI4 | NO GATE | (I/OD8) / I |

**TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)**

| Note | Name | Description | VCC Power Plane | VTR-POWER Plane | VCC=0 Operation (Note 2-14) | Buffer Modes (Note 2-1) |
|---|---|---|---|---|---|---|
| 2-9 | GP63* / nDCD4 | GPIO with I_VID buffer Input / Data Carrier Detect 4 | nDCD4 | GP63* | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP64* / RXD4 | GPIO with I_VID buffer Input / Receive Data 4 | RXD4 | GP64* | NO GATE | (IS/O8/OD8) / IS |
| 2-11, 2-9 | GP65* / TXD4 | GPIO with I_VID buffer Input / Transmit Data 4 | TXD4 | GP65* | / HI-Z | (I/O8/OD8) / O8 |
| 2-9 | GP66* / nDSR4 | GPIO with I_VID buffer Input / Data Set Ready 4 | nDSR4 | GP66* | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP67* / nRTS4 | GPIO with I_VID buffer Input / Request to Send 4 | nRTS4 | GP67* | / HI-Z | (I/O8/OD8) / I |
| 2-9 | GP62* / nCTS4 | GPIO with I_VID buffer Input / Clear to Send 4 | nCTS4 | GP62* | NO GATE | (I/O8/OD8) / I |
| 2-9 | GP34 / nDTR4 | GPIO (OD Only in Output Mode)/ Data Terminal Ready 4 | nDTR4 | GP34 | / HI-Z | (I/OD12) / O12 |
| **SERIAL PORT 5 INTERFACE** | | | | | | |
| | nSCOUT5 | Serial Port 5 out control | nSCOUT5 | | / HI-Z | (O8/OD8) |
| 2-9 | nSCIN5 | Serial Port 5 input Control | | nSCIN5 | NO GATE | I |
| | RXD5 | Receive 5 | RXD5 | | GATE | IS |
| | TXD5 | Serial Port 5 Transmit | TXD5 | | NO GATE / HI-Z | (O12.OD12) |
| **SERIAL PORT 6 INTERFACE** | | | | | | |
| 2-12 | GP47 / nSCOUT6 | GPIO with Schmitt trigger input Serial Port 6 output control | nSCOUT6 | GP47 / | HI-Z | (IS/O4/OD4) / (O4/OD4) |
| 2-12 | GP46 / nSCIN6 | GPIO with Schmitt trigger input Serial Port 6 input Control | | GP46 / nSCIN6 | NO GATE | (IS/O8/OD8) / (O8/OD8) |
| 2-12 | GP45 / RXD6 | GPIO with Schmitt trigger input Receive serial port 6 | RXD6 | GATE | PG | (IS/O8/OD8) / (O8/OD8) |
| 2-12 | GP44 / TXD6 | GPIO with Schmitt trigger input Serial Port 6 Transmit | TXD6 | GP44 | NO GATE/ Hi-Z | (IS/O4/OD4) / (O4/OD4) |
| **PARALLEL PORT INTERFACE** | | | | | | |
| 2-12 | nINIT | Initiate Output | nINIT | | GATE / HI-Z | (OD14/OP14) |
| 2-12 | nSLCTIN | Printer Select Input (Output to printer) | nSLCTIN | | GATE / HI-Z | (OD14/OP14) |
| 2-12 | PD0 | Port Data 0 | PD0 | | GATE / HI-Z | IOP14 |
| 2-12 | PD1 | Port Data 1 | PD1 | | GATE / HI-Z | IOP14 |
| 2-12 | PD2 | Port Data 2 | PD2 / | | GATE / HI-Z | IOP14 |