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SCH3223

LPC IO with Reset Generation, HWM and Multiple Serial Ports

Product Features

- General Features
  - 3.3 Volt Operation (SIO Block is 5 Volt Tolerant)
  - Programmable Wake-up Event (PME) Interface
  - PC99, PC2001 Compliant
  - ACPI 2.0 Compliant
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - ISA Plug-and-Play Compatible Register Set
  - Four Address Options for Power On Configuration Port
  - System Management Interrupt (SMI)
  - 19 General Purpose I/O pins, 2 with VID compatible inputs
  - Security Key Register (32 byte) for Device Authentication
- Low Pin Count Bus (LPC) Interface
  - Supports LPC Bus frequencies of 19MHz to 33MHz
- Watchdog Timer
- Resume and Main Power Good Generator
- Programmable Clock Output to 16Hz
- 2 Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with
  - Send/Receive 16-Byte FIFOs
  - Supports 230k, 460k, 921k and 1.5M Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
  - Support IRQ Sharing among serial ports
  - RS485 Auto Direction Control Mode
- Hardware Monitor
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp (processor voltage), VCC, Vbat and Vtr.
  - Remote Thermal Diode Sensing for One External Temperature Measurement accurate to 1.5°C
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - One Programmable Automatic FAN control based on temperature
- IDE Reset Output and 3 PCI Reset Buffers with Software Control Capability
- Power Button Control and AC Power Failure Recovery
- Temperature Range Available
  - Industrial (+85°C to -40°C)
  - Commercial (+70°C to 0°C)
- 64-Ball WFBGA RoHS Compliant Package

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Table of Contents

1.0 General Description 4
2.0 Pin Layout 5
3.0 Block Diagram 13
4.0 Power Functionality 14
5.0 SIO Overview 17
6.0 LPC Interface 18
7.0 Serial Port (UART) 20
8.0 Power Management 36
9.0 Serial IRQ 37
10.0 General Purpose I/O (GPIO) 40
11.0 System Management Interrupt (SMI) 45
12.0 PME Support 46
13.0 Watchdog Timer 48
14.0 Programmable Clock Output 49
15.0 Reset Generation 50
16.0 Buffered PCI Outputs 53
17.0 Power Control Features 55
18.0 Low Battery Detection Logic 62
19.0 Battery Backed Security Key Register 64
20.0 Temperature Monitoring and Fan Control 66
21.0 Hardware Monitoring Register Set 100
22.0 Config Registers 137
23.0 Runtime Registers 150
24.0 Valid Power Modes 169
25.0 Operational Description 170
26.0 Timing Diagrams 178
27.0 Package Outline 188
Appendix A: ADC Voltage Conversion 189
Appendix B: Example Fan Circuits 190
Appendix C: Revision History 193
Product Identification System 194
The Microchip Web Site 195
Customer Change Notification Service 195
Customer Support 195

1.0 GENERAL DESCRIPTION

The SCH3223 is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. The SCH3223 also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

SCH3223 The SCH3223 incorporates Super I/O functionality including LPC bus interface, a Serialized IRQ interface and the ISA Plug-and-Play standard register set (Version 1.0a). The I/O Address and hardware IRQ of each logical device in the SCH3223 may be reprogrammed through the internal configuration registers. Related functionality offers flexibility to the system designer, with General Purpose I/O control functions, and control of two LED's.

The SCH3223's Hardware Monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system of out-of-limit conditions and automatically control the speed of a fan via PWM and Tach pins. There are four analog inputs for monitoring external voltages of +5V, +2.5V, +12V and Vccp (core processor voltage), as well as internal monitoring of its VCC, VTR, and Vbat power supplies. The SCH3223 includes support for monitoring one external temperature via thermal diode inputs and an internal sensor for measuring ambient temperature. The hardware monitoring block of the SCH3223 is accessible via the LPC bus. Interrupt events can create PME wakeup events.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST and reset generation. The reset generation includes a watchdog timer which can be used to generate a reset pulse. The width of this pulse is selectable via an external strapping option.

The two serial ports are fully functional NS16550 compatible UARTs that support data rates up to 1.5 Mbps. The Serial Ports contain programmable direction control, which can automatically drive nRTS based on the status of the Output Buffer.

The SCH3223 is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes.

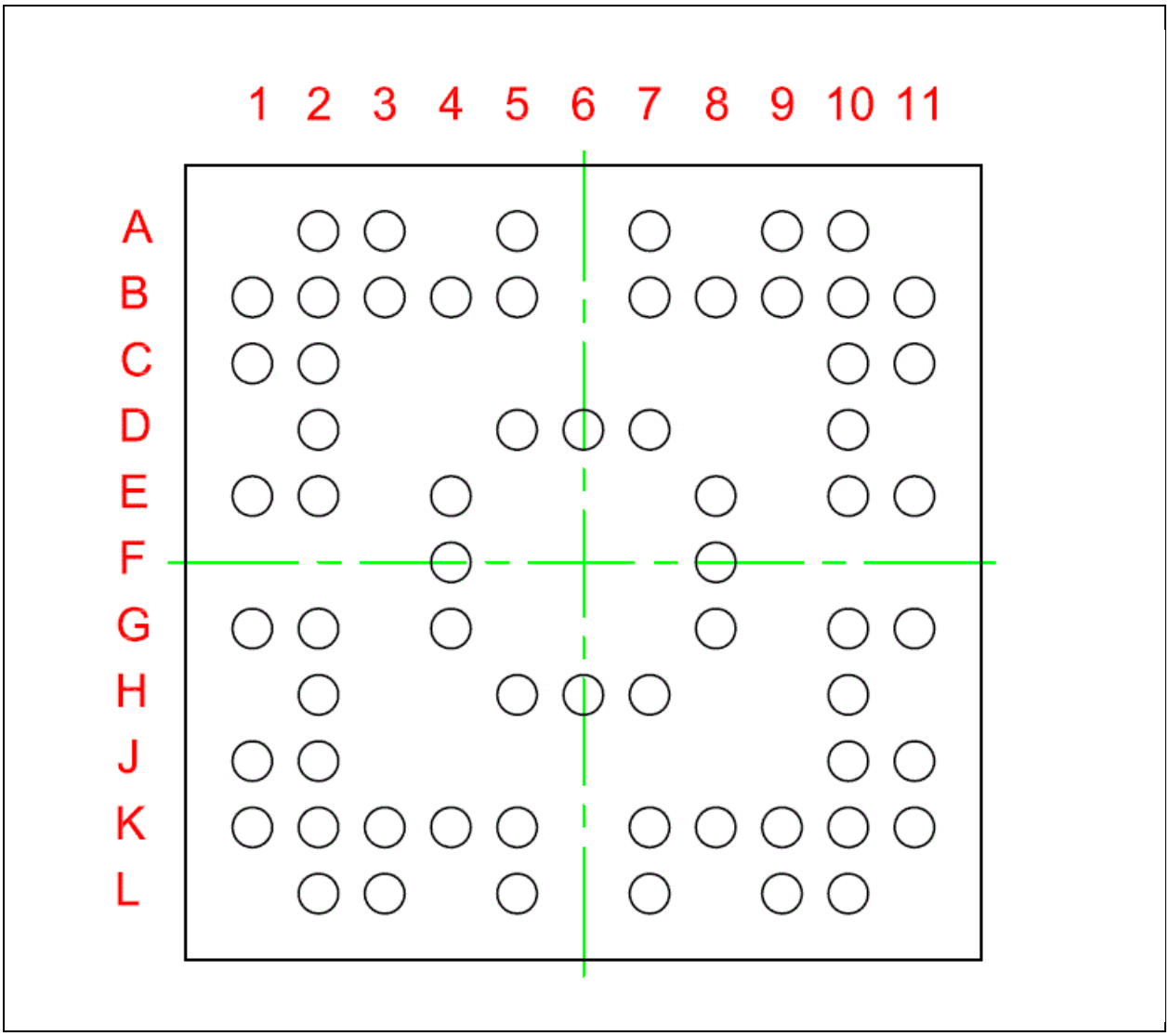
CAUTION: This device contains circuits which must not be used because their pins are not brought out of the package, and are pulled to known states internally. Any features, and especially Logical Devices, that are not listed in this document must not be activated or accessed. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.

1.1 Reference Documents

1. *Intel Low Pin Count Specification, Revision 1.0*, September 29, 1997
2. *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
3. *Advanced Configuration and Power Interface Specification, Revision 1.0b*, February 2, 1999

2.0 PIN LAYOUT

FIGURE 2-1: SCH3223 64-BALL WFBGA FOOTPRINT DIAGRAM, TOP VIEW



This is a 64-ball 6mm x 6mm package, with ball pitch of 0.5mm. However, the sparse 0.5mm pitch ball array allows 0.65mm trace routing rules. For a specific recommendation, see the drawing in Section 27.0, "Package Outline," on page 188.

2.1 SCH3223 Pin Layout Summary

TABLE 2-1: SCH3223 SUMMARY

Ball#	Function (Note 1)
B1	+12V_IN
C1	+5V_IN
C2	VTR
D2	TEST=VSS
E2	VSS
E1	CLOCKI
E4	LAD0
F4	LAD1
G4	LAD2
G2	LAD3
G1	LFRAME#
H6	PCI_RESET#
H5	PCI_CLK
H2	SER_IRQ
J2	VSS
K3	VCC
J1	nIDE_RSTDRV / GP44
K2	nPCIRST1 / GP45
K1	nPCIRST2 / GP46
L2	nPCIRST3 / GP47
L3	AVSS
K4	VBAT
K5	GP27 / nIO_SMI
L5	VTR
L9	nRI1
L10	nDCD1
K11	RXD1
K7	TXD1
K8	nDSR1
K9	nRTS1 / SYSOPT0
K10	nCTS1
J10	nDTR1 / SYSOPT1
J11	GP50 / nRI2
H10	VTR
L7	VSS
H7	GP51 / nDCD2
G11	GP52 / RXD2
G10	GP53 / TXD2
G8	GP54 / nDSR2
F8	GP55 / nRTS2 / RESGEN
E8	GP56 / nCTS2
D6	GP57 / nDTR2
D7	PB_OUT#

TABLE 2-1: SCH3223 SUMMARY (CONTINUED)

Ball#	Function (Note 1)
E10	PS_ON#
E11	PB_IN#
D10	SLP_SX#
C11	GP42 / nIO_PME
C10	GP61 / nLED2 / CLKO
B11	GP60 / nLED1 / WDT
A10	GP63
B10	CLKI32
A9	nRSMRST
B9	GP62
B8	PWRGD_OUT
B7	PWRGD_PS
A7	nFPRST / GP30
A5	PWM1
B5	FANTACH1
D5	HVSS
B4	HVTR
B3	REMOTE1-
A3	REMOTE1+
B2	VCCP_IN
A2	+2.5V_IN

Note 1: Device ID register at Plug&Play Index 0x20 holds 0x7D.

2.2 Pin Functions

TABLE 2-2: SCH3223 PIN FUNCTIONS DESCRIPTION

Note	Name	Description	VCC Power Plane	VTR Power Plane	VCC=0 Operation (Note 2-10)	Buffer Modes (Note 2-1)
POWER PINS						
2-3, 2-4	VCC	+3.3 Volt Supply Voltage				
2-3, 2-4	VTR	+3.3 Volt Standby Supply Voltage				
2-6	VBAT	+3.0 Volt Battery Supply)				
	VSS	Ground				
	AVSS	Analog Ground				
2-3	HVTR	Analog Power. +3.3V VTR pin dedicated to the Hardware Monitoring block. HVTR is powered by +3.3V Standby power VTR.				

TABLE 2-2: SCH3223 PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR Power Plane	VCC=0 Operation (Note 2-10)	Buffer Modes (Note 2-1)
2-3	HVSS	Analog Ground. Internally connected to all of the Hardware Monitoring Block circuitry.				
CLOCK PINS						
	CLKI32	32.768kHz Trickle Clock Input		CLKI32	No Gate	IS
	CLOCKI	14.318MHz Clock Input	CLOCKI			IS
LPC INTERFACE						
	LAD[3:0]	Multiplexed Command Address and Data	LAD[3:0]		GATE/ Hi-Z	PCI_IO
	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	LFRAME#		GATE	PCI_I
	PCI_RESET#	PCI Reset	PCI_RESET#		NO GATE	PCI_I
	PCI_CLK	PCI Clock	PCI_CLK		GATE	PCI_ICLK
	SER_IRQ	Serial IRQ	SER_IRQ		GATE / Hi-Z	PCI_IO
SERIAL PORT 1 INTERFACE						
	RXD1	Receive Data 1	RXD1		GATE	IS
	TXD1	Transmit Data 1	TXD1		HI-Z	O12/O12
	nDSR1	Data Set Ready 1	nDSR1		GATE	I
2-5	nRTS1 / SYSOPT0	Request to Send 1/ SYSOPT (Configuration Port Base Address Control)	nRTS1/ SYSOPT0		GATE/ Hi-Z	OP14 / I
	nCTS1	Clear to Send 1	nCTS1		GATE	I
	nDTR1 / SYSOPT1	Data Terminal Ready 1	nDTR1 / SYSOPT1		GATE/ Hi-Z	O6 / I
2-7	nRI1	Ring Indicator 1		nRI1	GATE	IS
	nDCD1	Data Carrier Detect 1	nDCD1		GATE	I
SERIAL PORT 2 INTERFACE						
2-7	GP50 / nRI2	Ring Indicator 2	GP50	nRI2	NO GATE/ HI-Z	(I/OD8/OD8) / IS
2-7	GP51 / nDCD2	Data Carrier Detect 2	GP51 / nDCD2		NO GATE/ HI-Z	(I/OD8/OD8) / I
2-7	GP52 / RXD2	Receive Data 2	GP52 / RXD2		NO GATE/ HI-Z	(I/OD8OD8) / IS
2-9, 2-7	GP53 / TXD2	Transmit Data 2	GP53 / TXD2		NO GATE/ HI-Z	(I/O12/OD12) / (O12/OD12)
2-7	GP54 / nDSR2	Data Set Ready 2	GP54 / nDSR2		NO GATE/ HI-Z	(I/OD8/OD8) / I
2-7 2-11	GP55 / nRTS2 / RESGEN	Request to Send 2 / Reset Generator Pulse Width Strap Option	GP55 / nRTS2 / RESGEN		NO GATE/ HI-Z	(I/O8/OD8) / I / IOP8
2-7	GP56 / nCTS2	Clear to Send 2	GP56 / nCTS2		NO GATE/ HI-Z	(I/OD8OD8) / I
2-7	GP57 / nDTR2	Data Terminal Ready 2	GP57 / nDTR2		NO GATE/ HI-Z	(I/OD8OD8) / O6

TABLE 2-2: SCH3223 PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR Power Plane	VCC=0 Operation (Note 2-10)	Buffer Modes (Note 2-1)
MISCELLANEOUS PINS						
	GP42/ nIO_PME	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in either S3 or S5 and below.		GP42/ nIO_PME	NO GATE	(I/O12/OD12) /(O12/OD12)
2-6, 2-7	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output		GP60 /nLED1 /WDT	NO GATE	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
	nFPRST / GP30	Front Panel Reset / General Purpose IO		nFPRST / GP30	NO GATE	ISPU_400 / (I/O4/OD4)
	PWRGD_PS	Power Good Input from Power Supply		PWRGD_PS	NO GATE	ISPU_400
	PWRGD_OUT	Power Good Output – Open Drain		PWRGD_ OUT	NO GATE	OD8
	nRSMRST	Resume Reset Output		nRSMRST	NO GATE	OD24
2-6, 2-7	GP61 /nLED2 / CLKO	General Purpose I/O /nLED2 / Programmable Clock Output		GP61 /nLED2 / CLKO	NO GATE	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-7	GP27 /nIO_SMI	General Purpose I/O /System Mgt. Interrupt	GP27 /nIO_SMI	GP27	/ HI-Z	(I/O12/OD12) /(O12/OD12)
	TEST	Test purposes. Customer should tie this pin to VSS at all times.	TEST	TEST		
HARDWARE MONITORING BLOCK						
2-8	+5V_IN	Analog input for +5V	HVTR			I_{AN}
2-8	+2.5_IN	Analog input for +2.5V	HVTR			I_{AN}
2-8	VCCP_IN	Analog input for +Vccp (processor voltage: 1.5 V nominal).	HVTR			I_{AN}
2-8	+12V_IN	Analog input for +12V	HVTR			I_{AN}
	REMOTE1-	This is the negative input (current sink) from the remote thermal diode 1.	HVTR			I_{AND-}
	REMOTE1+	This is the positive input (current source) from the remote thermal diode 1.	HVTR			I_{AND+}
	PWM1	Fan Speed Control 1 Output.		PWM1		OD8
	FANTACH1	Tachometer Input 1 for monitoring a fan.		FANTACH 1		I_M
RESET OUTPUTS						
	nPCIRST3 / GP47	PCI Reset output 3 GPIO with Schmitt trigger input	nPCIRST3	GP47	NO GATE	(O4/OD4) / (IS/O4/OD4)
	nPCIRST2 / GP46	PCI Reset output 2 GPIO with Schmitt trigger input	nPCIRST2	GP46	NO GATE	(O8/OD8) / (IS/O8/OD8)

TABLE 2-2: SCH3223 PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR Power Plane	VCC=0 Operation (Note 2-10)	Buffer Modes (Note 2-1)
	nPCIRST1 / GP45	PCI Reset output 1 GPIO with Schmitt trigger input	nPCIRST1	GP45	NO GATE	(O8/OD8) / (IS/O8/OD8)
	nIDE_RSTDRV / GP44	IDE Reset output GPIO with Schmitt trigger input	nIDE_RSTDRV	GP44	NO GATE	(O4/OD4) / (IS/O4/OD4)
GLUE LOGIC						
	PB_IN#	Power Button In is used to detect a power button event		PB_IN#	NO GATE	I
2-7	SLP_SX#	Sx Sleep State Input Pin.		SLP_SX#	NO GATE	I
	PB_OUT#	Power Button Out		PB_OUT#	NO GATE	O8
	PS_ON#	Power supply On		PS_ON#	NO GATE	O12
DEDICATED GPIO						
2-7	GP62*	GPIO with I_VID buffer Input		GP62*	NO GATE	(I/O8/OD8)
2-7	GP63*	GPIO with I_VID buffer Input		GP63*	NO GATE	(I/O8/OD8)

Note 2-1 Buffer types per function on multiplexed pins are separated by a slash "/". Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 2-2 Pins that have input buffers must always be held to either a logical low or a logical high state when powered. Bi-directional buses that may be trisected should have either weak external pull-ups or pull-downs to hold the pins in a logic state (i.e., logic states are VCC or ground).

Note 2-3 VCC and VSS pins are for Super I/O Blocks. HVTR and HVSS are dedicated for the Hardware Monitoring Block.

Note 2-4 VTR can be connected to VCC if no wake-up functionality is required.

Note 2-5 The nRTS1/SYSOPT0 pin requires an external pull-down resistor to put the base I/O address for configuration at 0x02E. An external pull-up resistor is required to move the base I/O address for configuration to 0x04E.

Note 2-6 The LED pins are powered by VTR so that the LEDs can be controlled when the part is under VTR power.

Note 2-7 This pin is an input into the wake-up logic that is powered by VTR. In the case of a ring indicator for a serial port, or a GPIO it will also go to VCC powered logic. This logic must be disabled when VCC=0.

Note 2-8 This analog input is backdrive protected. Although HVTR is powered by VTR, it is possible that monitored power supplies may be powered when HVTR is off.

Note 2-9 The GP53/TXD2 pin defaults to the GPIO input function on a VTR POR and presents a tristate impedance. When VCC=0 the pin is tristate. If GP53 function is selected and VCC is power is applied, the pin reflects the current state of GP53. The GP53/TXD2 pin is tristate when it is configured for the TXD2 function.

Note 2-10 All logic is powered by VTR. Vcc on pin 29 is used as an indication of the presence of the VCC rail being active. All logic that requires VCC power, is only enabled when the VCC rail is active.

Note 2-11 The GP55/nRTS2/RESGEN pin requires an external pull-down resistor to enable 500ms delay circuit. An external pull-up resistor is required to enable 200ms delay circuit.

User's Note:

Open-drain pins should be pulled-up externally to supply shown in the power well column. All other pins are driven under the power well shown.

- NOMENCLATURE:
  - No Gate indicates that the pin is not protected, or affected by VCC=0 operation
  - Gate indicates that the pin is protected as an input (if required) or set to a HI-Z state as an output (if required)
  - In these columns, information is given in order of pin function: e.g. 1st pin function / 2nd pin function

2.3 Buffer Description

Table 2-3 lists the buffers that are used in this device. A complete description of these buffers can be found in Section 25.0, "Operational Description," on page 170.

TABLE 2-3: BUFFER DESCRIPTION

Buffer	Description
I	Input TTL Compatible - Super I/O Block.
IL	Input, Low Leakage Current.
I_M	Input - Hardware Monitoring Block.
I_{AN}	Analog Input, Hardware Monitoring Block.
I_{ANP}	Back Bias Protected Analog Input, Hardware Monitoring Block.
I_{AND-}	Remote Thermal Diode (current sink) Negative Input
I_{AND+}	Remote Thermal Diode (current source) Positive Input
IS	Input with Schmitt Trigger.
I_VID	Input. See DC Characteristics Section.
I_MOD3	Input/Output (Open Drain), 3mA sink.
I_MO3	Input/Output, 3mA sink, 3mA source.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
IOD8	Input/Open Drain Output, 8mA sink, 4mA source.
IS/O8	Input with Schmitt Trigger/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
OD4	Open Drain Output, 4mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
IOD12	Input/Open Drain Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
OD_PH	Input/Output (Open Drain), See DC Electrical Characteristics on page 170
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
IO16	Input/Output 16mA sink.
IOD16	Input/Output (Open Drain), 16mA sink.
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics.
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics.
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics.
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing.

TABLE 2-3: BUFFER DESCRIPTION (CONTINUED)

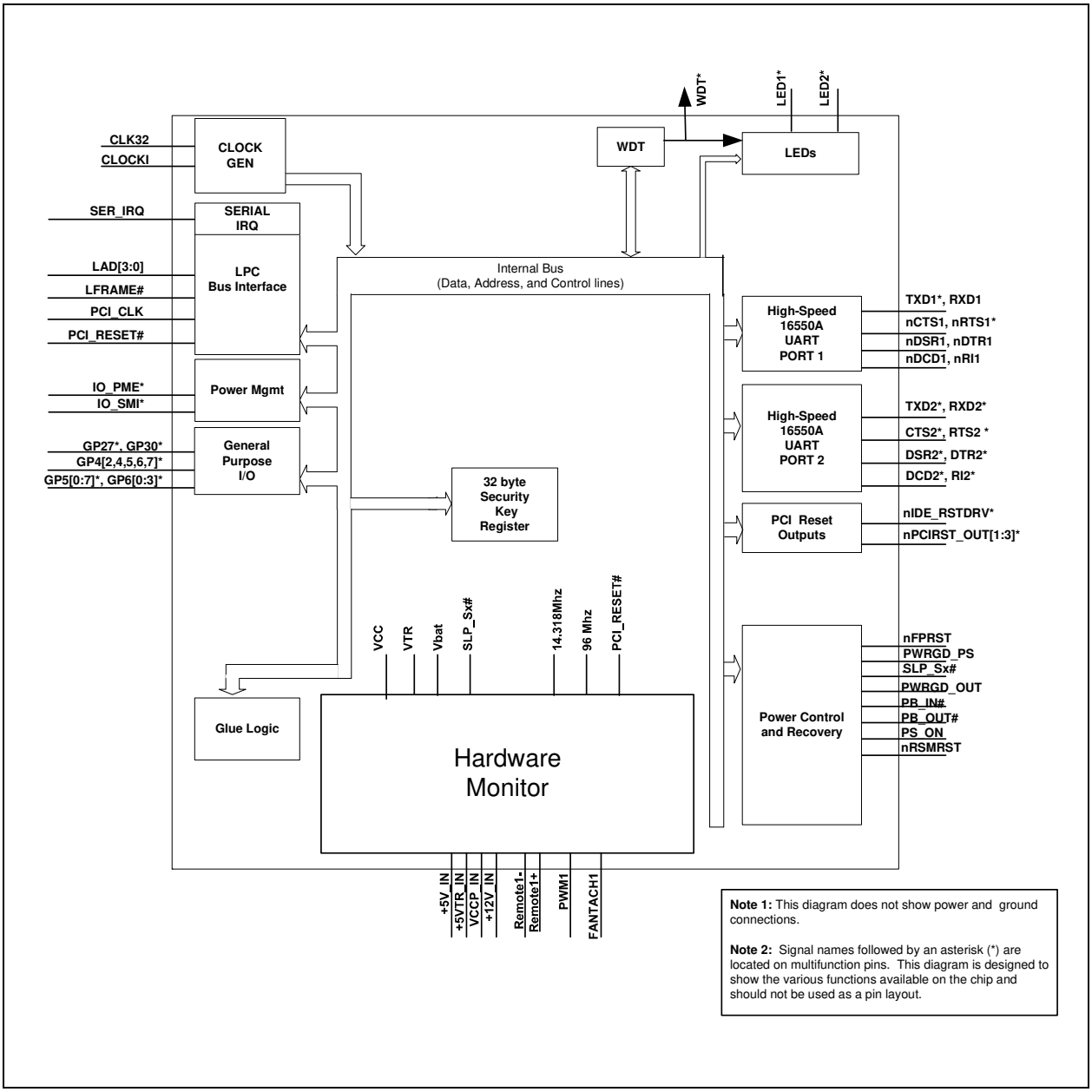
Buffer	Description
nSW	n Channel Switch (R_{on}~25 Ohms)
ISPU_400	Input with 400mV Schmitt Trigger and 30uA Integrated Pull-Up.
ISPU	Input with Schmitt Trigger and Integrated Pull-Up.

Note 2-12 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2.

Note 2-13 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2 and 4.2.3.

3.0 BLOCK DIAGRAM

FIGURE 3-1: SCH3223 BLOCK DIAGRAM



4.0 POWER FUNCTIONALITY

The SCH3223 has five power planes: VCC, HVTR, VREF, VTR, and Vbat.

4.1 VCC Power

The SCH3223 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). VCC is the main power supply for the Super I/O Block. See Section 25.2, "DC Electrical Characteristics," on page 170.

4.2 HVTR Power

The HVTR supply is 3.3 Volts (nominal). HVTR is a dedicated power supply for the Hardware Monitoring Block. HVTR is connected to the VTR suspend well. See Section 25.2, "DC Electrical Characteristics," on page 170.

Note:	The hardware monitoring logic is powered by HVTR, but only operational when VCC is on. The hardware monitoring block is connected to the suspend well to retain the programmed configuration through a sleep cycle.

4.3 VTR Support

The SCH3223 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See Section 25.0, "Operational Description," on page 170. The maximum VTR current that is required depends on the functions that are used in the part. See Section 25.0.

If the SCH3223 is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. VTR powers the IR interface, the PME configuration registers, and the PME interface. The VTR pin generates a VTR Power-on-Reset signal to initialize these components. If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 ms before Vcc begins a power-on cycle. Note that under all circumstances, the hardware monitoring HVTR must be driven as the same source as VTR.

4.3.1 TRICKLE POWER FUNCTIONALITY

When the SCH3223 is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP27, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are PME wakeup as a GPIO (or alternate function).

The other GPIOs function as follows:

GP42, GP60 and GP61:

- Buffers powered by VTR. GP42 is the nIO_PME pin which is active under VTR. GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- PME runtime register block (includes all PME, SMI, GPIO, Fan and other miscellaneous registers)
- Digital logic in the Hardware Monitoring block
- LED control logic
- Watchdog Timer

- Power Recovery Logic
- Pins for PME Wakeup:
  - GP42/nIO_PME (output, buffer powered by VTR)
  - CLOCKI32 (input, buffer powered by VTR)
  - nRI1 (input)
  - GP50/nRI2 (input)
  - GP52/RXD2 (input)
  - GPIOs (GP27, GP50-GP57, GP60, GP61) – all input-only except GP60, GP61. See below.
- Other Pins
  - GP60/LED1 (output, buffer powered by VTR)
  - GP61/LED2 (output, buffer powered by VTR)
  - nRSMRST
  - PWRGD_PS
  - PB_IN#
  - PB_OUT#
  - PS_ON#
  - nFPRST
  - SLP_SX#
  - PWRGD_OUT

4.4 Vbat Support

Vbat is a battery generated power supply that is needed to support the power recovery logic. The power recovery logic is used to restore power to the system in the event of a power failure. Power may be returned to the system by the main power button, or by the power recovery logic following an unexpected power failure.

The Vbat supply is 3.0 Volts (nominal). See Section 25.0, "Operational Description," on page 170.

The following Runtime Registers are powered by Vbat:

- Bank 2 of the Runtime Register block used for the 32kbyte Security Key register
- PME_EN7 at offset 10h
- PWR_REC Register at offset 49h
- PS_ON Register at offset 4Ah
- PS_ON Previous State Register at offset 53h

Note:	All Vbat powered pins and registers are powered by VTR when VTR power is on and are battery backed-up when VTR is removed.

4.5 32.768 KHz Trickle Clock Input

The SCH3223 utilizes a 32.768 KHz trickle input to supply a clock signal for the WDT, LED blink and Power Recovery Logic.

Indication of 32KHZ Clock

There is a bit to indicate whether or not the 32KHz clock input is connected to the SCH3223. This bit is located at bit 0 of the CLOCKI32 register at 0xF0 in Logical Device A. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32KHz clock is connected to the CLKI32 pin (default)

1=32KHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32KHz (nominal) clock for the LED blink logic. When the external 32KHz clock is connected, that will be the source for the LED logic. When the external 32KHz clock is not connected, an internal 32KHz clock source will be derived from the 14MHz clock for the LED logic.

The following functions will not work under VTR power (VCC removed) if the external 32KHz clock is not connected. These functions will work under VCC power even if the external 32 KHz clock is not connected.

- LED blink
- Power Recovery Logic
- WDT
- Front Panel Reset with Input Debounce, Power Supply Gate, and CPU Powergood Signal Generation

4.6 Super I/O Functions

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The super I/O pins that are powered by VTR are as follows: GP42/nIO_PME, GP60/LED1, and GP61/LED2. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum Vbat current, I_{bat}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

4.7 Power Management Events (PME/SCI)

The SCH3223 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the Section 12.0, "PME Support," on page 46 section.

5.0 SIO OVERVIEW

The SCH3223 is a Super I/O Device with hardware monitoring. The Super I/O features are implemented as logical devices accessible through the LPC interface. The Super I/O blocks are powered by VCC, VTR, or Vbat. The Hardware Monitoring block is powered by HVTR and is accessible via the LPC interface. The following chapters define each of the functional blocks implemented in the SCH3223, their corresponding registers, and physical characteristics.

This chapter offers an introduction into the Super I/O functional blocks, registers and host interface. Details regarding the hardware monitoring block are defined in later chapters. Note that the Super I/O registers are implemented as typical Plug-and-Play components.

5.1 Super I/O Registers

The address map, shown below in Table 5-1 shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of all the Super I/O Logical Blocks, including the configuration register block, can be moved or relocated via the configuration registers.

Note:	Some addresses are used to access more than one register.

5.2 Host Processor Interface (LPC)

The host processor communicates with the Super I/O features in the SCH3223 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 5-1, "Super I/O Block Addresses". Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Note:	The SCH3223 does not use or need LPC DMA.

TABLE 5-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name	Logical Device	Notes
na	Reserved	0, 1, 2, 3	
Base+(0-7)	Serial Port Com 1	4	
Base+(0-7)	Serial Port Com 2	5	
na	Reserved	6, 7, 8, 9	
Base1 + (0-7F) Base2 + (0-1F)	Runtime Registers Security Key Registers	A	(Note 5-2)
na	Reserved	B, C, D, E, F	
Base + (0-1)	Configuration		(Note 5-1)

Note 5-1 Refer to the configuration register descriptions for setting the base address.

Note 5-2 Logical Device A is referred to as the Runtime Register block at Base1 or PME Block and may be used interchangeably throughout this document.

Note 5-3 na = not applicable

6.0 LPC INTERFACE

6.1 LPC Interface Signal Definition

The signals implemented for the LPC bus interface are described in the tables below. LPC bus signals use PCI 33MHz electrical signal characteristics.

6.1.1 LPC REQUIRED SIGNALS

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
PCI_CLK	Input	PCI Clock.

6.1.2 LPC OPTIONAL SIGNALS

Signal Name	Type	Description	Comment
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.	Not implemented
SER_IRQ	I/O	Serial IRQ.	Implemented
CLKRUN#	OD	Clock Run	Not Implemented
nIO_PME	OD	Same as the PME# or Power Mgt Event signal. Allows the SCH3223 to request wakeup in S3 and below.	Implemented
LPCPD#	I	Power down - Indicates that the device should prepare for LPC I/F shutdown	Not Implemented
LSMI#	OD	Only need for SMI# generation on I/O instruction for retry.	Not Implemented

6.2 Supported LPC Cycles

Table 6-1 summarizes the cycle types are supported by the SCH3223. All other cycle types are ignored.

TABLE 6-1: SUPPORTED LPC CYCLES

Cycle Type	Transfer Size	Comment
I/O Write	1 Byte	Supported
I/O Read	1 Byte	Supported
Memory Write	1 Byte	Not Supported
Memory Read	1 Byte	Not Supported
DMA, Bus Master	any	Not Supported

6.3 Device Specific Information

The LPC interface conforms to the *"Low Pin Count (LPC) Interface Specification"*. The following section will review any implementation specific information for this device.

Note: The SCH3223 packaging does not support any form of DMA, as it has no peripherals that would use it.

6.3.1 SYNC PROTOCOL

The SYNC pattern is used to add wait states. For read cycles, the SCH3223 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SCH3223 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SCH3223 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value. The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks.

The SYNC value of 0110 is intended to be used where the number of wait states is large. However, the SCH3223 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

6.3.2 RESET POLICY

The following rules govern the reset policy:

- When PCI_RESET# goes inactive (high), the PCI clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
- When PCI_RESET# goes active (low):

1. The host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
2. The SCH3223 ignores LFRAME#, tristates the LAD[3:0] pins and drives the LDRQ# signal inactive (high).

7.0 SERIAL PORT (UART)

The SCH3223 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic “1”. OUT2 being a logic “0” disables that UART’s interrupt.

7.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Section 22.0, "Config Registers," on page 137). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The register set of the UARTS are described below.

TABLE 7-1: ADDRESSING THE SERIAL PORT

DLAB*	A2	A1	A0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note: *DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

7.1.1 RECEIVE BUFFER REGISTER (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

7.1.2 TRANSMIT BUFFER REGISTER (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

7.1.3 INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH3223. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic “1”.

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic “1”.

Bit 2

This bit enables the Received Line Status Interrupt when set to logic “1”. The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic “1”. This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic “0”.

7.1.4 FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCRs are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x21).

Bit 0

Setting this bit to a logic “1” enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic “0” disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic “1” clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic “1” clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the Trigger Level For The Rcvr Fifo Interrupt.

7.1.5 INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 7-2 on page 22). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic “0”, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic “1”, no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table (Table 7-2).

Bit 3

In non-FIFO mode, this bit is a logic “0”. In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic “0”.

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

TABLE 7-2: INTERRUPT CONTROL

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.

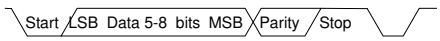
TABLE 7-2: INTERRUPT CONTROL (CONTINUED)

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

7.1.6 LINE CONTROL REGISTER (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

FIGURE 7-1: SERIAL DATA



This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Bit 2	Word Length	Number of Stop Bits
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic “1”, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic “1” and bit 4 is a logic “0”, an odd number of logic “1”’s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic “1” and bit 4 is a logic “1” an even number of bits is transmitted and checked.

Bit 5

This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic “1”, the transmit data output (TXD) is forced to the Spacing or logic “0” state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic “1”) to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic “0”) to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

7.1.7 MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic “1”, the nDTR output is forced to a logic “0”. When bit 0 is a logic “0”, the nDTR output is forced to a logic “1”.

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic “1”, the following occur:

1. The TXD is set to the Marking State (logic “1”).
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

7.1.8 LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least ½ bit time.

Note:	Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

