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Data Sheet

SCR1100-D02 SINGLE AXIS GYROSCOPE WITH DIGITAL SPI INTERFACE

Features

- ±100 º/s angular rate measurement range
- Angular rate measurement around X axis
- Angular rate sensor exceptionally insensitive to mechanical vibrations and shocks
- Superior bias instability for MEMS gyroscopes (<1º/h)
- Digital SPI interfacing
- Enhanced self diagnostics features
- Small size 8.5 x 18.7 x 4.5 mm (w x l x h)
- RoHS compliant robust packaging suitable for lead free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology
- Temperature range -40 °C...+125 °C

Applications

SCR1100-D02 is targeted to applications with high stability and tough environmental requirements. Typical applications are:

- Inertial Measurement Units (IMUs) for highly demanding environments
- Platform stabilization and control
- Motion analysis and control
- Roll over detection
- Robotic control systems
- Guidance systems
- Navigation systems

General Description

SCR1100-D02 is a single axis high performance gyroscope. It is part of VTI's high performance gyro family and it has the same gyro section as the combined gyro acceleration product SCC1300-D02. The sensor is based on VTI's proven capacitive 3D-MEMS technology and it has highly sophisticated signal conditioning ASIC with digital SPI interface. Small robust packaging guarantees reliable operation over product lifetime. The housing is suitable for SMD mounting and the component is compatible with RoHS and ELV directives.

SCR1100-D02 is designed, manufactured and tested against high stability, reliability and quality requirements. The angular rate sensor provides highly stable output over wide ranges of temperature and mechanical noise. The bias stability is in the elite of MEMS gyros and the component has several advanced self diagnostics features.

TABLE OF CONTENTS

1 General Description

1.1 Introduction

This document contains essential technical information for SCR1100 sensor. Specifications, SPI interface descriptions, user accessible register details, electrical properties and application information etc. This document should be used as a reference when designing in SCR1100 component.

1.2 General Product Description

The SCR1100 sensor consists of silicon based MEMS angular rate sensing element and Application Specific Integrated Circuits (ASIC) used to sense and control sensing element. Figure 1 represents an upper level block diagram of the component. ASIC have digital SPI interfaces to control and read the gyroscope.

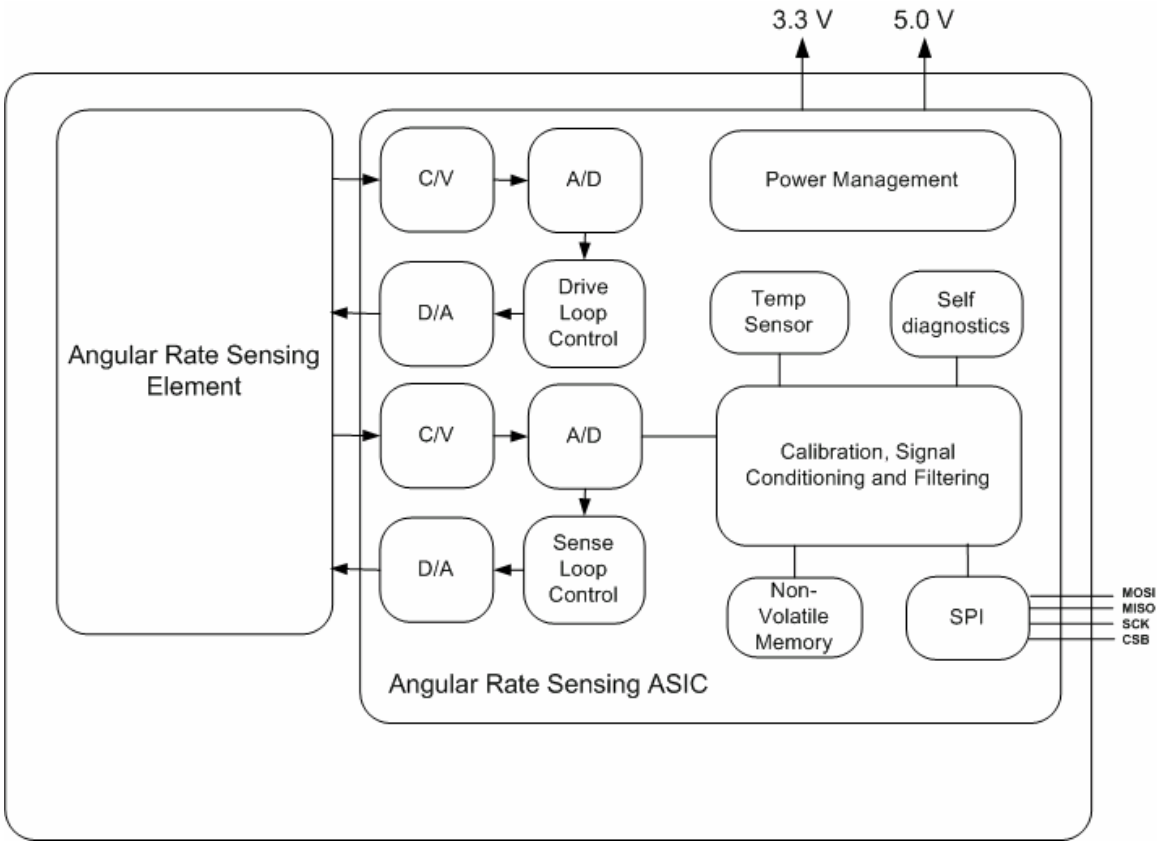

Figure 1. SCR1100 component block diagram.

The angular rate sensing element is manufactured using VTI proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

The angular rate sensing element consists of moving masses that are purposely exited to in-plane drive motion. Rotation in sensitive direction causes out-of-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

1.2.1 Factory Calibration

SCR1100 sensor is factory calibrated. No separate calibration is required in the application. Trimmed parameters during production include sensitivities and offsets over temperature, and frequency responses. *However it should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.*

Calibration parameters are stored during manufacturing inside non-volatile memory. The parameters are read automatically from the internal non-volatile memory during the start-up.

1.3 Abbreviations

ASIC	Application Specific Integrated Circuit
SPI	Serial Peripheral Interface
RT	Room Temperature
STC	Self Test Continuous (continuous self testing of accelerometer element)
STS	Self Test Static (gravitational based self test of accelerometer element)
Avdd	Analog supply voltage
Dvdd	Digital supply voltage

2 Specifications

2.1 Performance Specifications for Gyroscope

Table 1. Gyroscope performance specifications (Avdd = 5 V, Dvdd = 3.3 V and ambient temperature unless otherwise specified).

Parameter	Condition	Min [A]	Typ	Max [A]	Units
Analog supply voltage		4.75	5	5.25	V
Analog supply current	Temperature range -40 ... +125 °C	24	26	29.5	mA
Digital supply voltage		3.0	3.3	3.6	V
Digital supply current	Temperature range -40 ... +125 °C	16	20	24	mA
Operating range	Measurement axis X	-100		100	°/s
Offset error [B]		-1		1	°/s
Offset over temperature	Temperature range -40 ... +125 °C	-0.6		0.6	°/s
	Temperature range -10 … +60 °C	-0.3		0.3	°/s
Offset drift velocity	Temperature gradient ≤ 2.5 K/min	-0.3		0.3	(°/s)/min
Bias instability [C]			<1		°/h
Angular random walk (ARW) [C]			0.45		°/√h
Sensitivity			50		LSB/(°/s)
Sensitivity over temperature	Temperature range -40 ... +125 °C	-1		1	%
Total sensitivity error [B]		-2		2	%
Nonlinearity	Temperature range -40 ... +125 °C	-0.5		0.5	°/s
Noise (RMS)			0.06	0.1	°/s
Noise Density			0.0085		(°/s)/√Hz
Cross-axis sensitivity				1.7	%
G-sensitivity		-0.1		0.1	(°/s)/g
Shock sensitivity	50g, 6ms			2.0	°/s
Shock recovery time				50.0	ms
Amplitude response	-3dB frequency		50		Hz
Quantization				0.05	°/s
Power on setup time				0.8	s
Output data rate			2		kHz
Output load				200	pF
SPI clock rate		0.1		8	MHz

A) MIN/MAX values are ±3 sigma variation limits from validation test population.

B) Including calibration error and drift over lifetime.

C) Typical, constant temperature, Allan Variance curve Figure 2 b).

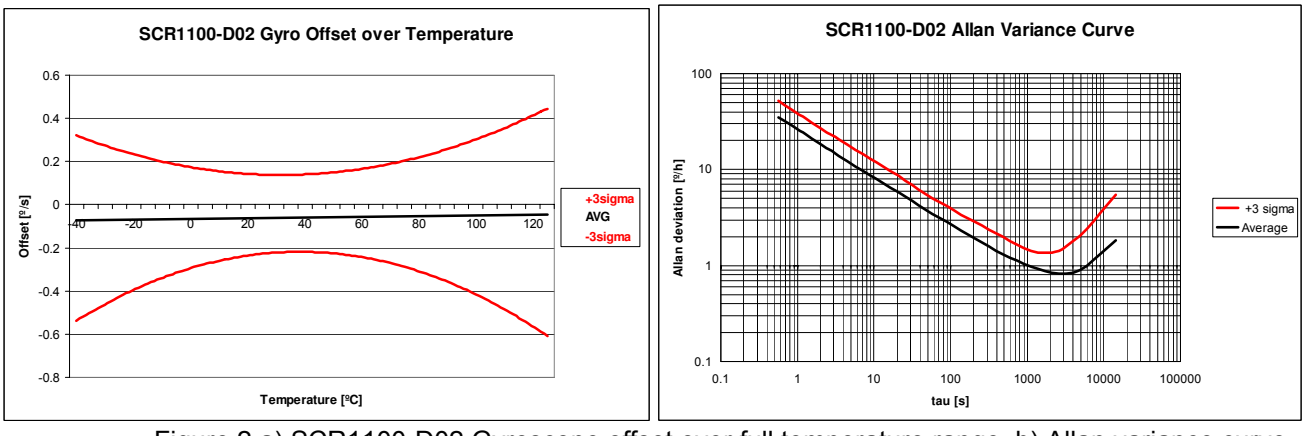

Figure 2 a) SCR1100-D02 Gyroscope offset over full temperature range, b) Allan variance curve

2.2 Absolute Maximum Ratings

Table 2. Absolute maximum ratings of the SCR1100 sensor.

Parameter	Condition	Min	Typ	Max	Units
Analog supply voltage, AVDD_G		-0.5		7	V
Digital supply voltage, DVDD_G		-0.3		3.6	V
Maximum voltage at analog input/output pins		-0.3		AVDD_G + 0.3V	
Maximum voltage at digital input/output pins		-0.3		DVDD_G + 0.3	V
Operating temperature		-40		125	°C
Storage temperature		-40		125	°C
	Max 96h	-40		150	°C
Maximum junction temperature during lifetime. Note: device has to be functional, but not in full spec.				155	°C
Mechanical Shock			3000		g
ESD	HBM			2	kV
	CDM			500	V
Ultrasonic Cleaning	Prohibited				

2.3 Digital I/O Specification

Table 3 below describe the DC characteristics of SCR1100 sensor digital I/O pins. Supply voltage is 3.3 V unless otherwise noted. Current flowing into the circuit has positive values.

Table 3. Absolute maximum ratings of the SCR1100 gyroscope SPI interface.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSN_G						
Pull up current	V_{IN} = 0 V	I_{PU}	10		50	µA
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
V_{IN}	Open circuit	V_{IN}	2			V
Input terminal SCK_G						
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
Input leakage current	0 < V_{MISO} < 3.3 V	I_{LEAK}	-1		1	uA
Output terminal MOSI_G						
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
Input current source (pull-down)	V_{IN} = V_{DVDD_G}	I_{LEAK}	10		50	uA
V_{IN}	Open circuit	V_{IN}			0.3	V
Output terminal MISO_G (Tri-state)						
Output high voltage	I_{OUT} = -1mA	V_{OH}	DVDD_G -0.5V			V
	I_{OUT} = -50µA		DVDD_G -0.2V			V
Output low voltage	0 ≤ V_{MISO} ≤ 3.3 V	V_{OL}			0.5	V
Capacitive load					200	pF

2.4 SPI AC Characteristics

The AC characteristics of SCR1100 are defined in Figure 3 and Table 4.

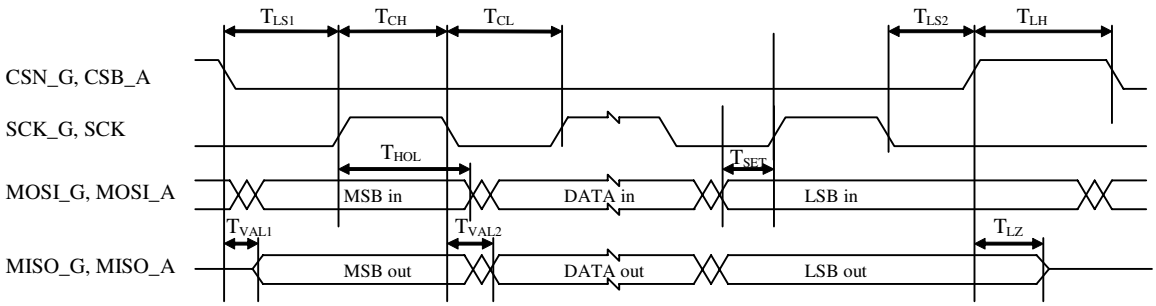

Figure 3. Timing diagram of SPI communication

Table 4. Timing Characteristics of SPI Communication.

Parameter	Condition	Min	Typ	Max	Units
F_{SPI}				8	MHz
T_{SPI}			1/ F_{SPI}		
T_{CH}	SCK_G high time	T_{SPI} /2			ns
T_{CL}	SCK_G low time	T_{SPI} /2			ns
T_{LS1}	CSN_G setup time	T_{SPI} /2			ns
T_{VAL1}	Delay CSN_G -> MISO_G			T_{SPI} /4	ns
T_{SET}	MOSI_G setup time	T_{SPI} /4			ns
T_{HOL}	MOSI_G data hold time	T_{SPI} /4			ns
T_{VAL2}	Delay SCK_G -> MISO_G			1.3 * T_{SPI} /4	ns
T_{LS2}	CSN_G hold time	T_{SPI} /2			ns
T_{LZ}	Tri-state delay time			T_{SPI} /4	ns
T_{RISE}	Rise time of the SCK_G			10	ns
T_{FALL}	Fall time of the SCK_G			10	ns
T_{LH}	Time between SPI cycles	T_{SPI}			ns

3 Reset and Power Up

After the start-up the angular rate and acceleration data is immediately available through SPI registers. There is no need to initialize the gyroscope or accelerometer before starting to use it. If the application requires monitoring operation correctness there are several options available to monitor the status.

3.1 Power-up Sequence

To ensure correct ASIC start up please connect the digital supply voltage V_{DVDD_G} (3.3V) before the analog supply voltage V_{AVDD_G} (5.0V) to the gyro ASIC. After power up please read Status register twice to clear error flags. Angular rate data is available immediately so no start up command sequence is required if error flags are not used.

Table 5. SCR1100 gyroscope power-up sequence.

Procedure	Functions	Check
Set V_{DVDD_G} V=3.0...3.6V		
Wait 10ms		
Set V_{AVDD_G} V=4.75...5.25V		
Wait 800 ms		
Read Status register (08h) two times	Acknowledge error flags after start up	

3.2 Reset

SCR1100 can be reset by writing 0x04 in to IC Identification register (address 07h) or with external active low reset pin (EXTRESN_G). Power supplies should be within the specified range before the reset pin can be released.

4 Component Interfacing

4.1 SPI Interfaces

SCR1100 sensor SPI interface is a digital 4 wire interface where SCR1100 always operate as slave devices in the master-slave operation mode.

SCR1100 Angular rate sensor ASIC SPI interface:

MOSI_G	master out slave in	µP → ASIC
MISO_G	master in slave out	ASIC → µP
SCK_G	serial clock	µP → ASIC
CSN_G	chip select (low active)	µP → ASIC

4.1.1 SPI Transfer

The SPI transfer is based on a 16-bit protocol. Figure 5 shows an example of a single 16-bit data transmission. Each output data/status-bits are shifted out on the falling edge of SCK (MISO line). Each bit is sampled on the rising edge of SCK (MOSI line).

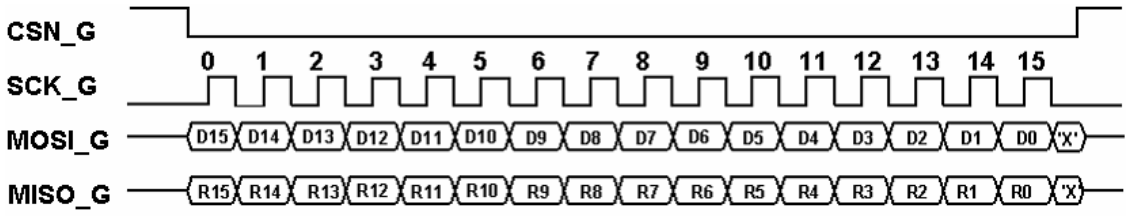

Figure 4. SCR1100 angular rate sensor 16-bit data transmission.

After the falling edge of CSN_G the device interprets the first 16-bit word is an address transfer having a bit coding scheme below.

Address Transfer:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	RW	0	Par odd

ADR[6:0] : Register address
RW : RW=1 : Write access
RW=0 : Read access
par odd : odd parity bit.
par odd = 0 : the number of ones in the data word (D15:D1) is odd.
par odd = 1 : the number of ones in the data word (D15:D1) is even.

The address selects an internal register of the device; the RW bit selects the access mode.

RW = ‘0' The master performs a read access on the selected register. During the transmission of the next word, the slave sends the requested register value to MISO_G. The slave interprets the next word at MOSI_G as an address transfer.

RW = ‘1' The master performs a write access on the selected register. The slave stores the next transmitted word in the selected device register of MOSI_G and sends the actual register value in response to MOSI_G. The transmission goes on with an address transfer to MOSI_G and the address mode flags to MISO_G.

If the device is addressed by a nonexistent address it will respond with ´0´.

The next table shows the encoding scheme of a data value for a write access.

Data Transfer:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Dat14	Dat13	Dat12	Dat11	Dat10	Dat9	Dat8	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2	Dat1	Dat0	Par odd

dat[14:0] : data value for write access (15 Bit)
par odd : see Address Transfer

It is possible to combine the two access modes (write and read access) during one communication. The communication can be finished after last transmitted word of mixed access communication frame with CSN_G='1'. CSN_G must be '0' during mixed access communication frame.

SPI result values on MISO_G

Within SPI communication SCR1100 gyro ASIC sends Status Flags (Status/Config register value) and register result values on MISO_G. The following two tables show the encoding scheme:

Status Flags:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														s_ok	par odd

S_OK is generated out of the monitoring flags in the status register (08h).

Register Result:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
reg 14	reg 13	reg 12	reg11	reg 10	reg9	reg8	reg7	reg6	reg5	reg4	reg3	reg2	reg1	reg0	par odd

reg[14:0] : value of the internal register. All bits, which are not used, are set to zero.
par odd : see Address Transfer

Figure 6 shows an example of communication sequence:

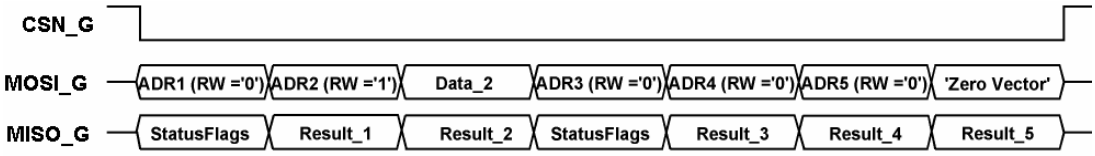

Figure 5. Communication example.

Each communication frame in the figure 6 contain 16 SCK cycles. After communication start (CSN_G falling edge) the master sends ADR1 and performs a read access. In parallel the slave sends Status Flags. During the transmission of the next data word (ADR2) the slave sends the register value of ADR1 (Result_1). On ADR2 the master performs a write access (RW='1'). The slave stores Data_2 in the register of ADR2 and sends the current register value of ADR2 to MISO_G. After the transmission of data value during a write access the slave always sends Status Flags. To receive Result_5 of the last read access the Master has to send an additional word ('Zero Vector').

4.1.2 SPI Transfer Parity Mode

SCR1100 gyro ASIC is able to support parity check during SPI Transfer. This functionality is controlled by the IC Identification Register. The internal parity status is reported in Status/Config Register.

With parity enable bit set the SCR1100 gyro ASIC is expecting an additional parity bit after the transmission of each 16 bit data word. This additional parity bit requires an additional SCK cycle, i.e. the SPI frame consists of 17 SCK cycles instead of the normal 16 SCK cycles. Detecting a wrong parity bit has the following consequences:

During read access:
The Parity Error Flag in the Status/Config Register is set. The SCR1100 reports the contents of the received register address.

During write access:
The Parity Error Flag in the Status/Config Register is set. The SPI Write Access is cancelled.
These actions are performed either if the parity failure is detected in the address word or the data word.

Due to the additional parity bit a single SPI Transfer is using now 17 Bit as shown in the Figure 7.

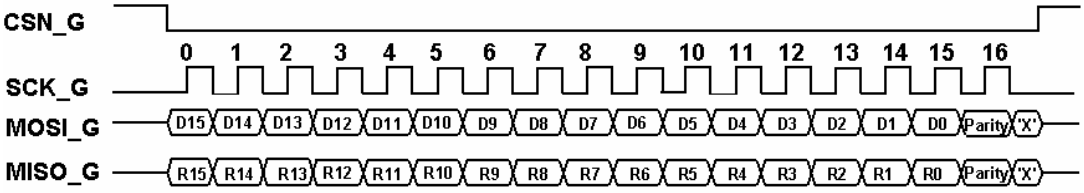

Figure 6. Communication in parity mode.

At the end of the data word the SPI master and the SPI slave have to add an additional parity bit. Both devices have to check the received parity according to the selected parity mode odd or even.

4.2 ASIC Addressing Space

4.2.1 Register Definition

The ASIC has multiple register and EEPROM blocks. The EEPROM blocks holding the calibration data will be programmed via SPI during manufacturing process. User only needs to access the Data Register Block at addresses 00h and 07h - 0Ah (addresses 01h-06h are reserved). The content of this register block is described below.

4.2.2 Data Register Block

Table 6. Register map of data register block.

Address Dec (hex)	Register Name [bit definition]	Number of Bits	Read/ Write/ Factory	Data Format	Description
00(00)	Rate_X[0]	1	R	-	odd Parity bit of Rate_X[14,1]
00(00)	Rate_X[1] (S_OK Flag)	1	R	-	S_OK =0 Rate_X failed S_OK =1 Rate_X valid (ok) S_OK is generated out of the monitoring flags in the status register (08h). If either one of the flags in register 08h [15:2] is 0, S_OK will be 0. Only if all flags in register 08h[15:2] are 1 S_OK is set to 1
00(00)	Rate_X[15:2]	14	R	S	Sensor output data format two's complement
07(07)	IC Identification [14, 11:4, 2, 1]	13	F	-	Reserved
07(07)	IC Identification []	1	r		Soft Reset bit Writing '1' to this register bit will reset the device
07(07)	IC Identification[12] HWParEn	1	W		Setting this bit to '1' is enabling the Parity functionality
07(07)	IC Identification[13] HWParSel	1	W		This bit is selecting an even or an odd parity mode. Bit = 0: Even Parity mode means that the number of ones in the data word including the parity bit is even. Bit = 1: Odd Parity mode means that the number of ones in the data word including the parity bit is odd.
08(08)	Status/Config [14:10, 8:1]	14	F	-	Reserved
08(08)	Status/Config[9] (Parity_OK)	1	R	-	This bit is set as soon as the SPI logic is detecting a wrong parity bit received from the µC. This bit is automatically cleared during read access to this register. Bit = 0 : Parity error Bit = 1 : Parity check ok.
09(09)	Reserved	14	F	-	Reserved
10(0A)	Temp[0]	1	R	-	odd Parity bit of TEMP[14,1]
10(0A)	Temp[1] (S_OK Flag)	1	R	-	S_OK =0 Rate_X failed S_OK =1 Rate_X valid
10(0A)	Temp[15,2]	14	R	S	Temperature sensor output

The offset of temperature data is factory calibrated but sensitivity of the temperature data varies from part to part. Note: Registers marked with F are reserved for factory use only and not to be written to.

4.2.3 Temperature Output Registers

The offset of temperature sensor is factory calibrated but sensitivity of the temperature data varies from part to part. The temperature doesn't reflect absolute ambient temperature.

Temperature data is in 2's complement format in 14 bits (15:2) of Temp register. To use the temperature sensor as an absolute temperature sensor or for additional system level compensations, the offset and sensitivity of the sensor should be measured and calibrated on system level

Temperature registers' typical output at +23 °C is -1755 counts and 1 °C change in temperature typically corresponds to 65 count change in temperature sensor output. Temperature information can be converted from decimals to [°C] as follows

$$Temp[^{o}C] = (Temp[LSB] + 3250)/65,$$

where Temp[°C] is temperature in Celsius and Temp[LSB] is temperature from TEMP registers in decimal format,

Temperature sensor offset calibration error at 25°C: ≤ ±15 °C
Temperature sensor sensitivity calibration error : ≤ 5%

Application Information

4.3 Pin Description

The pin out for SCR1100 is presented in Figure 7 (pin descriptions can be found from Table 7).

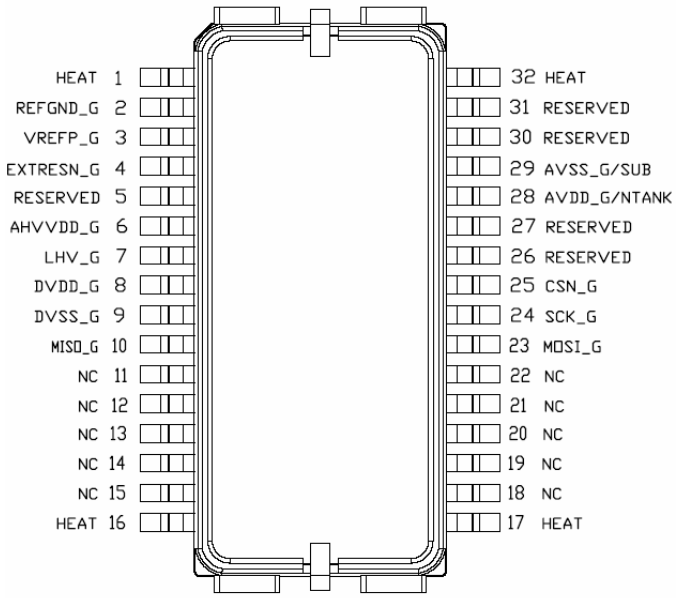

Figure 7. SCR1100 pinout diagram.

Table 7. SCR1100 pin descriptions.

pin #	Name	Type 1)	PD/PU/HV 3)	Description
1	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
2	REFGND_G	AI		Analog reference ground should be connected external to AVSS_G
3	VREFP_G	AO		External C for positive reference voltage and output pin for use as supply for external load. Max load current compare section TBD. Note this voltage can only be used as supply for analog circuits. Circuits that produce high current spikes due to switching circuit can not be driven by this node.
4	EXTRESN_G	DI	PU	External Reset, 3.3V level Schmitt-trigger input with internal pull-up, High low transition cause system restart
5	RESERVED	R		Factory used only, leave floating
6	AHVVDDS_G	AO	HV (~30V)	External C for high voltage analog supply, high voltage pad ≈30V
7	LHV	AI		Connection for inductor for high voltage generation, high voltage pad ≈30V
8	DVDD_G	AI		Digital Supply Voltage
9	DVSS_G	AI		Digital Supply Return, external connected to AVSS_G
10	MISO_G	DOZ		Data Out of SPI Interface, 3.3V level, Level definition see SPI-section
11	NC	NC		Not connected, connect to GND or leave floating.
12	NC	NC		Not connected, connect to GND or leave floating.
13	NC	NC		Not connected, connect to GND or leave floating.
14	NC	NC		Not connected, connect to GND or leave floating.
14	NC	NC		Not connected, connect to GND or leave floating.
15	NC	NC		Not connected, connect to GND or leave floating.
16	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
17	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
18	NC	NC		Not connected, connect to GND or leave floating.
19	NC	NC		Not connected, connect to GND or leave floating.
19	NC	NC		Not connected, connect to GND or leave floating.
20	NC	NC		Not connected, connect to GND or leave floating.
21	NC	NC		Not connected, connect to GND or leave floating.
22	NC	NC		Not connected, connect to GND or leave floating.
23	MOSI_G	DI	PD	Data In of SPI Interface, 3.3V level Schmitt-trigger input

pin #	Name	Type 1)	PD/PU/HV 3)	Description
24	SCK_G	DI	PD	Clk Signal of SPI Interface, 3.3V level Schmitt-trigger input, Input Clock range 2 to 8MHz. Level definition see SPI-section
25	CSN_G	DI	PU	Chip Select of SPI Interface, 3.3V level Schmitt-trigger input, Input Clock range 2 to 8MHz. Level definition see SPI-section
26	RESERVED	R		Factory used only, leave floating
27	RESERVED	R		Factory used only, leave floating
28	AVDD_G	AI		Analog Supply voltage
29	SUB	AI		Connected external to AVSS_G
30	RESERVED	R		Factory used only, leave floating
31	RESERVED	R		Factory used only, leave floating
32	HEAT	A1		Heat sink connection, externally connected to AVSS_G.

Notes:
1) A=Analog, D=Digital, I=Input, O=Output, Z=Tristate Output, R = Reserved
3) PU=internal pullup, PD=internal pulldown, HV = high voltage

4.4 Application Circuitry and External Component Characteristics

See recommended schematics in Figure 8. Component characteristics are presented in Table 8.

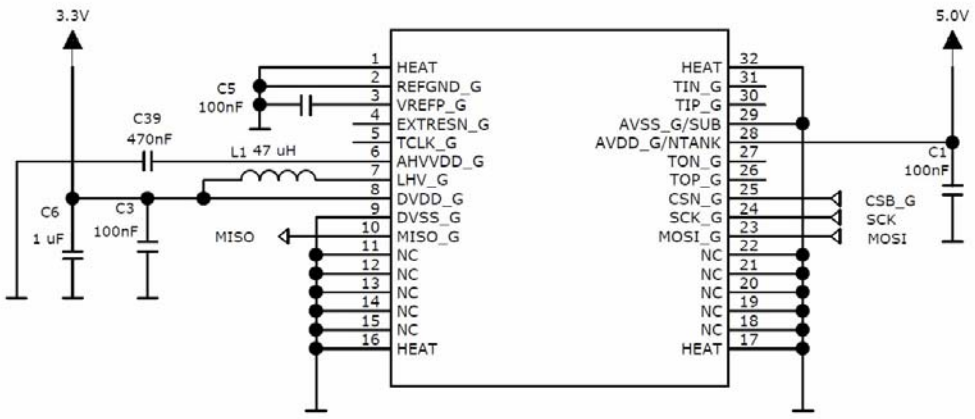

Figure 8. SCR1100 recommended circuit diagram.

Optional filtering recommendations for better PSRR (Power Supply Rejection Ratio) is presented in Figure 9. Please note that PSSR filtering is optional and not required if the 3.3V power supply is already stabile enough. RC filtering (R1 & C7 without L2) could also be sufficient for most cases.

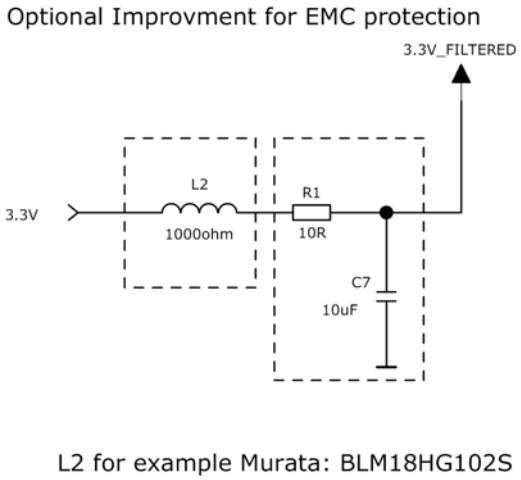

Figure 9. Optional filtering recommendation to improve PSRR if required.

4.4.1 Separate Analog and Digital Ground Layers with Long Power Supply Lines

If power supply routings/cablings are long separate ground cabling, routing and layers for analog and digital supply voltages should be used to avoid excessive power supply ripple.

In the recommended circuit diagram Figure 8 and layout Figure 11 joint ground is used as it is the simplest solution and is adequate as long as the supply voltage lines are not long (when connecting the SCR1100 directly to µC on the same PCB).

Table 8. SCR1100 external components.

Component	Parameter	Min	Typ	Max	Units
C1, C3, C5	Capacitance	70	100	130	nF
	ESR @ 1 MHz			100	mΩ
	ESL			TBD	nH
	Voltage rating	7			V
C39	Capacitance	376	470	564	nF
	ESR @ 1 MHz			100	mΩ
	ESL			TBD	nH
	Voltage rating	30			V
L1	Inductance	37	47	57	µH
	ESR L=47 µH			5	Ω
	Voltage rating	30			V
C6	Capacitance	0.7	1	1.3	µF
	ESR @ 1 MHz			100	mΩ
	ESL			TBD	nH
Optional for better PSRR:					
R1	Resistance		10		Ω
C7	Capacitance		4.7		µF
L2	Impedance		1k		Ω

4.5 Boost Regulator and Power Supply Decoupling in Layout

Recommended layout for DVDD_G/LHV pin decoupling is shown in Figure 10.

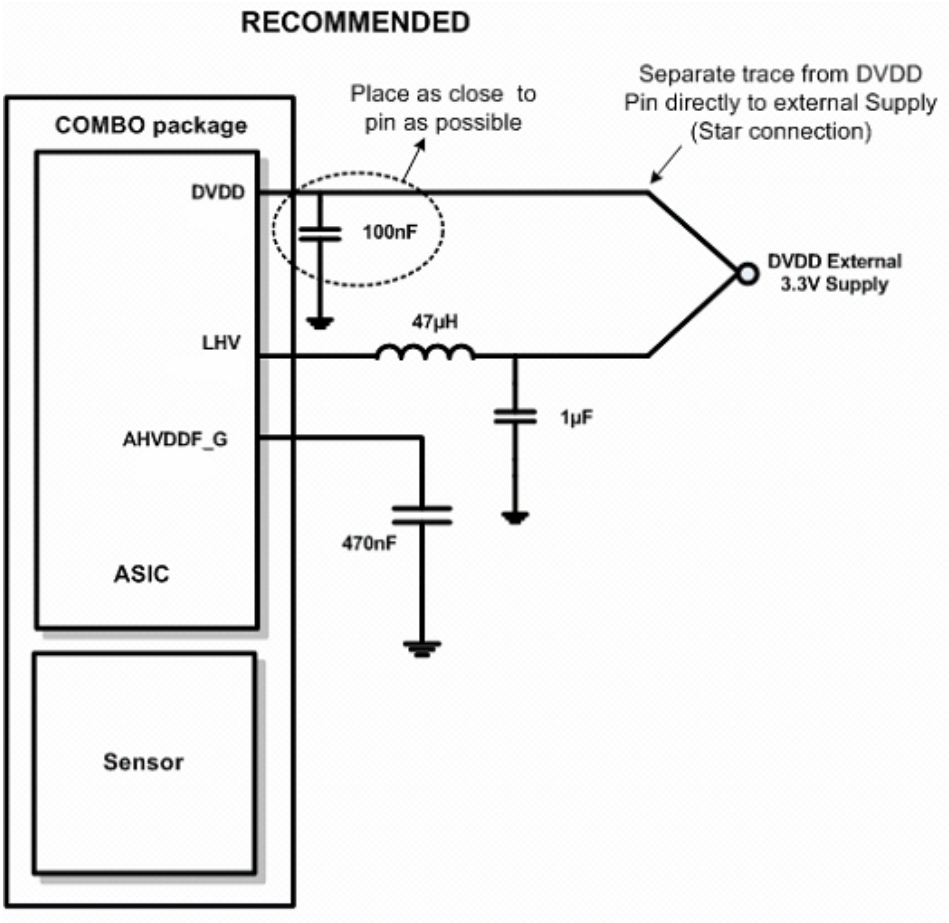

Figure 10. Layout recommendations for DVDD_G/LHV pin decoupling.

4.5.1 Layout Example

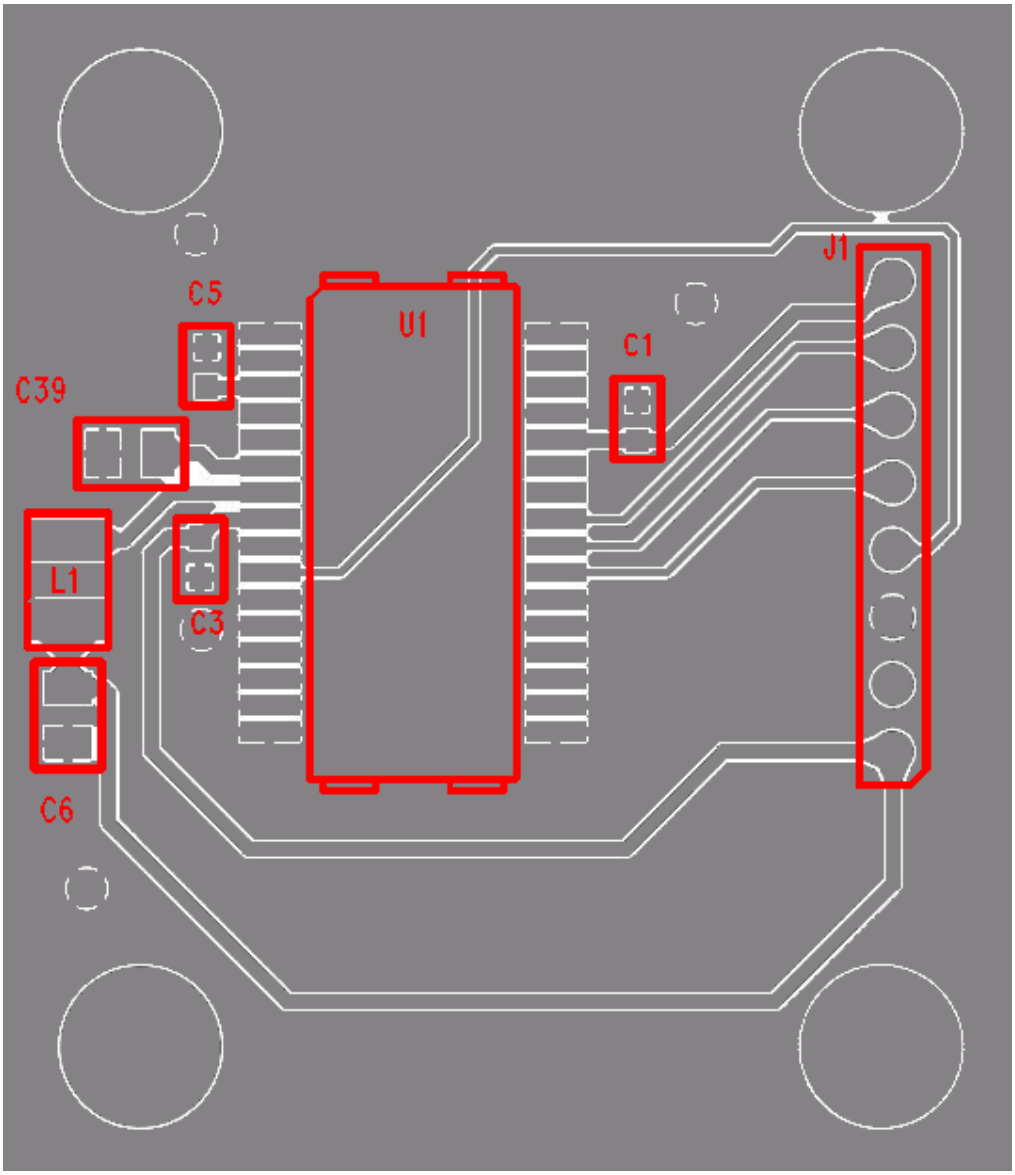

Figure 11. Example layout for SCR1100.

4.5.2 Thermal Connection

The component includes heat sink pins to transfer the internally generated heat from the package to outside. The thermal resistance to ambient should be low enough not to self heat the device. If the internal junction temperature gets too high compared to ambient, that may lead to out of specification behaviour.

Table 9. Thermal resistance.

Component	Parameter	Min	Typ	Max	Units
Thermal resistance Θ_{JA}	Total resistance from junction to ambient			50	°C/W

4.6 Measurement Axis and Directions

The SCR1100 angular rate measurement direction is shown below in Figure 12.

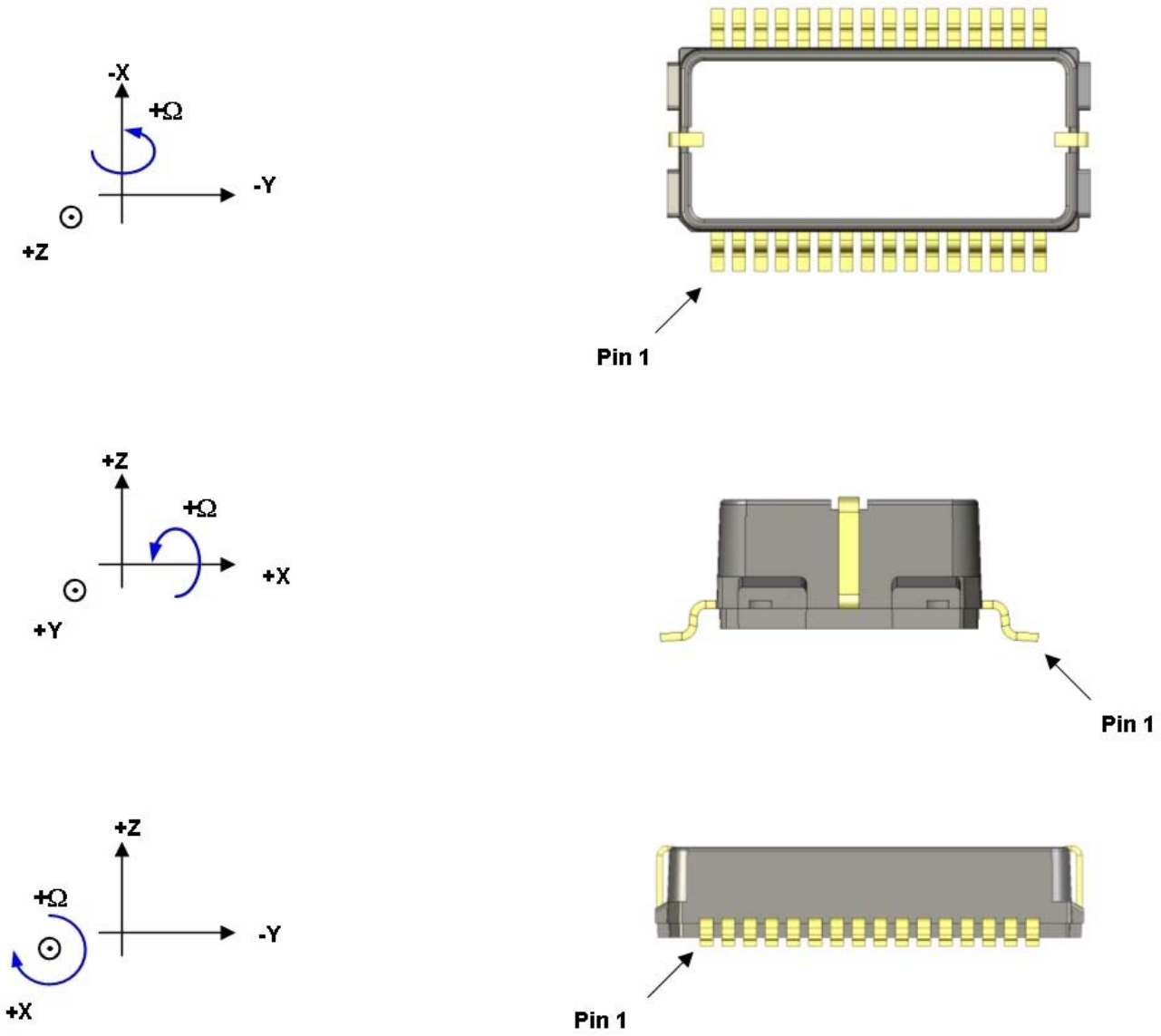

Figure 12. SCR1100 angular rate measurement direction.

4.7 Package Characteristics

4.7.1 Package Outline Drawing

The SCR1100 package outline and dimensions are presented in Figure 13 and Table 10.

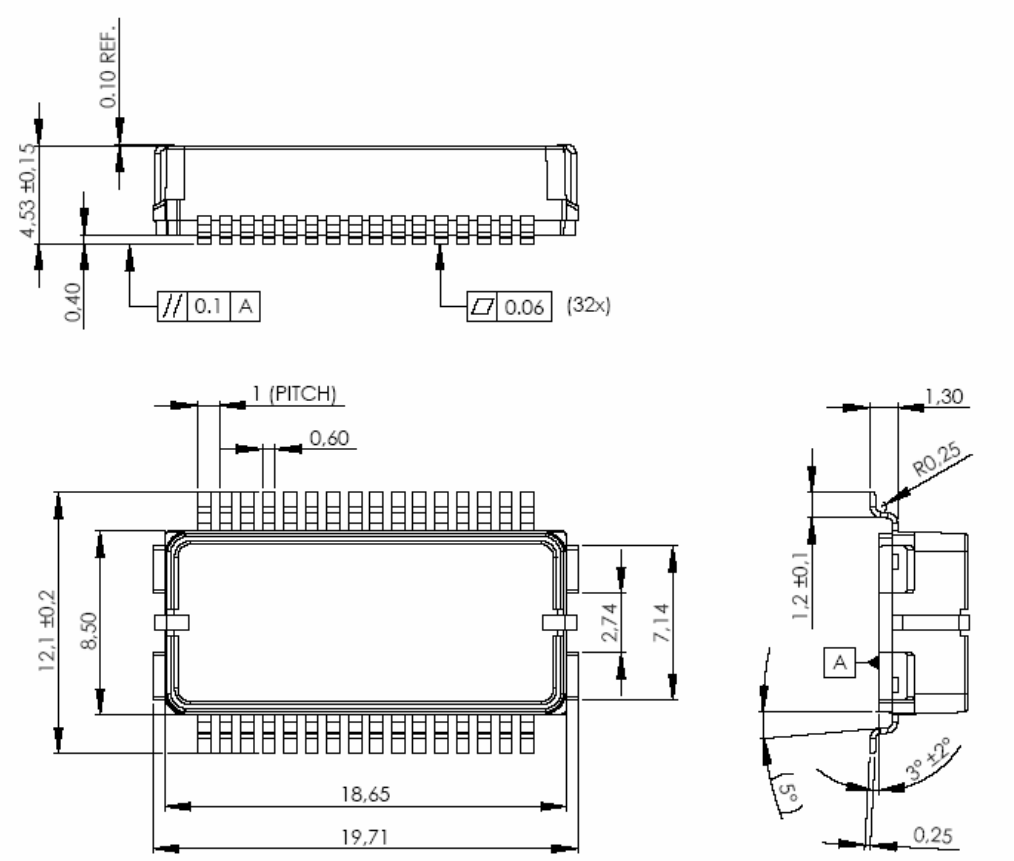

Figure 13. SCR1100 package outline and dimensions.

Table 10. SCR1100 package dimensions.

Component	Parameter	Min	Typ	Max	Units
Length	Without leads		19.71		mm
Width	Without leads		8.5		mm
Width	With leads		12.1		mm
Height	With leads (including stand-off and EMClead)		4.53		mm
Lead pitch			1.0		mm

4.7.2 PCB Footprint

SCR1100 footprint dimensions are presented in Figure 14 and Table 11.

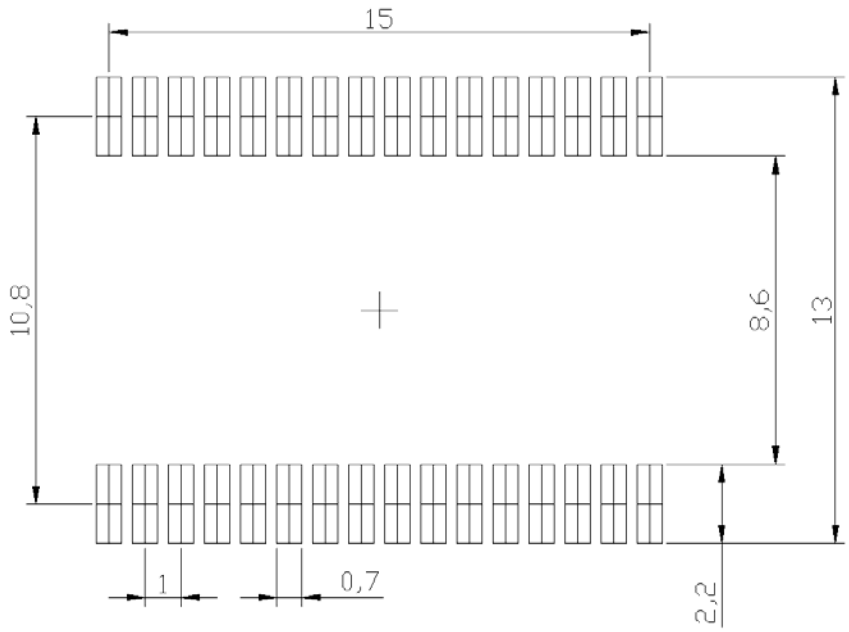

Figure 14. SCR1100 footprint.

Table 11. SCR1100 footprint dimensions.

Component	Parameter	Min	Typ	Max	Units
Footprint length	Without lead footprints		15.7		mm
Footprint width	Without lead footprints		13.0		mm
Footprint lead pitch	Long side leads		1.0		mm
Footprint lead length			2.20		mm
Footprint lead width	Long side leads		0.7		mm

4.8 Assembly instructions

Please refer to "Technical Note 82" document for assembly instructions.

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