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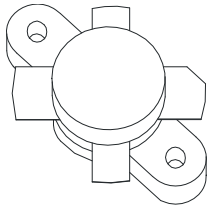
SD2931-10

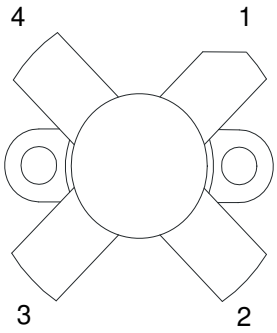
RF power transistor: HF/VHF/UHF N-channel power MOSFETs

Datasheet - production data



M174
Epoxy sealed

Figure 1. Pin connection



1. Drain
2. Source
3. Gate
4. Source

- P_{OUT} = 150 W min. with 14 dB gain @ 175 MHz
- Thermally enhanced packaging for lower junction temperatures

Description

The SD2931-10 is a gold metalized N-channel MOS field-effect RF power transistor. Being electrically identical to the standard SD2931 MOSFET, it is intended for use in 50 V dc large signal applications up to 230 MHz.

The SD2931-10 is mechanical compatible to the SD2931 but offers in addition a better thermal capability (25% lower thermal resistance), representing the best-in-class transistors for ISM applications, where reliability and ruggedness are critical factors.

Features

- Gold metalization
- Excellent thermal stability
- Common source configuration

Table 1. Device summary

Order code	Marking	Base qty.	Package	Packaging[1]
SD2931-10W	SD2931-10	25 pcs	M174	Plastic tray

1. For more details please refer to *Chapter 11: Marking, packing and shipping specifications*.

Contents

1 Electrical data

1.1 Maximum ratings

(T_{CASE} = 25 °C).

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$ (1)	Drain source voltage	125	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1 MΩ)	125	V
V_{GS}	Gate-source voltage	±40	V
I_D	Drain current	20	A
P_{DISS}	Power dissipation	389	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1. T_J = 150°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.45	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C).

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0	I_{DS} = 100 mA		125			V
I_{DSS}	V_{GS} = 0	V_{DS} = 50 V				50	µA
IGSS	V_{GS} = 20	V_{DS} = 0				250	nA
$V_{GS(Q)}$ (1)	V_{DS} = 10 V	I_D = 250 mA		See table below			V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 10 A				3.0	V
G_{FS}	V_{DS} = 10 V	I_D = 5 A		5	6		mho
C_{ISS}	V_{GS} = 0	V_{DS} = 50 V	f = 1 MHz		480		pF
C_{OSS}	V_{GS} = 0	V_{DS} = 50 V	f = 1 MHz		190		pF
CRSS	V_{GS} = 0	V_{DS} = 50 V	f = 1 MHz		18		pF

1. $V_{GS(Q)}$ sorted with alpha/numeric code marked on unit.

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 50 V I_{DQ} = 250 mA f = 175 MHz	150			W
G_{PS}	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175 MHz	14	15		dB
n_D	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175 MHz	55	65		%
Load mismatch	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175 MHz All phase angles	10:1			VSWR

Table 6. V_{GS} sorts

Symbol	Value	Symbol	Value
A	2.0 - 2.1	K	2.9 - 3.0
B	2.1 - 2.2	L	3.0 - 3.1
C	2.2 - 2.3	M	3.1 - 3.2
D	2.3 - 2.4	N	3.2 - 3.3
E	2.4 - 2.5	P	3.3 - 3.4
F	2.5 - 2.6	Q	3.4 - 3.5
G	2.6 - 2.7	R	3.5 - 3.6
H	2.7 - 2.8	S	3.6 - 3.7
J	2.8 - 2.9		

3 Transient thermal impedance

Figure 2. Transient thermal impedance

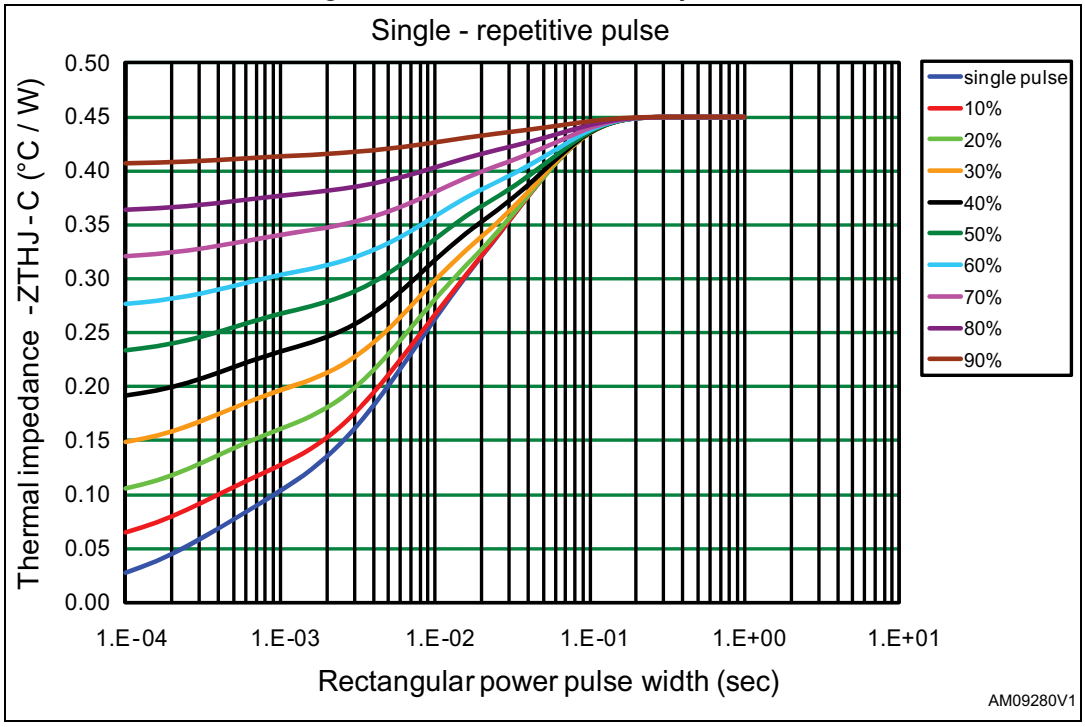
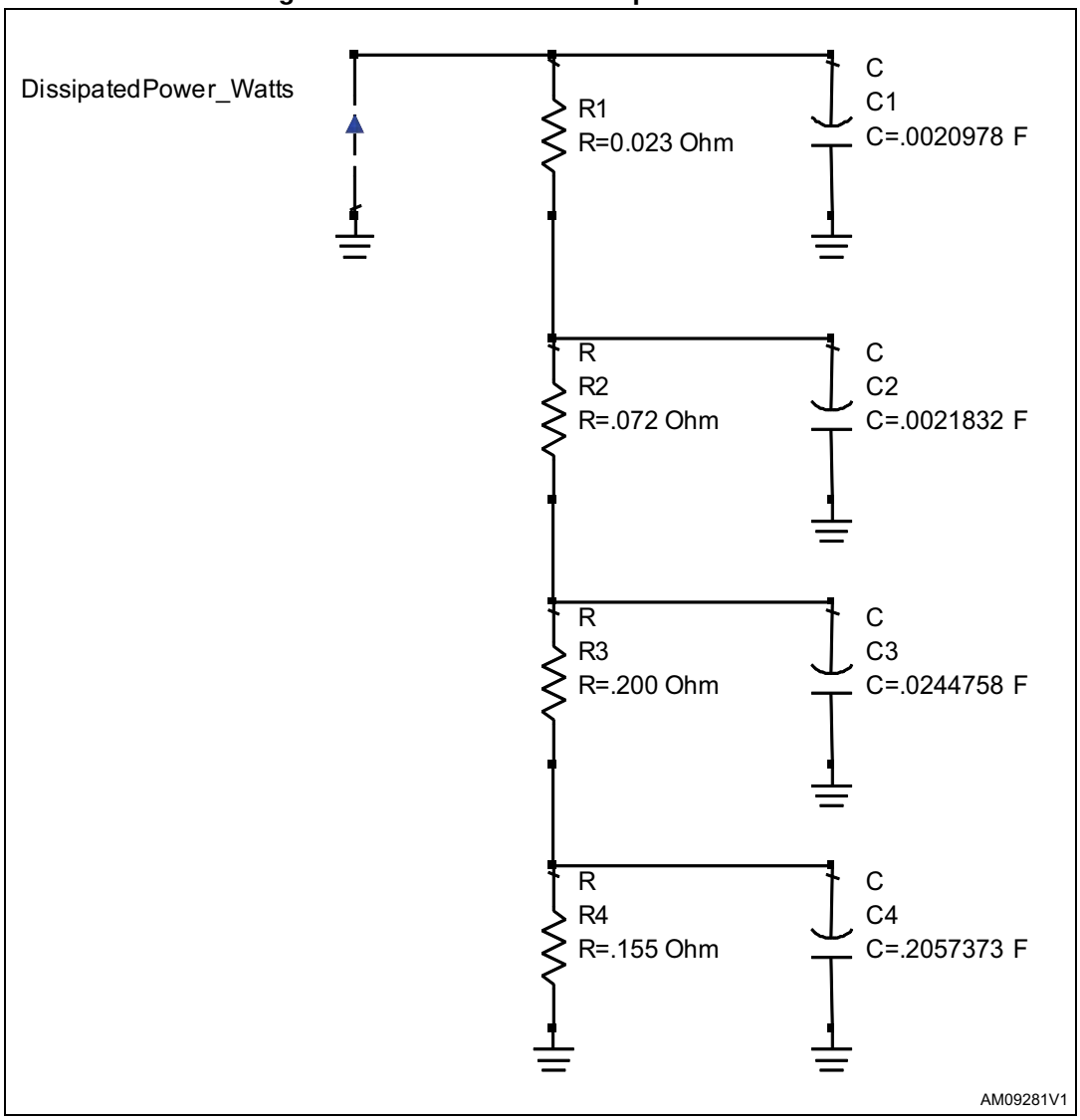


Figure 3. Transient thermal impedance model



4 Impedance data

Figure 4. Impedance data

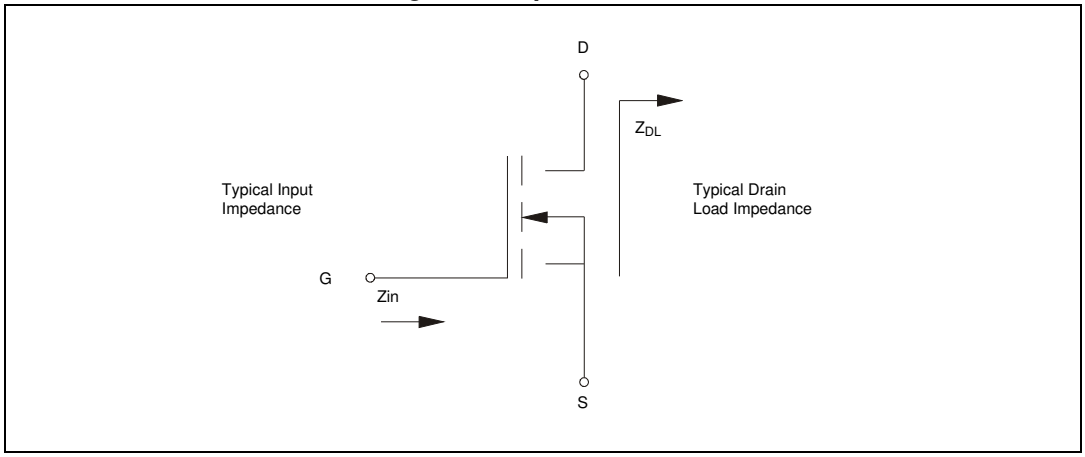


Table 7. Impedance data

Freq	Z_{IN} (Ω)	Z_{DL} (Ω)
30 MHz	1.7 - j 5.7	6.8 + j 0.9
175 MHz	1.2 - j 2.0	2.0 + j 2.4

5 Typical performance

Figure 5. Capacitance vs drain-source voltage

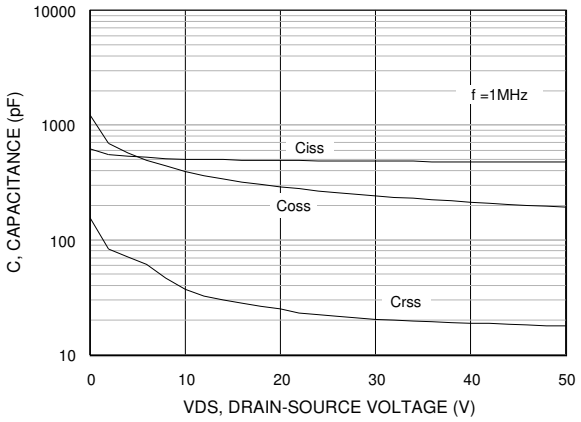


Figure 6. Drain current vs gate voltage

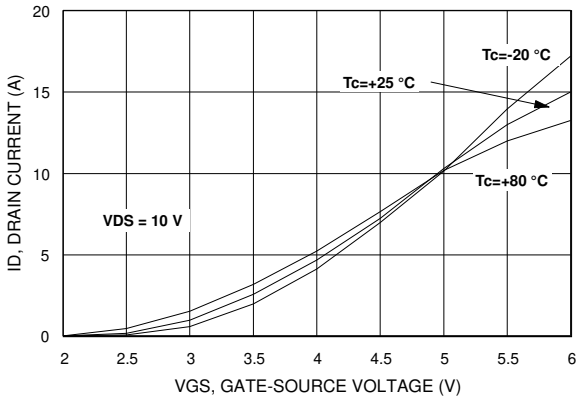


Figure 7. Gate-source voltage vs case temperature

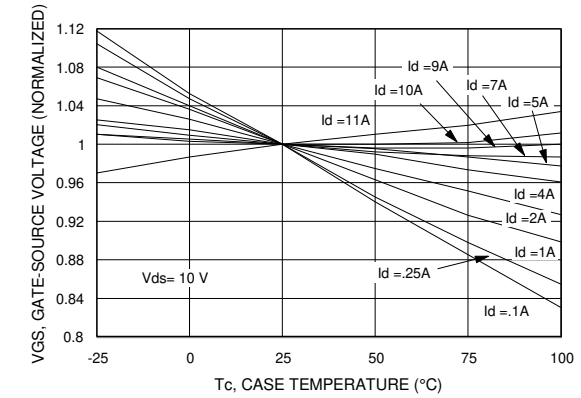


Figure 8. Maximum thermal resistance vs case temperature

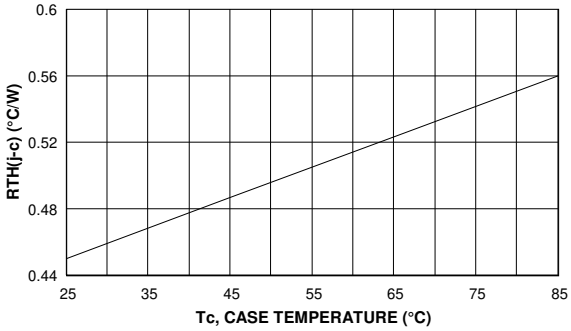
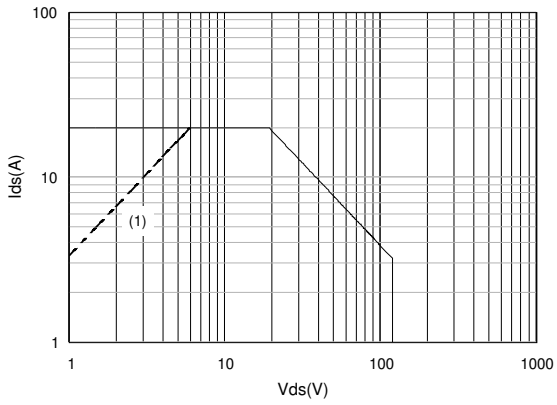


Figure 9. Safe operating area



(1) Current in this area may be limited by $R_{ds(on)}$

6 Typical performance @ 175 MHz

Figure 10. Output power vs input power

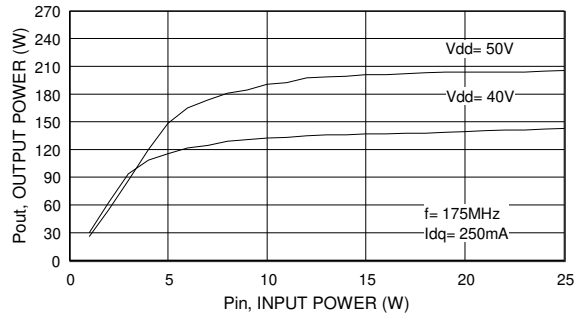


Figure 11. Output power vs input power

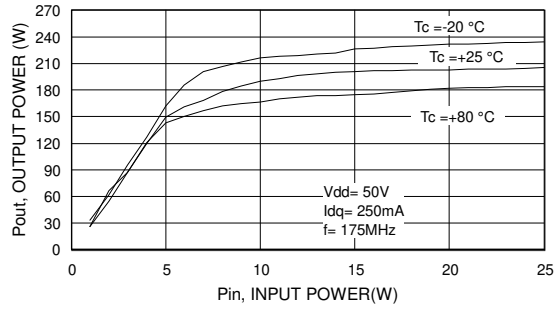


Figure 12. Power gain vs output power

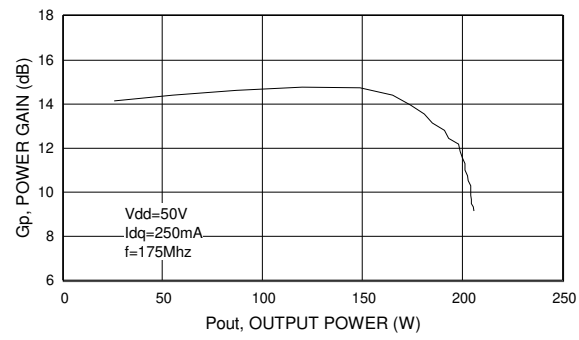


Figure 13. Efficiency vs output power

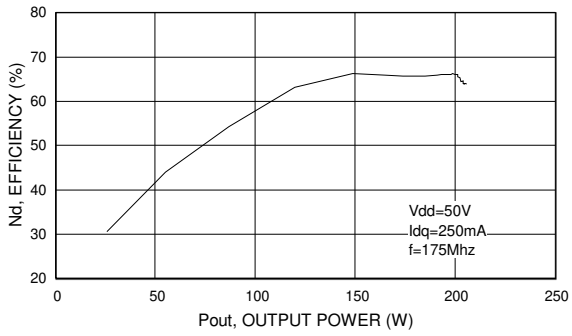


Figure 14. Output power vs supply voltage

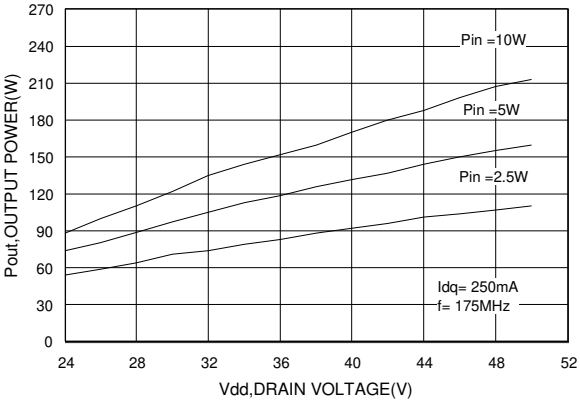
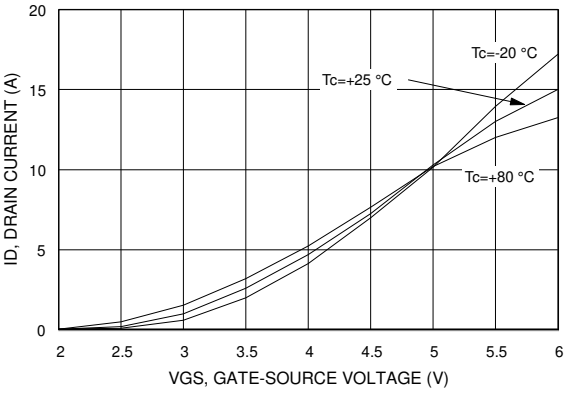
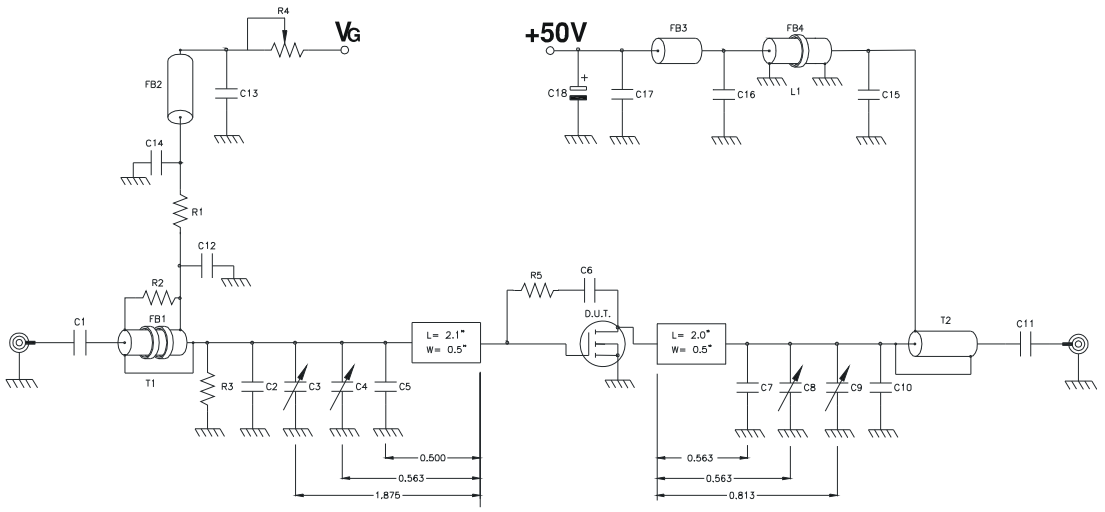


Figure 15. Drain current vs gate-source voltage



7 Test circuit

Figure 16. 175 MHz schematic (production test circuit)



Note: All dimensions in inches

REF. 1021579C

Table 8. Component part list

Component	Description
T1	4:1 transformer, 25 ohm flexible coax .090 OD 6” long
T2	1:4 transformer, 25 ohm semi-rigid coax .141 OD 6” long
FB1	Toroid X 2, 0.5” OD .312” ID 850µ 2 turns
FB2, FB3	VK200
FB4	Shield bead, 1” OD 0.5” ID 850µ 3 turns
L1	1/4 wave choke, 50 ohm semi-rigid coax .141 OD 12” Long
PCB	0.62” woven fiberglass, 1 oz. copper, 2 sides, εr = 2.55
R1, R3	470 ohm 1 W chip resistor
R2	360 ohm 1/2 W resistor
R4	20 Kohm 10 turn potentiometer
R5	560 ohm 1 W resistor
C1, C11	470 pF ATC chip cap
C2	43 pF ATC chip cap
C3, C8, C9	Arco 404, 12-65 pF
C4	Arco 423, 16-100 pF

Table 8. Component part list (continued)

Component	Description
C5	120 pF ATC chip cap
C6	0.01 µF ATC chip cap
C7	30 pF ATC chip cap
C10	91 pF ATC chip cap
C12, C15	1200 pF ATC chip cap
C13, C14,C16, C17	0.01 µF / 500 V chip cap
C18	10 µF 63 V electrolytic capacitor

Figure 17. 175 MHz test circuit photomaster

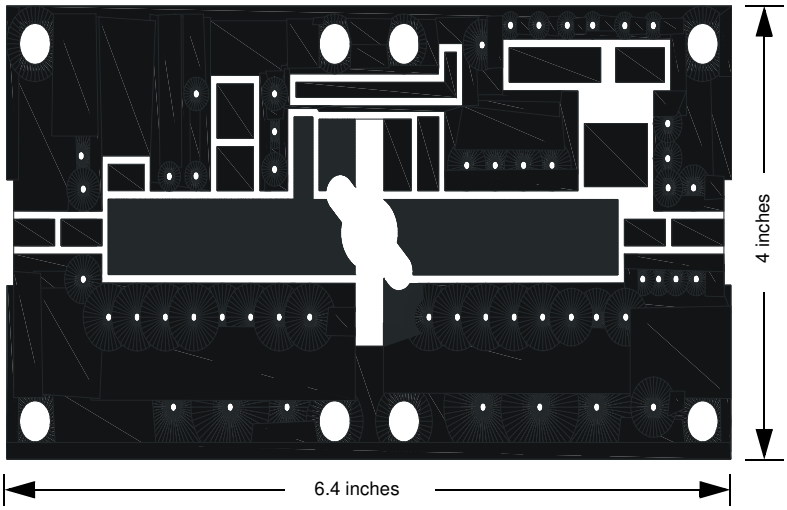
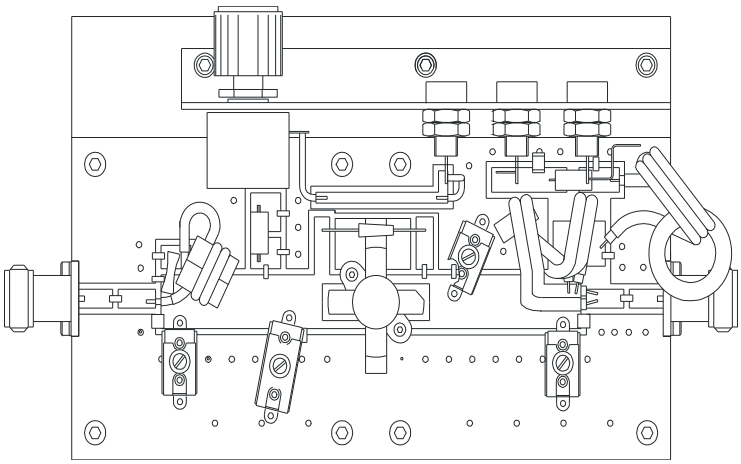


Figure 18. 175 MHz test circuit



8 Typical performance @ 30 MHz

Figure 19. Output power vs input power

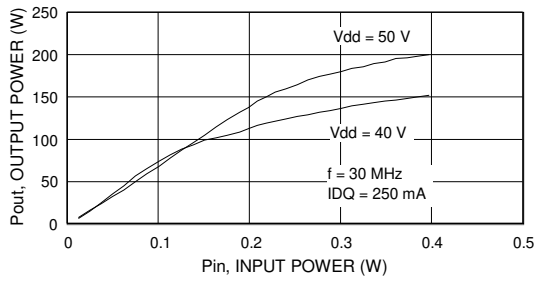


Figure 20. Power gain vs output power

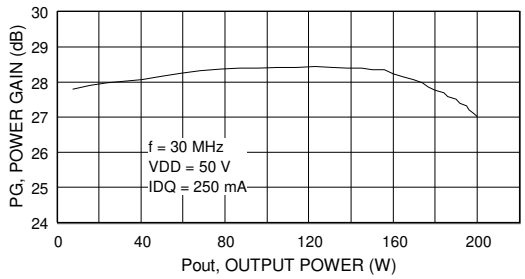


Figure 21. Efficiency vs output power

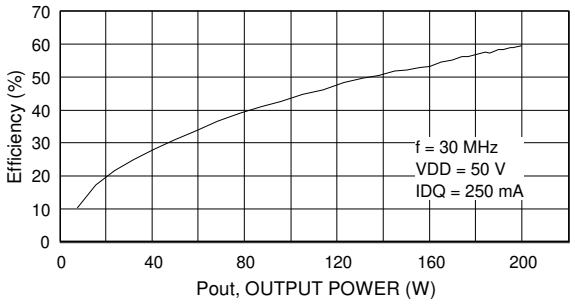


Figure 22. Output power vs supply voltage

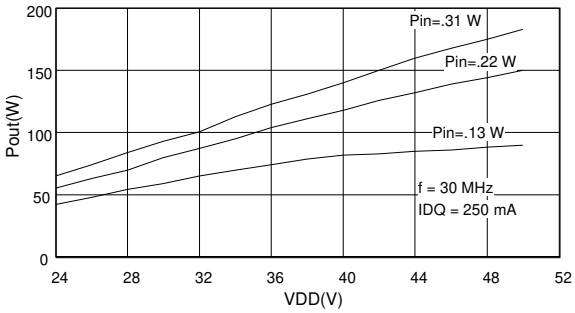
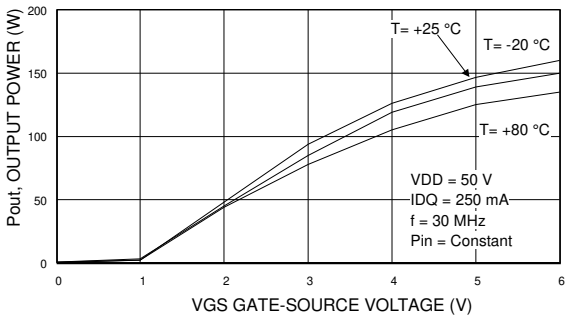


Figure 23. Output power vs gate voltage



9 Test circuit @ 30 MHz

Figure 24. 30 MHz test circuit schematic (engineering test circuit)

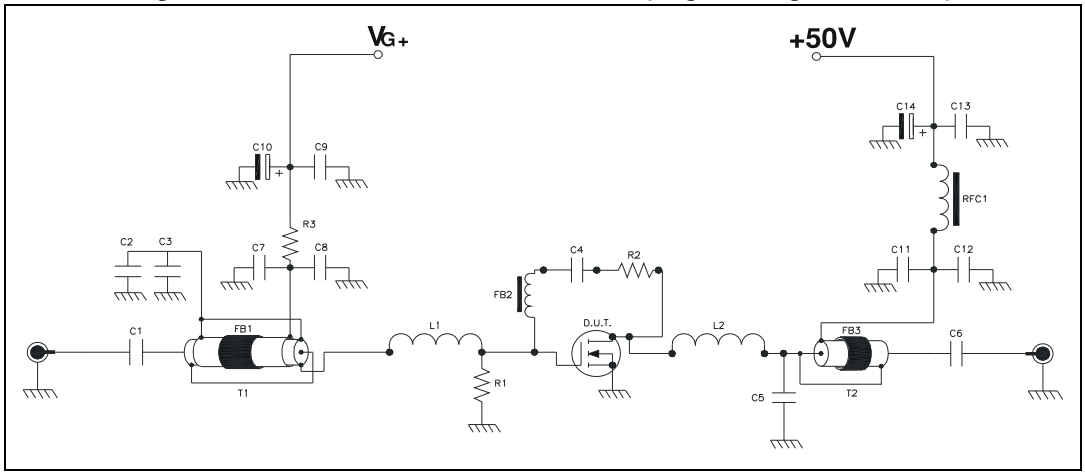


Figure 25. 30 MHz test circuit part list

Symbol	Description
T1	9:1 transformer, 25 Ω flexible coax with extra shield .090 OD 15” long
T2	1:4 transformer, 50 Ω flexible coax .225 OD 15” long
FB1	Toroid 1.7” OD .30” ID 220 µ 4 turns
FB2	Surface mount EMI shield bead
FB3	Toroid 1.7” OD .300” ID 220µ 3 turns
RFC1	Toroid 0.5” OD 0.30” ID 125µ 4 turns 12 awg wire
PCB	0.62” woven fiberglass, 1 oz. Copper, 2 Sides, εr = 2.55
R1, R3	1 KΩ 1 W chip resistor
R2	680 Ω 3 W wirewound resistor
C1,C4,C6,C7,C8, C9, C11,C12,C13	0.1 µF ATC chip cap
C2, C3	750 pF ATC chip cap
C5	470 pF ATC chip cap
C10	10 µF 63 V electrolytic capacitor
C14	100 µF 63 V electrolytic capacitor

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 26. M174 (0.500 DIA 4/L N/HERM W/FLG) package outline

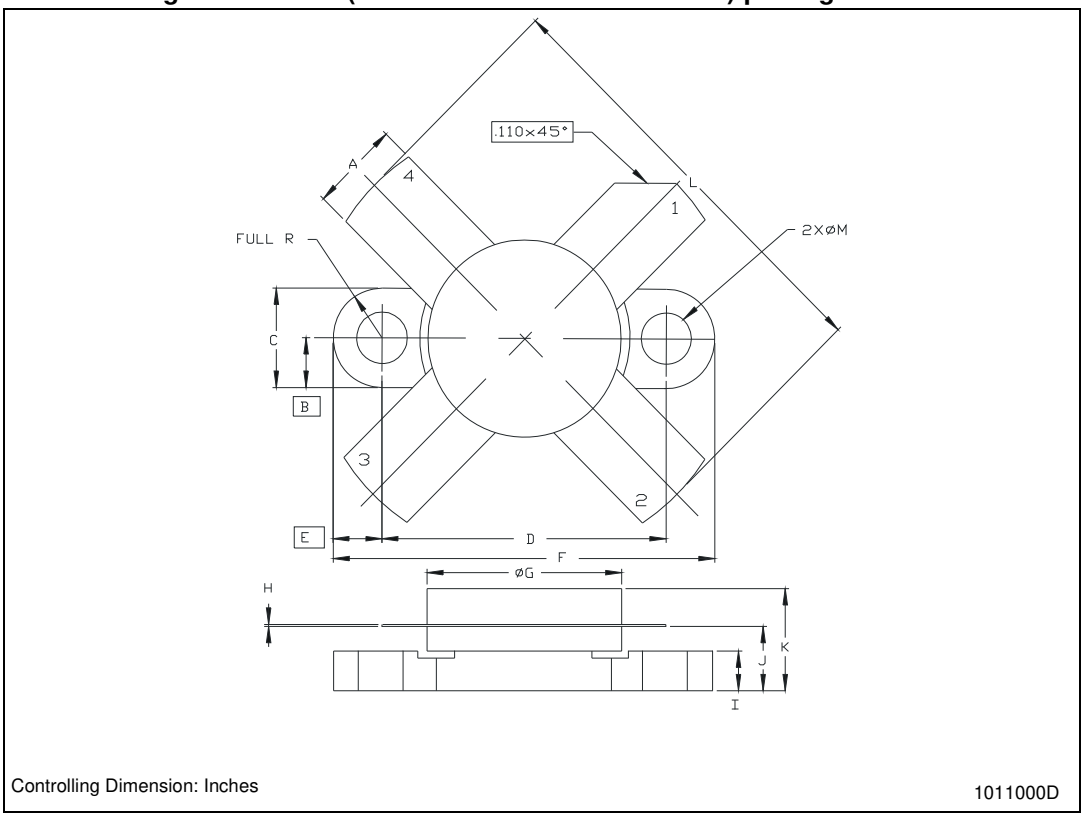


Table 9. M174 (0.500 DIA 4/L N/HERM W/FLG) package mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.56		5.584	0.219		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.11		3.00	0.083		0.118
J	3.81		4.45	0.150		0.175
K			7.11			0.280
L	25.53		26.67	1.005		1.050
M	3.05		3.30	0.120		0.130

11 Marking, packing and shipping specifications

Table 10. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	V_{GS}	Lot code
SD2931-10W	Plastic tray	25	< 10 %	Not mixed	Not mixed

Figure 27. Marking drawing

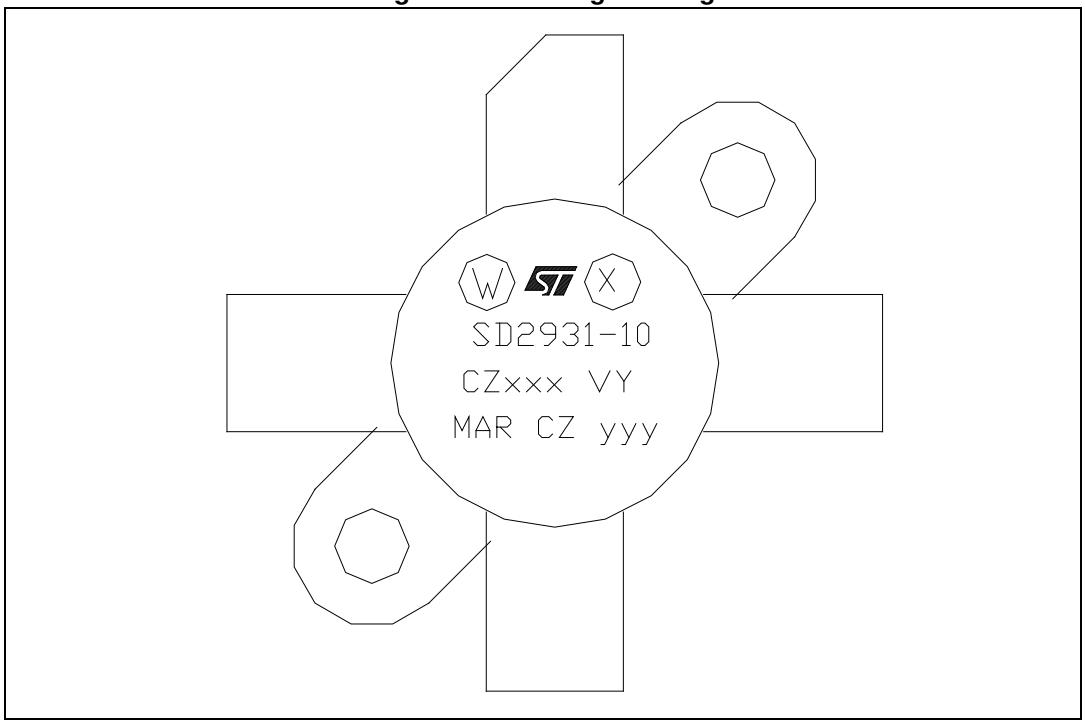


Table 11. Marking specifications

Symbol	Description
W	Wafer process code
X	V_{GS} sort
CZ	Assembly plant
xxx	Last 3 digit of diffusion lot
VY	Diffusion plant
MAR	County of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

12 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Sep-2004	4	
17-Jun-2004	5	Updated *Table 5: Dynamic on page 4*
04-Mar-2008	6	Updated *Table 4: Static (per side), Table 5: Dynamic* and *Table 6: VGS sorts on page 5*
08-Feb-2011	7	Inserted *Chapter 11: Marking, packing and shipping specifications.*
12-Jan-2012	8	Inserted *Chapter 3: Transient thermal impedance.*
19-Dec-2012	9	Updated *Table 10: Packing and shipping specifications*
14-Jul-2016	10	Updated V_{GS} value in *Table 2: Absolute maximum ratings*.