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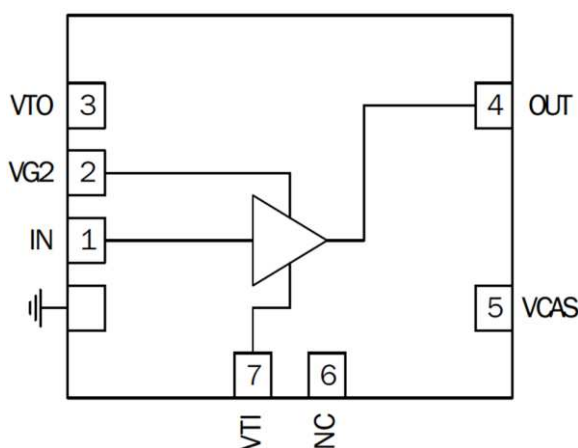
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# SDA-1000

## GaAs Distributed Amplifier

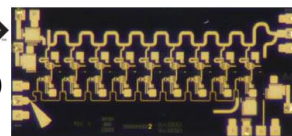
RFMD's SDA-1000 is a directly coupled (DC) GaAs microwave monolithic integrated circuit (MMIC) distributed driver amplifier die designed to support a wide array of high frequency commercial, military, and space applications. They are ideal for wideband amplifier gain blocks, broadband test equipment (ATE), military, and aerospace applications.



Functional Block Diagram

rfmd

SDA-1000



Package: Die, 3.1mm x 1.45mm x 0.102mm

### Features

- DC to 20GHz Operation
- +26dBm  $P_{3dB}$
- Gain = 14dB Typical
- Noise Figure = 4dB
- Output Voltage to  $8V_{PP}$
- 300mA Total Current

### Applications

- Military
- Aerospace
- Broadband ATE
- Instrumentation

### Ordering Information

SDA1000	GaAs Distributed Amplifier, GelPak, 10 pieces or more
SDA1000SB	GaAs Distributed Amplifier, GelPak, 2 pieces

## Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Bias Voltage ( $V_{DD}$ )	+9.0	$V_{DC}$
Gate Bias Voltage ( $V_{TI}$ )	-2 to 0	$V_{DC}$
Gate Bias Voltage ( $V_{G2}$ )	$(V_{DD} - 8.0) V_{DC}$ to $V_{DD}$	V
RF Input Power ( $V_{DD} = +8.0V_{DC}$ )	20	dBm
Operating Channel Temperature ( $T_J$ )	+175	°C
Continuous Power Dissipation ( $T = +85^{\circ}C$ )	3.5	W
Thermal Resistance (Pad to Die Bottom)	25	°C/W
Storage Temperature	-40 to +150	°C
Operating Temperature	-40 to +85	°C
ESD JESD22-A114 Human Body Model (HBM)	Class 0 (All Pads)	



**Caution!** ESD sensitive device.



RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

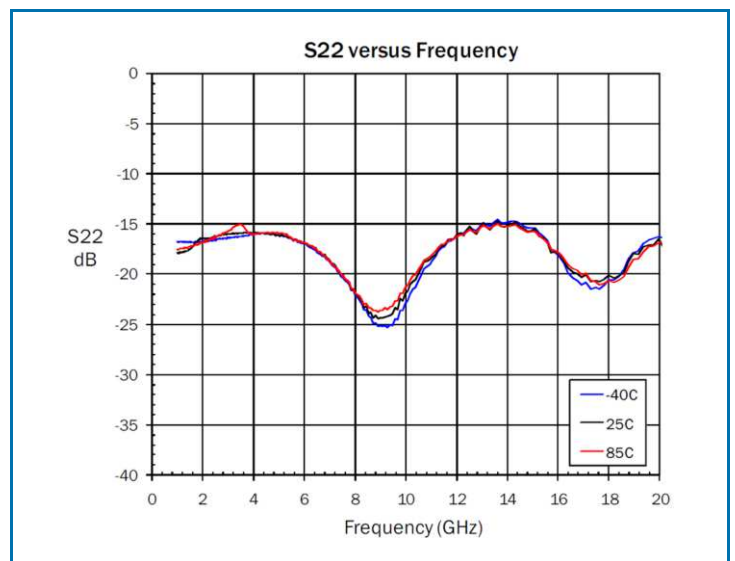
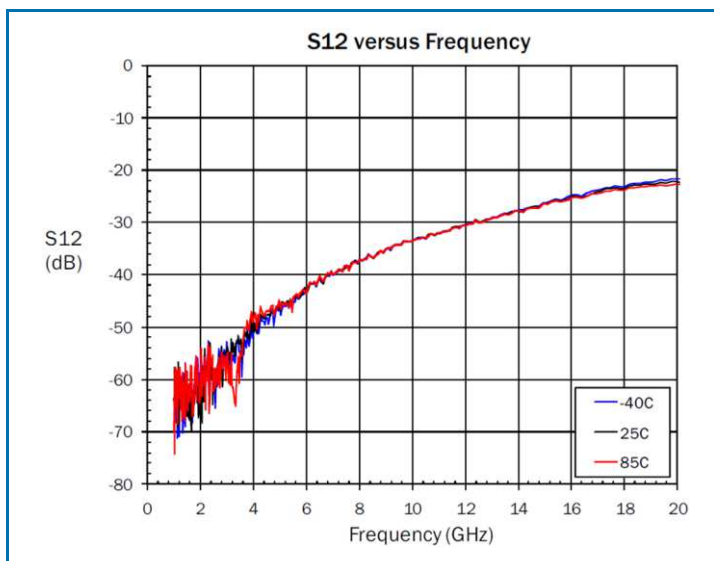
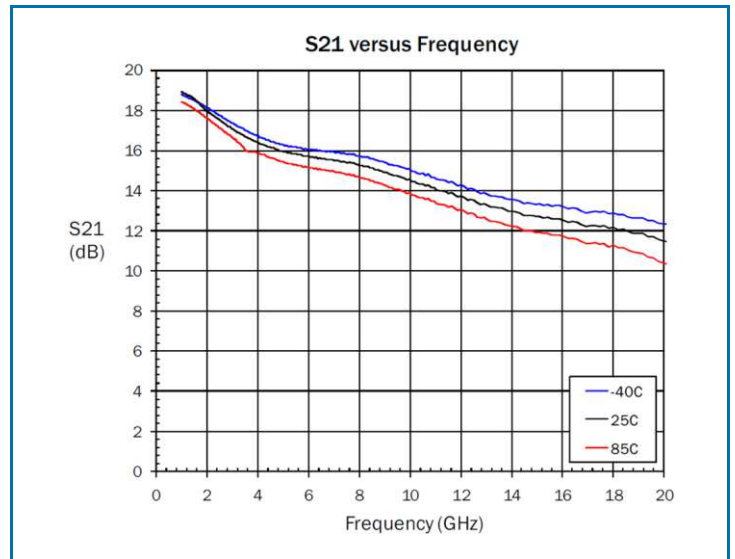
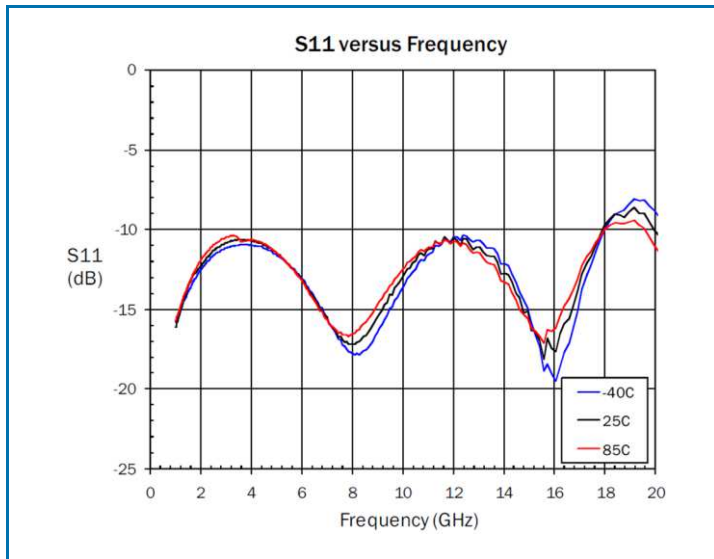
## Nominal Operating Parameters

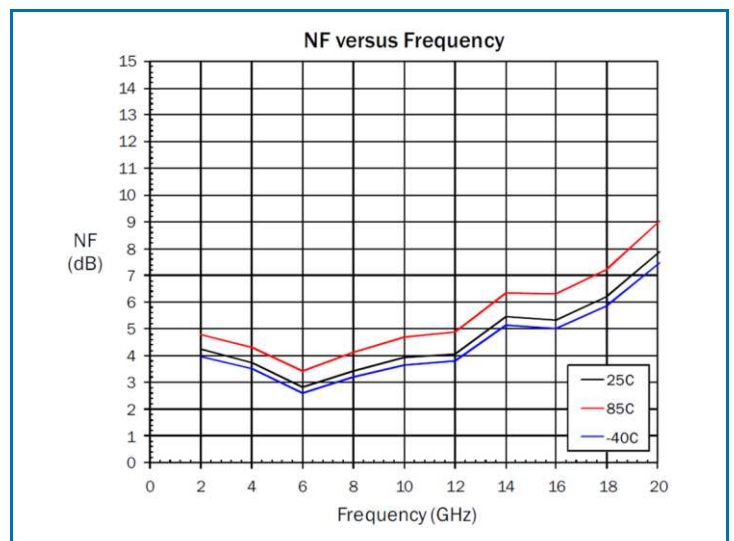
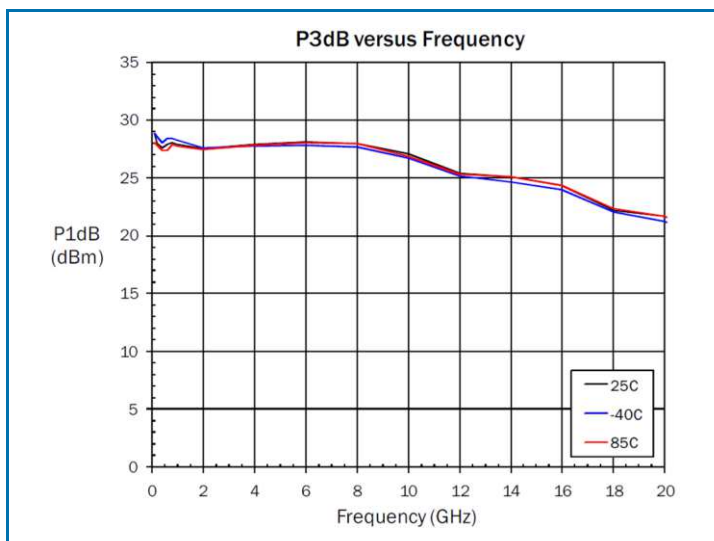
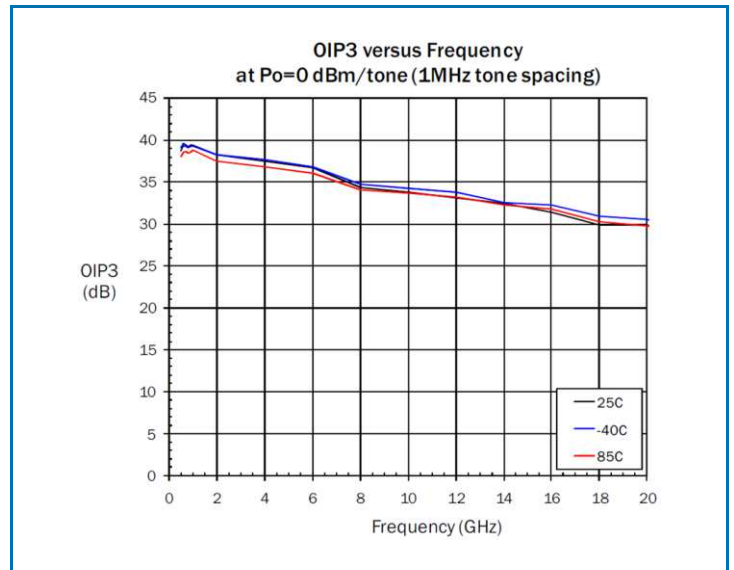
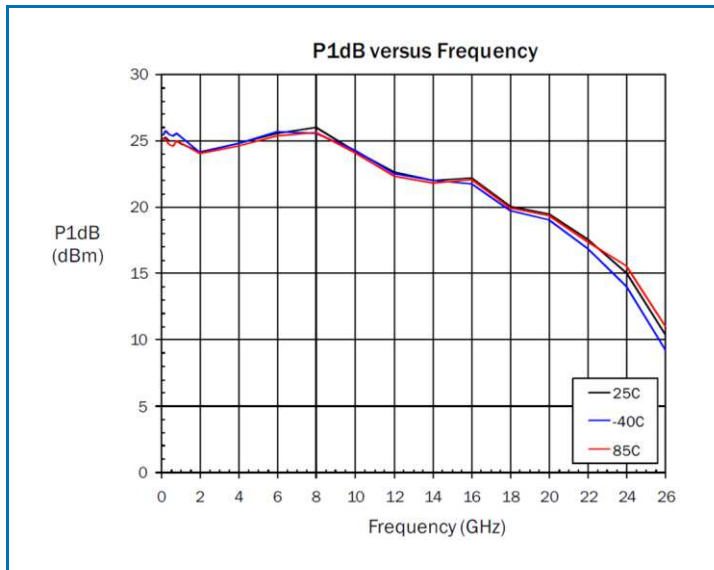
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
<b>General Performance</b>					<b><math>T_A = +25^{\circ}C</math>, <math>V_{DD} = +8V_{DC}</math>, <math>V_{G2}</math> at <math>= +3.5V_{DC}</math>, <math>I_{DD} = 300mA</math></b>
Operating Frequency	0		20	GHz	
Gain	13.8	14.5		dB	10GHz
Maximum Output Voltage		8		$V_{P-P}$	
IP3 at 10GHz		36		dBm	$P_{OUT} \approx 0dBm$
P1dB at 10GHz		25		dBm	
P3dB at 10GHz		26.5		dBm	
Noise Figure at Mid-Band		4		dB	
Input Return Loss		13		dB	
Output Return Loss		15			
Supply Current		300		mA	
Supply Voltage		8		$V_{DC}$	

\*Adjust  $V_{TI}$  between  $-1.5V_{DC}$  to  $+0.2V_{DC}$  to achieve  $I_{DD} = 300mA$  typical.,  $V_{G2} = 3.5V_{DC}$  typ.

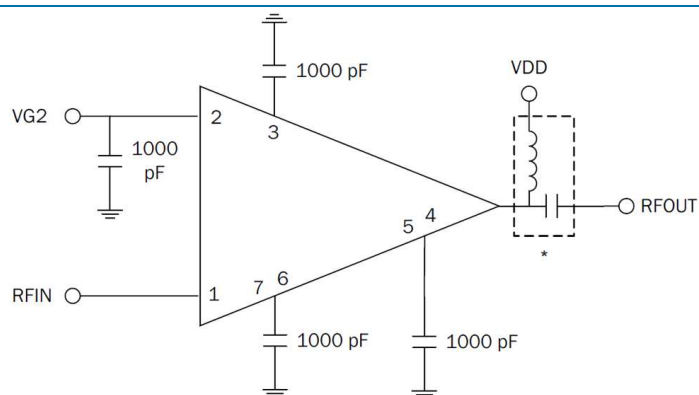


## Typical Performance



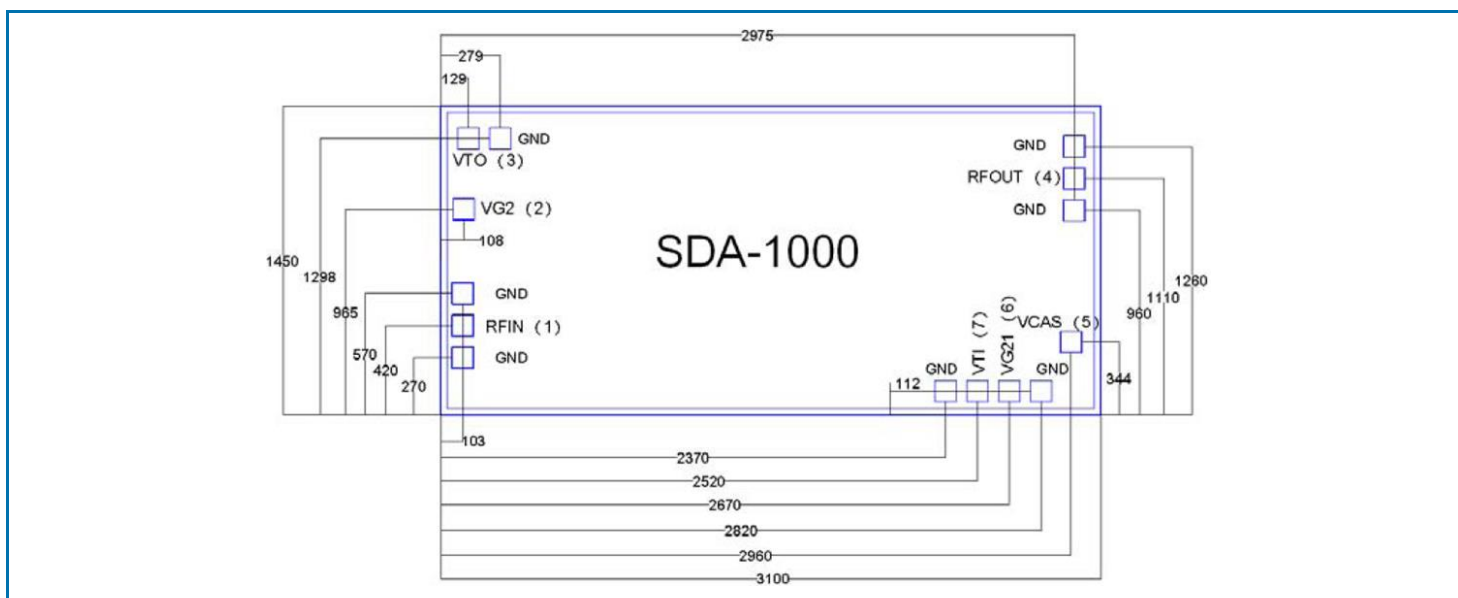
**Typical Performance: (Circuit Board Data with Bias Tees)  $V_S = 5V$ ,  $I_D = 51mA$ ,  $R_{BIAS} = 33\Omega$** 


## Typical Application Schematic



\*Note: Drain Bias (VDD) must be applied through a broadband bias tee or external bias network

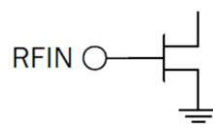
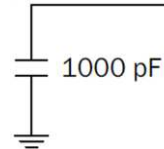
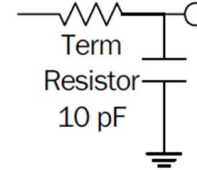
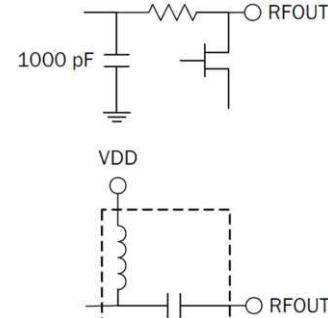
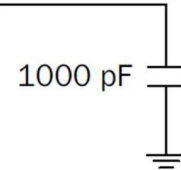
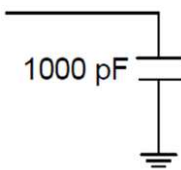
## Package Drawing (Dimensions in microns)



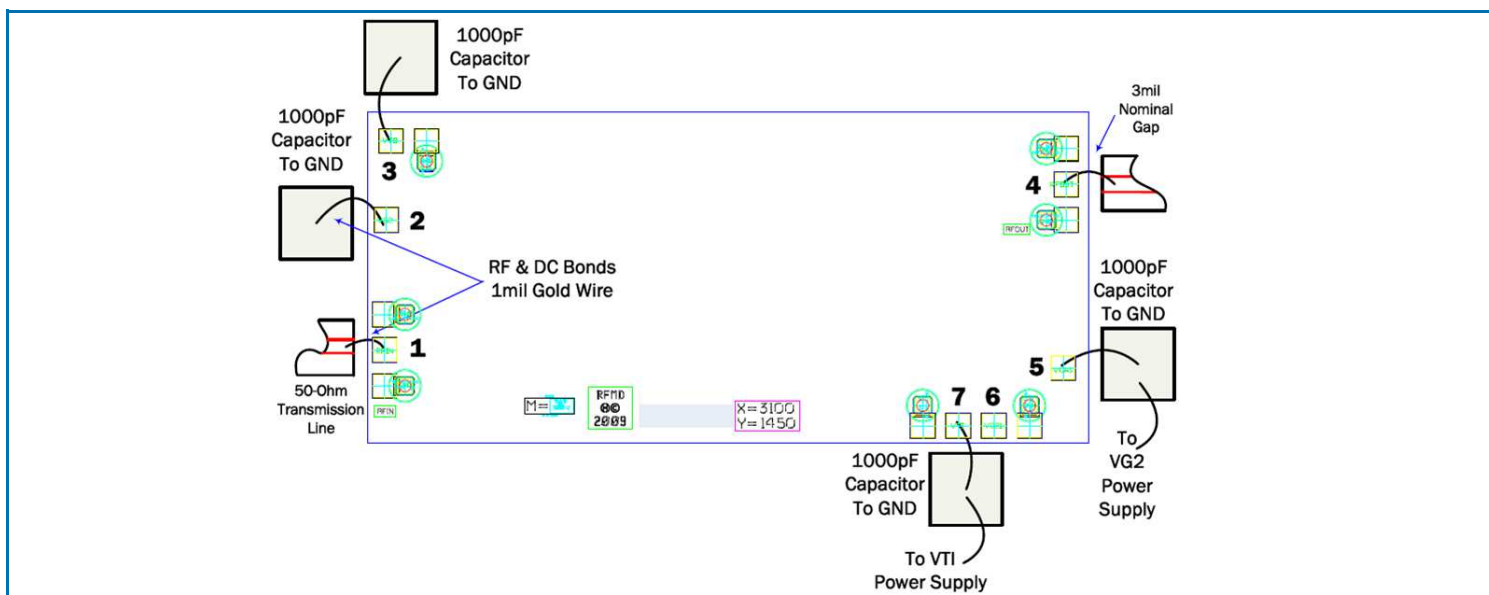
### Notes:

1. No connection required for ground bond pads
2. Die thickness is 0.102mm (4mil)
3. Typical bond pad is 0.100mm square
4. Backside metallization: gold
5. Backside metal is ground
6. Bond pad metallization: gold
7. Refer to drawing posted at [www.rfmd.com](http://www.rfmd.com) for tolerances

## Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1	RFIN	RF Input. This pad is DC coupled and matched to 50Ω from DC to 20GHz. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output.	
2	VG2	VG2 is an optional pad. It may be used to bias the cascode gate of the amplifier. If this port is used, a 1000pF bypass capacitor with the shortest wirebond length possible is recommended to prevent low frequency gain ripple.	
3	VTO	The output drain termination pad. This pad requires a suggested 1000pF bypass capacitor with the shortest wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
4	RFOUT and VDD	RF Output. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output. Connect the DC bias ( $V_{DD}$ ) network to provide drain current ( $I_{DD}$ ).	 <p>Note: Drain Bias (<math>V_{DD}</math>) must be applied through a broadband bias tee or external bias network</p>
5	VCAS	Provides VG2 gate voltage to the cascode amplifier. The value is $\sim (V_{CC}/2 - \text{absolute value of } V_{TI})$ .	
6	VG21	Not connected.	
7	VTI	Input gate voltage, used to bias the amplifier. The value is between $-1.5V_{DC}$ (device is pinched OFF) to $+0.2V_{DC}$ (fully ON). This pad requires a bypass capacitor to ground with the shortest possible wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
Die	GND	Ground connection. Connect die bottom directly to ground plane for best performance. NOTE: The die should be connected directly to the ground plane with conductive epoxy.	

## Assembly Diagram



## Measurement Technique

All specifications and typical performances reported in this document were measured in the following manner. Data was taken using a temperature controlled probe station utilizing 150 $\mu$ m pitch GSG probes. The interface between the probes and integrated circuit was made with a coplanar to microstrip ceramic test interface. The test interface was then wire bonded to the die as shown in the figure below using 1mil diameter bondwires. The spacing between the test interface and the die was 200 $\mu$ m, and the bond wire loop height was 100 $\mu$ m. The thickness of the test interface is 125 $\mu$ m (5mil). The calibration of the test fixture included the probes and test interfaces, so that the measurement reference plane was at the point of bond wire attachment. Therefore, all data represents the integrated circuit and accompanying bond wires.

