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SDIO101A

SD/SDIO/MMC/CE-ATA host controller

Rev. 1 — 13 June 2013 Product data sheet

1. General description

The SDIO101A is a SD/SDIO/MMC/CE-ATA host controller with a standard 16-bit asynchronous memory interface. The device conforms to the *SD Host Standard Specification Version 2.0* (see Ref. 1). The SDIO101A manages the physical layer of SD, SDIO, MMC and CE-ATA protocols and can be used together with SD Host Standard compatible driver software to add SD/SDIO/MMC/CE-ATA host functionality to a variety of microprocessor systems.

The SDIO101A supports both full-speed (< 25 MHz) and high-speed (< 52 MHz) data transmissions on the SD/SDIO/MMC/CE-ATA port. The SDIO101A offers separate pins for SD/SDIO/MMC/CE-ATA port supply voltage, host interface supply voltage and core supply voltage. The SD/SDIO/MMC/CE-ATA port can operate at a wide voltage range (1.8 V to 3.6 V) which allows the device to interface to a large variety of SD, SDIO, MMC or CE-ATA devices. The SDIO101A allows 1-bit and 4-bit SD transactions and 8-bit MMC/CE-ATA transactions. The 16-bit asynchronous memory interface can operate at a 2.5 V to 3.6 V voltage range.

A built-in, 2 kB data buffer allows for a low interrupt latency time and efficient communication with the host processor at high data rates. The SDIO101A provides a DMA request line that can be connected to an external DMA controller to off-load the host processor and increase overall system performance.

An on-board PLL allows a large range of SD/SDIO/MMC/CE-ATA clock speeds to be generated from a single externally available clock source. An additional fractional divider allows the SD clock speed to be fine-tuned with very fine granularity, which enables the user to achieve the maximum desired SD clock speed from the external clock source.

The SDIO101A offers 5 levels of power saving, including a ‘Hibernate mode’ where the on-board oscillator, PLL and data buffer memories are switched off, and a ‘Coma mode’ in which supply power to most of the device is internally switched off. This allows the device to be used in very power-critical applications.

2. Features and benefits

2.1 General

- Provides 1 SD/SDIO/MMC/CE-ATA slot, operating in 1-bit, 4-bit and 8-bit (MMC/CE-ATA) modes
- 2.5 V to 3.3 V host interface
- 1.8 V core supply voltage
- Separate SD supply voltage pin. SD/SDIO/MMC/CE-ATA slot is able to operate at a wide voltage range (1.8 V to 3.3 V).

- Compliant with *SDIO card specification version 2.00* (see Ref. 2)
- Compliant with *SD Host Controller Standard Specification Version 2.0* (see Ref. 1)
- Compliant with *SD Physical Layer Specification version 2.0* (see Ref. 3)
- Compliant with *MMC Specification version 3.31 and 4.2* (see Ref. 4)
- Supports CE-ATA Digital Protocol revision 1.1 (see Ref. 5)
- Supports CE-ATA Digital Protocol commands (CMD60/CMD61)
- Dedicated SD Card Detection input pin (insertion/removal)
- Dedicated SD Card Write Protection input pin
- Full speed (< 25 MHz) and high-speed (< 52 MHz) SD data transmissions
- Supports interrupt and slave-DMA transfer operation
- Built-in 2 kB double data buffer (with 1 kB maximum block size) for efficient communication with host processor
- Supports SDIO features Multi-block, Suspend/Resume, Read Wait and Wake-up Control
- Up to 400 Mbit/s read and write data transfer rates at 50 MHz using MMC 8 data lines
- Up to 208 Mbit/s read and write data transfer rates at 52 MHz using SD 4 data lines
- On-board crystal oscillator and PLL
- 5 levels of power saving, including a ‘Hibernate mode’ where oscillator, PLL and memories are switched off, and a ‘Coma mode’ that internally switches off supply power to most of the chip
- Additional on-board fractional clock divider for fine-grained SD clock speed control
- Cyclic Redundancy Check (CRC) for command and data
- Programmable pull-up resistor on SD CMD and SD DATn lines
- Programmable drive strength for SDCLK output to optimize SD/SDIO/MMC/CE-ATA clock speed

2.2 Host processor interface

- Supports 16-bit asynchronous memory interface
- Separate host interface power supply pin, able to operate on 2.5 V to 3.3 V
- Programmable open collector or push-pull mode for $\overline{\text{INT}}$ interrupt pin output

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SDIO101AIHR	D101A	HXQFN60	plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 5 × 5 × 0.5 mm	SOT1133-2

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SDIO101AIHR	SDIO101AIHRZ	HXQFN60	Reel 7" Q1/T1 *standard mark dry pack	1500	T_{amb} = −40 °C to +85 °C
SDIO101AIHR	SDIO101AIHRE	HXQFN60	Standard marking * Tray dry pack, bakeable, single	490	T_{amb} = −40 °C to +85 °C

4. Block diagram

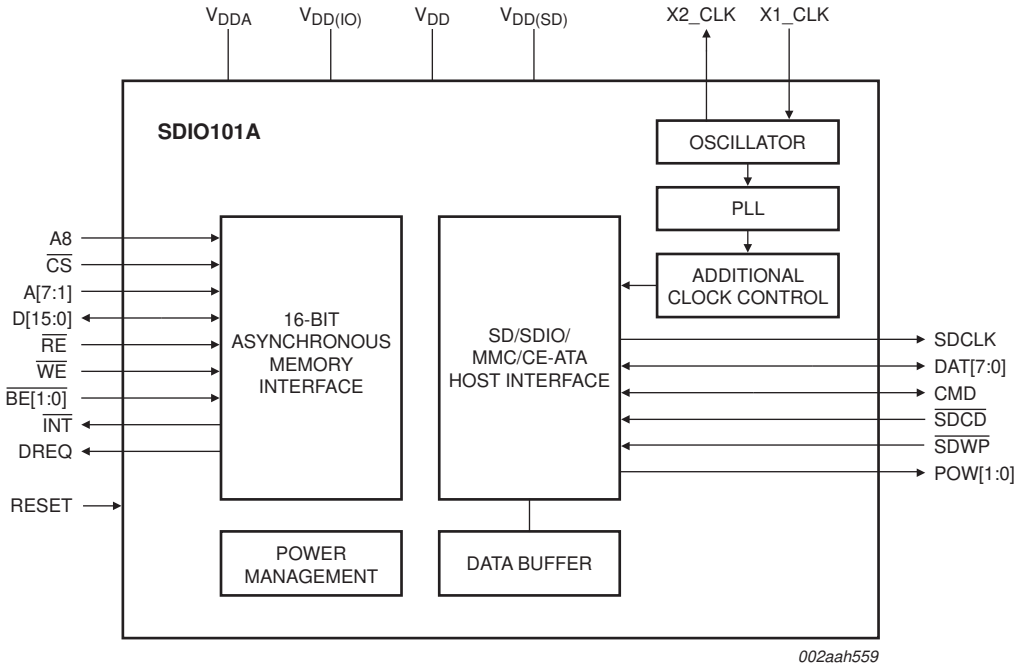


Fig 1. Block diagram of SDIO101A

5. Pinning information

5.1 Pinning

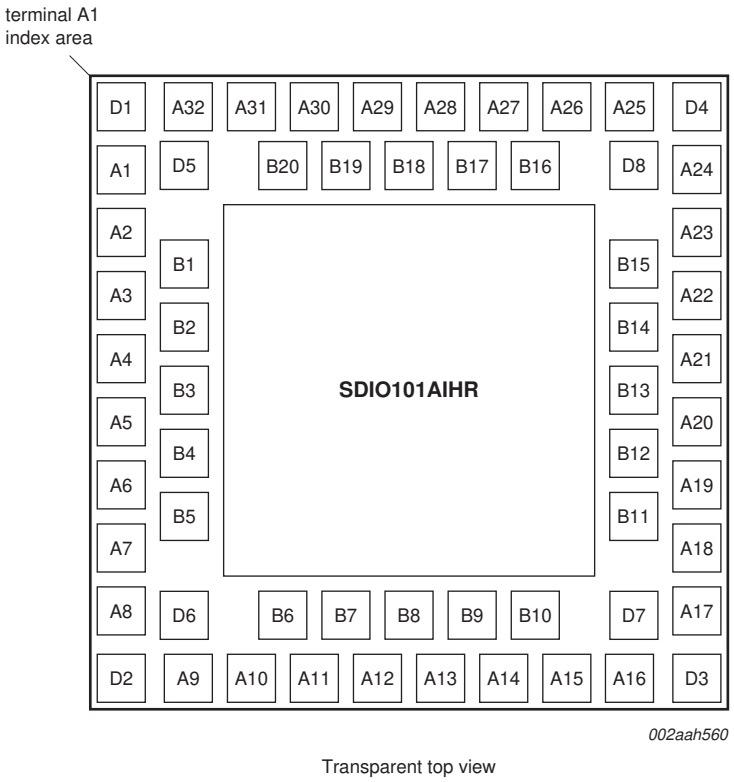
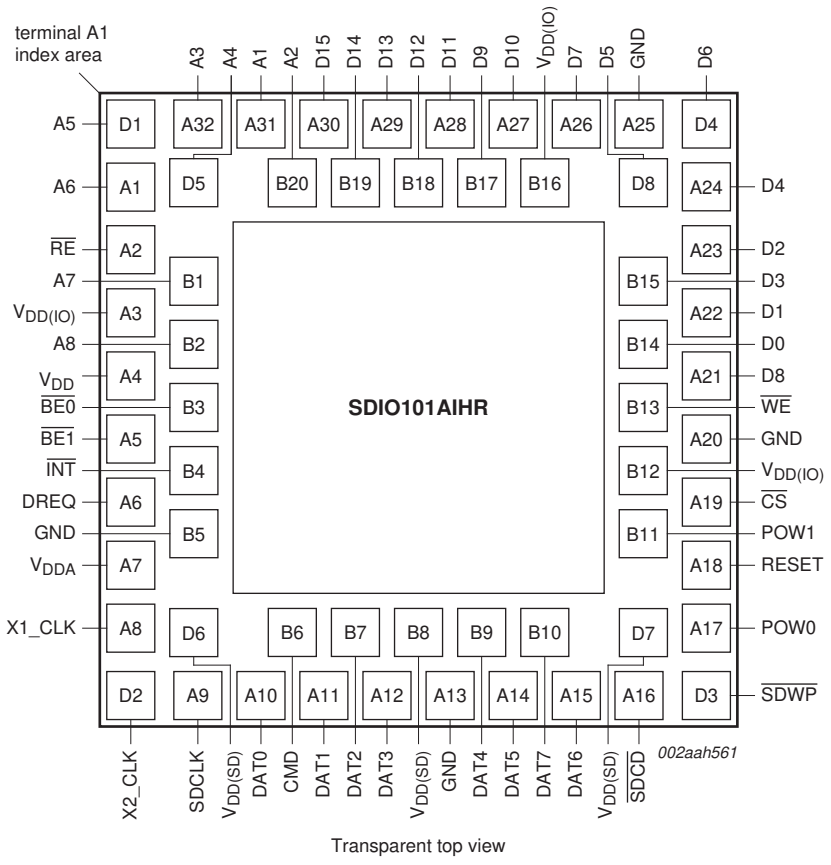


Fig 2. Pin configuration for HXQFN60



Transparent top view

Fig 3. Terminal mapping for HXQFN60

5.2 Pin description

5.2.1 Pin description by function

Following are the signal descriptions on the SDIO101A interfaces. Pins are organized by function.

Table 3. Pin description by function

B = bidirectional; I = input; O = output; n.c. = not connected.

Symbol	Pin	Type	Description
SD/SDIO/MMC/CE-ATA interface signals			
SDCLK	A9	O	**SD clock output.** This output clock is driven by the host controller during read and write transactions.
CMD	B6	B	**SD command line.** This bidirectional signal is used to transfer commands and responses between the host and the card.
DAT0	A10	B	**SD Data bit 0.**
DAT1	A11	B	**SD Data bit 1.**
DAT2	B7	B	**SD Data bit 2.**
DAT3	A12	B	**SD Data bit 3.**
DAT4	B9	B	**SD Data bit 4.**
DAT5	A14	B	**SD Data bit 5.**
DAT6	A15	B	**SD Data bit 6.**
DAT7	B10	B	**SD Data bit 7.**
$\overline{\text{SDCD}}$	A16	I	**SD card detect (active LOW).** This pin can be used to detect insertion and removal of SD/SDIO/MMC cards.
$\overline{\text{SDWP}}$	D3	I	**SD write protect (active LOW).** This pin can be used to detect if the inserted SD/SDIO/MMC card is write protected.
System interface signals			
X1_CLK	A8	I	**Clock input.** Must be connected to the system clock which is used to generate the host bus interface (see Section 6.4.3.1).
X2_CLK	D2	O	**Clock output.**
RESET	A18	I	**Asynchronous reset (active HIGH).** This active HIGH input pin unconditionally resets the entire device.
Card power supply control interface signals			
POW[1:0]	B11, A17	O	**SD power supply control bits.** These bits can be used to control the voltage of an external power supply for the SD/SDIO/MMC/CE-ATA device. See Table 5 for details.

Table 3. Pin description by function *...continued*

B = bidirectional; I = input; O = output; n.c. = not connected.

Symbol	Pin	Type	Description
Host Interface control signals			
$\overline{CS}$	A19	I	**Chip Select (active LOW).**
A[7:1]	B1, A1, D1, D5, A32, B20, A31	I	**Address lines.** Can be used to address the 256 bytes of the Standard Host register space.
A8	B2	I	**Address 8.** When accessing SDIO101A transmit or receive buffer under DMA control, this pin must be HIGH. This pin must be LOW when accessing other registers or when accessing transmit or receive buffer under interrupt control.
D[15:0]	A30, B19, A29, B18, A28, A27, B17, A21, A26, D4, D8, A24, B15, A23, A22, B14	B	**Data lines.** Used to transfer data between host controller and the processor.
$\overline{RE}$	A2	I	**Read Enable (active LOW).** Initiates a read transaction when active.
$\overline{WE}$	B13	I	**Write Enable (active LOW).** Initiates a write transaction when active.
$\overline{BE[1:0]}$	A5, B3	I	**Byte write enables (active LOW).** When $\overline{BE[0]}$ is active, the least significant byte on the data bus can be written. When $\overline{BE[1]}$ is active, the most significant byte on the data bus can be written.
$\overline{INT}$	B4	O	**Interrupt request (active LOW).** Can be configured as push/pull or open-collector output.
DREQ	A6	O	**DMA request.**
Power interface signals			
V_{DD}	A4	-	**Core power supply pin, 1.8 V.**
V_{DDA}	A7	-	**Analog power supply, 1.8 V.**
$V_{DD(SD)}$	D6, B8, D7	-	**SD power supply pins, 1.8 V to 3.3 V.**
$V_{DD(IO)}$	B12, B16, A3	-	**Host interface power supply pins, 2.5 V to 3.3 V.**
GND	B5, A13, A20, A25[1]	-	**Ground.**
GND	center pad[1]	-	**Ground.**

[1] HXQFN60 package die supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

The SDIO101A offers the SD Standard Host register set as defined in the *SD Host Standard Specification Version 2.0* (see Ref. 1), through which the Host Driver software can configure the host controller and initiate transactions to and from an SD/SDIO/MMC/CE-ATA target. On top of the Standard Host registers, 4 extra registers are available in the Host Controller register space, which can be used to control the additional features in the SDIO101A. These features are described in detail in Section 6.4. Section 6.2 gives an overview of the SDIO101A register set.

6.1 DMA mode

The SDIO101A supports slave DMA where the transferring of data between the host and the SDIO101A is under the control of the host's DMA controller. In this mode, the software can program DMA burst size (number of 16-bit words per DMA cycle) as well as the delay between back-to-back DMA requests from SDIO101A.

In DMA mode, Buffer Data Port 0 (0x20) and Buffer Data Port 1 (0x22) are mapped differently than in Interrupt mode — address line A8 must be at logic 1 when Buffer Data Ports are being accessed while the rest of the address lines are ignored by the SDIO101A. Once the DMA operation starts, all the accesses to the SDIO101A with A8 set to logic 1 will be considered as Buffer Data Ports access. To access other SDIO101A internal registers, address A8 must be set to logic 0.

The total number of DMA accesses to the Buffer Data Ports must be an even number. The first access from the host will be to Buffer Data Port 0, and the second access will be to Buffer Data Port 1. The SDIO101A will automatically alternate between Buffer Data Port 0 and Buffer Data Port 1 on each access by the host. This scheme allows the SDIO101A Buffer Data Ports to look like a continuous block of memory or FIFO to the DMA controller.

There are two registers that must be programmed for the SDIO101A to support DMA operation:

- Miscellaneous register (0xF8) bit 1 (enable slave DMA) must be set to logic 1.
- DMA burst size and DMA inter delay (back-to-back DREQs) must be programmed through DMA register (0xF4). DMA register bit [8:0] programs the DMA burst size (the number of 16-bit words to be transferred between the DMA controller and the SDIO101A), and DMA register bit [15:9] programs the delay time between two back-to-back DMA requests from SDIO101A (the inter delay value in bit [15:9] represents the number of SD clocks).

6.1.1 DMA read

When the receive buffer is empty, DREQ is at LOW state. Once the receive buffer has at least the number of 16-bit words equal to the programmed DMA burst size (DMA register [8:0]) DREQ goes HIGH. The DMA controller then can perform a block read of the receive buffer with the block size equal to the programmed DMA burst size in the DMA register.

The DREQ will go LOW once a block of data has been read from the SDIO101A's receive buffer, and DREQ will remain LOW for a period defined by DMA register bit [15:9]. The DREQ signal will go HIGH again if the receive buffer still holds at least the burst size of 16-bit word data.

6.1.2 DMA write

When the transmit buffer is empty, DREQ is at HIGH state. The DMA controller then can perform a block write to the receive buffer with the block size equal to the programmed DMA burst size programmed in DMA register [9:0].

The DREQ will go LOW once a block of data has been written to the SDIO101A's transmit buffer, and DREQ will remain LOW for a period defined by DMA register bit [15:9]. The DREQ signal will go HIGH again if the transmit buffer still has space to hold at least the burst size of 16-bit word data.

6.2 Standard Host register overview

Table 4. SD Host Controller register map

Offset	Bits 15:8	Bits 7:0	Offset	Bits 15:8	Bits 7:0
0x02	System Address (high)		0x00	System Address (low)	
0x06	Block Count		0x04	Block Size	
0x0A	Argument1		0x08	Argument0	
0x0E	Command		0x0C	Transfer Mode	
0x12	Response1		0x10	Response0	
0x16	Response3		0x14	Response2	
0x1A	Response5		0x18	Response4	
0x1E	Response7		0x1C	Response6	
0x22	Buffer Data Port1		0x20	Buffer Data Port 0	
0x26	Present State		0x24	Present State	
0x2A	Wake-up Control	Block Gap Control	0x28	Power Control	Host Control
0x2E	Software Reset	Time-out Control	0x2C	Clock Control	
0x32	Error Interrupt Status		0x30	Normal Interrupt Status	
0x36	Error Interrupt Status Enable		0x34	Normal Interrupt Status Enable	
0x3A	Error Interrupt Signal Enable		0x38	Normal Interrupt Signal Enable	
0x3E	reserved		0x3C	Auto CMD12 Error Status	
0x42	Capabilities		0x40	Capabilities	
0x46	Capabilities (reserved)		0x44	Capabilities (reserved)	
0x4A	Maximum Current Capabilities		0x48	Maximum Current Capabilities	
0x4E	Maximum Current Capabilities (reserved)		0x4C	Maximum Current Capabilities (reserved)	
0x52	(reserved)		0x50[1]	IO-cell Configuration	
-	-		-	-	
0xF6[1]	Secondary Clock Control		0xF4[1]	DMA register	
0xFA[1]	PLL		0xF8[1]	Miscellaneous	
0xFE	Host Controller Version		0xFC	Slot Interrupt Status	

[1] This register is not part of the Standard Host register set.

6.3 Standard Host register set description

The SDIO101A registers that are part of the Standard Host register set are described in detail in Ref. 1. In this paragraph, we will only describe the specific implementation of the Standard register set in the SDIO101A that are different from Ref. 1.

6.3.1 System Address register (offset 0x00)

Since master-DMA functionality is not implemented, all bits in this register will always read zero. Writes to this register will be ignored.

6.3.2 Block Size register (offset 0x04)

Data written to bits R[14:12] will be ignored. The maximum block size that can be programmed is 1 kB. Any block size higher than that will default to 1 kB.

6.3.3 Transfer Mode register (offset 0x0C)

Since master-DMA functionality is not implemented, bit R[00] will always read zero. Writes to this bit will be ignored.

6.3.4 Present State register (offset 0x24)

The SDIO101A supports multiple buffers, that is, the available data buffer space (2 kB) is larger than the Maximum Block Size (1 kB). The Buffer Write Enable bit R[10] indicates that there is room to write at least one more single block length (as specified in the Block Size register) in the data buffer even though previously-written blocks might still be present. Similarly, the Buffer Read Enable R[11] bit indicates that there is at least one single block length (as specified in the Block Size register) available in the data buffer.

6.3.5 Host Control register (offset 0x28)

A separate LED control pin SDLD is **not** supported in the SDIO101A. If desired, the user can use a GPIO pin on the Host Processor to implement this functionality. Bit R[00] in the Host Control register will always read zero, and writing to it will have no effect.

6.3.6 Power Control register (offset 0x29)

Bits R[03:00] control the POW[1:0] pins of the SDIO101A, which can be used to control an external power supply that powers the SD/SDIO/MMC/CE-ATA device. Two power modes are supported: ‘normal’ and ‘low power’. It is up to the user to decide what voltage to associate with normal and low-power modes, but a typical implementation is 3.3 V for normal and 1.8 V for low-power mode. Table 5 shows the relation between the Power Control register and the POW[1:0] pins.

Table 5. Relation between the Power Control register and the POW[1:0] pins

Power Control register R[03:00]	POW[1:0]	Description
xxx0b	00b	SD power off
1011b	01b	SD low power (1.8 V) on
1101b	10b	SD normal power (3.3 V) on
1111b	10b	SD normal power (3.3 V) on

6.3.7 Capabilities register (offset 0x40)

The SDIO101A Capabilities register contents are shown in Table 6.

Table 6. Contents of the Capabilities register (offset 0x40)

Location	Attribute	Default	Description
63:30	reserved	00h	reserved
29	reserved	1b	reserved
28	reserved	1b	reserved
27	reserved	1b	reserved
26	R	1b	low voltage (1.8 V) supported
25	R	0b	3.0 V not supported (defaults to normal voltage)
24	R	1b	normal voltage (3.3 V) supported
23	R	1b	suspend/resume supported
22	R	0b	master DMA not supported
21	R	1b	high-speed SD (> 25 MHz) supported
20:18	R	001b	8-bit supported
17:16	R	10b	2 kB maximum block length
15:14	reserved	00h	reserved
13:08	R	00h	get info through other method (Ref. 1)
07	R	1b	time-out clock unit in MHz
06	reserved	0b	reserved
05:00	R	00h	get info through other method (Ref. 1)

6.4 Additional register set description

The additional registers are not part of the *SD Host Standard Specification Version 2.0* (see Ref. 1). These registers do not have to be initialized, so Standard Host Driver software does not have to be aware of them.

6.4.1 IO Configuration register (offset 0x50)

The IO Configuration register offers three bits to set the drive strength of the IO cell used for driving the SDCLK pin. This way the user can adjust SDCLK rise/fall times according to their system performance requirements. Typically, drive strength should be set to LOW when the SD slot is operating on normal (2.7 V to 3.3 V) voltage, and to HIGH when the SD slot is operating on low voltage (1.8 V). Also, a bit is offered to disable the default pull-up resistors on the SD CMD and SD DATn lines, in case they are not required and the possible leakage current through these resistors is undesired.

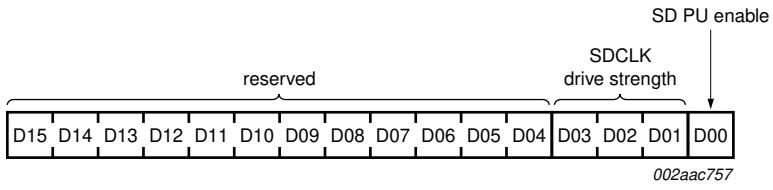


Fig 4. IO Configuration register

Table 7. Contents of the IO Configuration register (offset 0x50)

Location	Attribute	Default	Description
15:04	reserved	0h	reserved
03:01	R/W	0h	SDCLK drive strength select. These bits can be used to program the drive strength of the SDCLK IO cell. Table 8 shows the possible values.
00	R/W	0b	SD line pull-up. If set to b1, the internal pull-up resistors on the SD CMD and SD DATn lines are switched ON.

Table 8. SDCLK drive strength programming

IO Configuration register R[03:01]	SDCLK drive strength
000b	low (SD operating on 2.7 V to 3.6 V)
0001b	reserved
010b	reserved
011b	reserved
100b	high (SD operating on 1.8 V)
101b	reserved
110b	reserved
111b	reserved

6.4.2 DMA register (offset 0xF4)

The DMA register is located in the Common register area. This register controls the DREQ output. The DREQ LOW and HIGH times are programmed with DMA inter delay and DMA burst size.

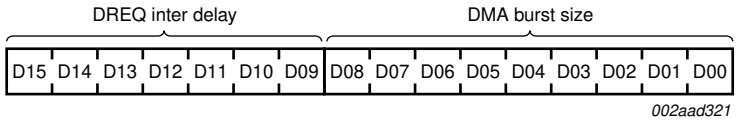


Fig 5. DMA register

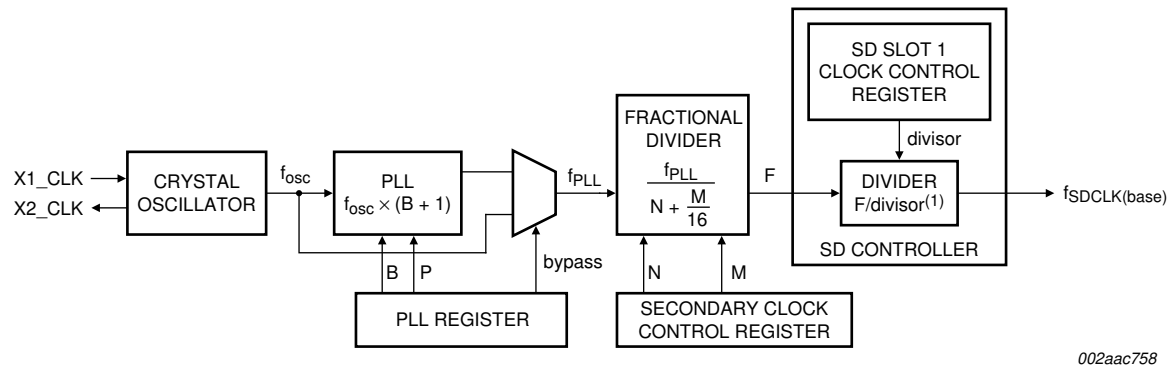
Table 9. DREQ control programming

Location	Attribute	Default	Description
15:09	R/W	0h	DREQ delay period (DREQ LOW time) LOW time = value × SD clock cycle time
08:01	R/W	0h	DMA burst size (DREQ HIGH time)

Remark: Refer to Section 6.1 for more detailed DMA description.

6.4.3 Secondary Clock Control register (offset 0xF6)

The Secondary Clock Control register is located in the Common register area. This register gives the user more control over the clock generation. An additional fractional divider is offered to program the SDCLK base frequency with higher granularity, allowing the design to use an existing (available) clock rather than an external crystal or oscillator. Figure 6 shows the architecture of the secondary clock control.



(1) Divisor is set by the Clock Control register (0x2C).

Fig 6. Secondary clock control architecture

The SDCLK base frequency can be calculated with Equation 1[1]:

$$f_{SDCLK(base)} = \frac{f_{PLL}}{divisor\left(N + \frac{M}{16}\right)} \quad (1)$$

Where 'divisor' is the standard divisor as programmed in the Clock Control register; N is the integer divisor as programmed in the Secondary Clock Control register R[07:00]; M is the fractional divisor as programmed in the Secondary Clock Control register R[11:08]. Figure 7 and Table 10 below show the register bits of the Secondary Clock Control register.

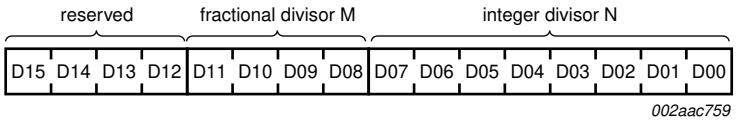


Fig 7. Secondary Clock Control register

Table 10. Contents of the Secondary Clock Control register (offset 0xF6)

Location	Attribute	Default	Description
15:12	reserved	00h	reserved
11:08	R/W	00h	fractional divisor value M
07:00	R/W	01h	integer divisor value N

1. This is the average SD clock frequency. The peak SD clock frequency might be higher when the fractional divisor M is used.

6.4.3.1 SDIO101A X1_CLK input

It is recommended that the SDIO101A's input clock be connected to one of the systems available clock sources to eliminate the use of an external crystal. The best use case is to have the SDIO101A's X1_CLK input be connected to the processor's clock output (Figure 8) or processor's crystal output (Figure 9). In either case, the SDIO101A internal PLL can be used to boost up the X1_CLK input then divided down to the desired SDIO clock by using the internal divider in combination with the built-in fractional divider.

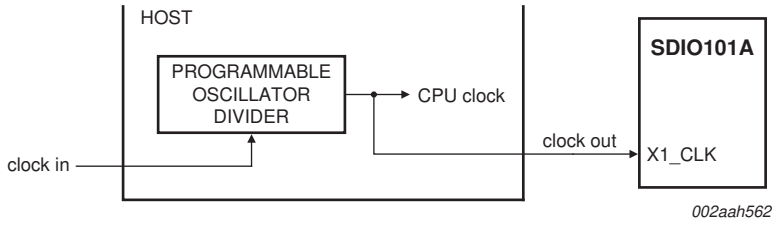


Fig 8. X1_CLK connected to processor's system clock

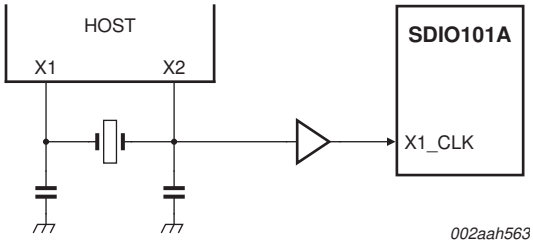


Fig 9. X1_CLK connected to processor crystal clock output

Figure 10 details a typical scenario where the host processor uses a 13 MHz crystal as its clock source, and the same clock is used by the SDIO101A to operate the SD clock as close to 50 MHz as possible.

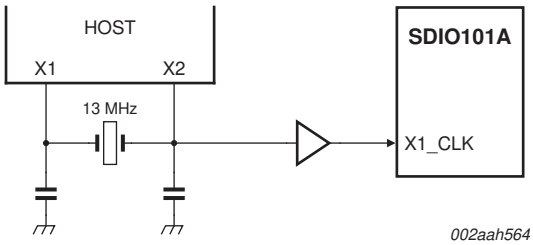


Fig 10. Host processor using 13 MHz crystal as clock source

With its input clock supplies by the processor crystal output, the SDIO101A internal PLL (0xFA) is used to boost the input frequency to 104 MHz, the standard Clock Control register (0x2C) and the fractional divider (0xF6) registers are then used to divide the 104 MHz to about 48.9 MHz to be used as SD clock.

PLL register (0xFA) settings:

Bit 15 = 0b

Bit 14 = 0b

Bit [13:7] = 0000000b

Bit [6:5] = 01b

Bit [4:0] = 00111b; B = 7

Fractional divider (0xF6) settings:

Bit [15:12] = 0000b; reserved bit

Bit [11:8] = 0001b; M = 1

Bit [7:0] = 00000001b; N = 1

Clock Control register (0x2C) settings:

Bit [15:0] = 103h

$$f_{SDCLK(base)} = \frac{f_{PLL}}{divisor\left(N + \frac{M}{16}\right)}$$

= (13 MHz × 8) / (2 × (1 + 1 / 16))

= 48.9 MHz

6.4.4 Miscellaneous register (offset 0xF8)

The Miscellaneous register is located in the Common register area. This register can be programmed to put the device in the 'Coma mode' or 'Hibernate mode', extra-low power-down modes on top of the Standby mode programmable through bit R[00] in the Clock Control register. Also, a bit is offered to disable the DREQ DMA request line on the Host Interface. Lastly, a bit is offered to switch between open-drain and push-pull mode for the $\overline{INT}$ interrupt output pin. Figure 11 and Table 11 below show the register bits of the Miscellaneous register.

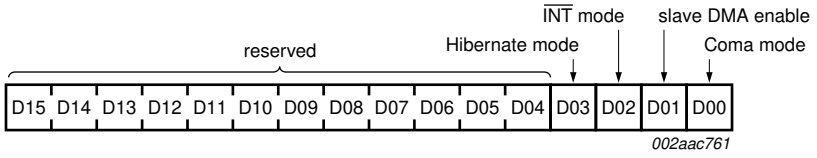


Fig 11. Miscellaneous register

Table 11. Contents of the Miscellaneous register (offset 0xF8)

Location	Attribute	Default	Description
15:04	reserved	00h	reserved
03	R/W	0b	Hibernate mode select. When set to 1b, the oscillator, PLL and supply to the buffer memory will be switched OFF. Card detection is disabled. Clearing this bit will re-instate power to the buffer memory, the oscillator and PLL are enabled.
02	R/W	0b	INT mode select. When set to 0b, the $\overline{INT}$ interrupt output pin will be open-drain mode. An external 10 kΩ pull-up resistor is required in this case. When set to 1b, the $\overline{INT}$ interrupt output pin will be in push-pull mode.
01	R/W	1b	Slave DMA enable. If programmed to 1b, the DREQ signal will be functional. If programmed to 0b, the DREQ signal will be fixed to zero.
00	R/W	0b	Coma mode. If programmed to 1b, power will internally be switched off to most of the device, resulting in a very low coma mode current. All state in the device will be lost, and no registers can be read or written, with the exception of the 'Software Reset for All' bit in the Software Reset register. Clearing this bit will re-instate power to the entire chip, and reset the SDIO101A. A hard-reset on the RESET pin will also bring the device back out of Coma mode.

6.4.5 PLL register (offset 0xFA)

The PLL register is located in the Common register area. This register provides control over the Phase-Locked Loop, which is used in the SDIO101A to generate an SD base clock frequency from the crystal oscillator or external clock source. The default values of this register are such that the PLL multiplies the incoming frequency from the crystal oscillator by 5. This means that, if the PLL register is not programmed, the frequency generated by the crystal oscillator or external clock source should be 10.4 MHz in order to generate the 52 MHz maximum SDCLK speed. For the SD base clock frequency generated by the PLL from the Crystal oscillator frequency it holds

$$f_{PLL} = (B + 1) \times f_{CLK} \tag{2}$$

where B is the feedback divider value as programmed in R[04:00] of the PLL register. The user should determine the desired f_{PLL}, choose the required value B for the feedback divider based on the available clock source f_{osc}, and then choose a value for post divider P (as programmed in R[06:05]) such that the following condition gets satisfied:

$$156\ MHz < 2 \times (P + 1) \times f_{PLL} < 320\ MHz \tag{3}$$

The post divider setting decided by the value of P does not affect the frequency value (in MHz) of the f_{PLL}. The only advantage of this post divider is in adjusting the duty cycle of the resulting f_{PLL} clock. The greater the value of P, the closer the duty cycle will be to 50 % (provided the condition mentioned in Equation 3 is not violated, for a guaranteed behavior).

The PLL register also provides the possibility to bypass the PLL post divider, effectively setting a value of 1 for P. Also, the user can bypass the entire PLL. Figure 12 and Table 12 show the register bits of the PLL register.

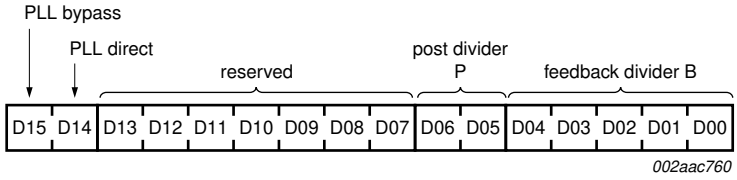


Fig 12. PLL register

Table 12. Contents of the PLL register (offset 0xFA)

Location	Attribute	Default	Description
15	R/W	1b	PLL bypass. If this bit is 1b, the PLL is bypassed. The SDCLK base frequency is then equal to the frequency provided by the oscillator, either generated by a crystal or generated by an external clock. If this bit is 0b, the PLL is not bypassed.
14	R/W	1b	PLL direct. If this bit is 1b, the post divider of the PLL is bypassed, effectively setting the post divider value P to 1b. In this mode, the duty cycle out of the PLL can be unequal to 50 %. If set to 0b, the post divider P is used, and its value is determined by R[06:05] of the PLL register.
13:07	reserved	00h	reserved
06:05	R/W	01h	PLL post divider P
04:00	R/W	04h	PLL feedback divider B

6.4.6 Host Controller Version register (offset 0xFE)

The SDIO101A Host Controller version is shown in Table 13.

Table 13. Contents of the Host Controller Version register (offset 0xFE)

Location	Attribute	Default	Description
15:08	R	10h	SDIO101A version 1.0
07:00	reserved	00h	reserved[1]

[1] These bits do not match Host Controller specification. Host driver should not use these bits.

6.5 Power-saving modes

The SDIO101A provides 5 power-saving modes that can be used in different situations to minimize the power consumption of the device. Table 14 below describes these modes and their associated register bits that can be programmed to enable them. Idle, Low Power and Standby modes can be used if card interrupts should still be serviced. The Hibernate mode will switch off the power to the SD device and the Coma mode switches off most of the Host Controller, therefore, card interrupts will not be generated. Table 14 shows the 5 power-saving modes.

Table 14. SDIO101A Power-saving modes

Mode	Associated register bits	Description
Idle mode	Clock Control register R[02]	SD Card clock stopped; oscillator and PLL are active.
Low-Power mode	Power Control register R[00]	SD Card power switched off.
Standby mode	Clock Control register R[00]	When the Clock Control register R[00] is set to b0, the SDIO101A internal clock is stopped, the PLL is in Power-down mode, the oscillator is active and all register states are maintained. The device will still respond to card interrupts. When waking up from Standby mode, after writing a b1 in the Clock Control register R[00], the data buffer FIFO pointers will reset to empty.
Coma mode	Miscellaneous register R[00]	When the Miscellaneous register R[00] is set to b1, the SDIO101A internal power is switched off. All device pins are 3-stated, and only a write to the 'Software Reset for All' bit in the Software Reset register or a hard reset on the RESET pin will wake up the device. All device states, including data buffer contents, are lost. Card insertion and removal detection through the $\overline{SDCD}$ pin is disabled.
Hibernate mode	Miscellaneous register R[03]	The oscillator, PLL and supply to the buffer memory will be switched off. All states are maintained, but data buffer contents are lost. Card insertion and removal detection through the $\overline{SDCD}$ pin is disabled. Upon wake-up, the data buffer FIFO pointers will reset to empty.

7. Application design-in information

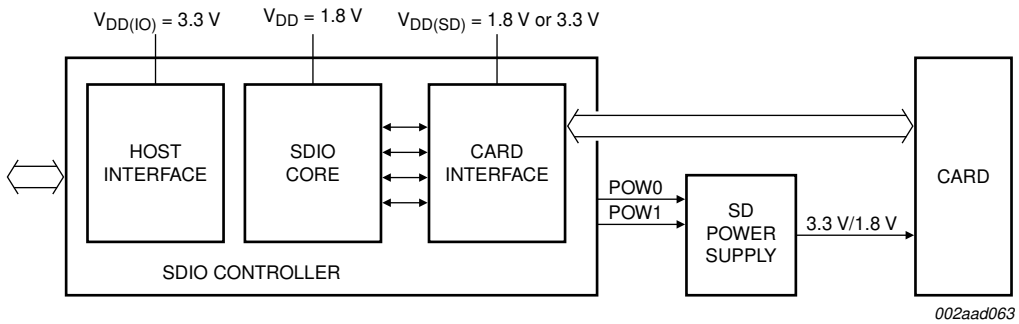


Fig 13. Typical application: host and card interface

8. Basic architecture

The SDIO101A provides SD/SDIO/MMC/CE-ATA functionality to a microprocessor system as illustrated in Figure 14. A standard SD/SDIO/MMC/CE-ATA driver running on the host processor will be able to access the standard host register set in the SDIO101A through the 16-bit memory interface, and initiate transactions to and from the SD card. An external SD power supply (controlled by the SDIO101A) can be used to supply the SD card.

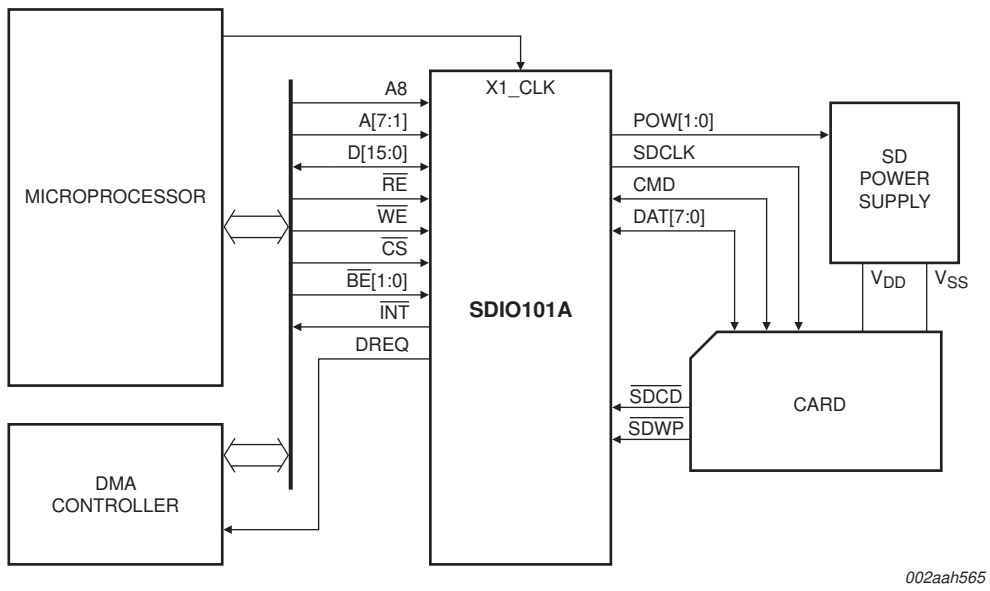


Fig 14. SDIO101A used in a microprocessor application

9. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(IO)}$	input/output supply voltage	host interface; in 2.5 V to 3.3 V range	−0.3	+4.6	V
$V_{DD(SD)}$	SD supply voltage	SD interface			
		in 1.8 V range	−0.3	+1.95	V
		in 3.3 V range	−0.3	+3.6	V
V_{DD}	supply voltage	core; 1.8 V range	−0.3	+2.4	V
V_I	input voltage	on any input pin			
		1.8 V interface	V_{SS} − 0.3	V_{DD} + 0.6	V
		3.3 V interface	−0.3	+3.6	V
T_{amb}	ambient temperature	operating	−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{ESD}	electrostatic discharge voltage	SD/MMC/SDIO interface; Human Body Model	−4	+4	kV

10. Recommended operating conditions

Table 16. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	core	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage	host interface	2.25	3.3	3.6	V
$V_{DD(SD)}$	SD supply voltage	SD interface	1.65	3.3	3.6	V
$f_{clk(ext)}$	external clock frequency	[1]	1	-	52	MHz
$I_{DD(AV)}$	average supply current	f = 13 MHz; SDCLK = 25 MHz	-	6	-	mA
I_{DD}	supply current	Standby mode	-	460	-	µA
		Hibernate mode	-	69	-	µA
		Coma mode	-	5	-	µA
T_{oper}	operating temperature		−40	+25	+85	°C

[1] If the PLL is not bypassed, the minimum input frequency is 10 MHz.

11. Static characteristics

Table 17. Static characteristics

Symbol	Parameter	Conditions		$V_{DD(IO)}$ = 2.5 V		$V_{DD(IO)}$ = 3.3 V		Unit
				Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage	X1_CLK	[1]	−0.3	+0.6	−0.3	+0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage	X1_CLK	[1]	2.4	V_{DD}	2.4	V_{DD}	V
V_{IL}	LOW-level input voltage			−0.3	+0.65	−0.3	+0.8	V
V_{IH}	HIGH-level input voltage			1.6	V_{DD}	2.1	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	0.4	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = −800 µA		1.4	-	2.1	-	V
I_{LIL}	LOW-level input leakage current			-	10	-	10	µA
I_{LIH}	HIGH-level input leakage current			-	10	-	10	µA
$I_{L(clk)}$	clock leakage current	X1_CLK		-	30	-	30	µA
C_i	input capacitance			-	5	-	5	pF
Dynamic average supply current ($V_{DD(SD)}$ = 3.3 V)								
$I_{DD(AV)}$	average supply current	25 MHz	[2]	-	7	-	7	mA
		52 MHz	[2]	-	9	-	9	mA
$I_{DD(IO)}$	input/output supply current	25 MHz	[3]	-	1.3	-	1.5	mA
		52 MHz	[3]	-	1.3	-	1.5	mA
$I_{DD(SD)}$	SD supply current	25 MHz		-	1.5	-	1.5	mA
		52 MHz		-	2.3	-	2.3	mA
Hibernate mode supply current ($V_{DD(SD)}$ = 3.3 V)								
I_{DD}	supply current		[2]	-	130	-	130	µA
$I_{DD(IO)}$	input/output supply current	25 MHz	[3]	-	20	-	20	µA
$I_{DD(SD)}$	SD supply current			-	1.5	-	1.5	µA
Standby mode supply current ($V_{DD(SD)}$ = 3.3 V)								
I_{DD}	supply current		[2]	-	4	-	4	mA
$I_{DD(IO)}$	input/output supply current		[3]	-	20	-	20	µA
$I_{DD(SD)}$	SD supply current			-	1.5	-	1.5	µA
Coma mode supply current ($V_{DD(SD)}$ = 3.3 V)								
I_{DD}	supply current		[2]	-	0.6	-	0.6	µA
$I_{DD(IO)}$	input/output supply current		[3]	-	20	-	20	µA
$I_{DD(SD)}$	SD supply current			-	0.5	-	0.5	µA

[1] X1_CLK = 3.3 V only.

[2] I_{DD} is the supply on V_{DD} and V_{DDA}.

[3] $I_{DD(IO)}$ current might be higher or lower depending on the activity of the 16-bit data bus. The numbers specified in the data sheet are measured with no activity on the host controller bus. The data bus, address bus and control signals are pulled HIGH.

12. Dynamic characteristics

Table 18. Dynamic characteristics for 16-bit host bus interface

Symbol	Parameter	Conditions	$V_{DD(IO)}$ = 2.5 V		$V_{DD(IO)}$ = 3.3 V		Unit
			Min	Max	Min	Max	
$t_{WL(X1\_CLK)}$	X1_CLK pulse width LOW		9	-	9	-	ns
$t_{WH(X1\_CLK)}$	X1_CLK pulse width HIGH		9	-	9	-	ns
f_{X1_CLK}	frequency on pin X1_CLK		-	52	-	52	MHz
$t_{su(A)}$	address set-up time		5	-	5	-	ns
$t_{h(A)}$	address hold time		10	-	5	-	ns
$t_{h(WE-CS)}$	hold time from $\overline{WE}$ to $\overline{CS}$		0	-	0	-	ns
$t_{d(CSL-WEL)}$	delay time from $\overline{CS}$ LOW to $\overline{WE}$ LOW		0	-	0	-	ns
$t_{w(WE)}$	$\overline{WE}$ pulse width		10	-	20	-	ns
$t_{d(WE)}$	$\overline{WE}$ delay time		10	-	20	-	ns
$t_{su(D-WEH)}$	set-up time from data input to $\overline{WE}$ HIGH		5	-	5	-	ns
$t_{h(WEH-D)}$	data input hold time after $\overline{WE}$ HIGH		5	-	5	-	ns
$t_{su(BEn)}$	set-up time on pin $\overline{BEn}$		5	-	5	-	ns
$t_{h(BEn)}$	hold time on pin $\overline{BEn}$		5	-	5	-	ns
$t_{h(RE-CS)}$	hold time from $\overline{RE}$ to $\overline{CS}$		0	-	0		ns
$t_{d(CS-RE)}$	delay time from $\overline{CS}$ to $\overline{RE}$		0	-	0		ns
$t_{w(RE)}$	$\overline{RE}$ pulse width		25	-	20		ns
$t_{d(RE)}$	$\overline{RE}$ delay time		10	-	10		ns
$t_{d(RE-Q)}$	delay time from $\overline{RE}$ to data output	25 pF load	-	20	-	25	ns
$t_{dis(RE-QZ)}$	disable time from $\overline{RE}$ to high-impedance data output	25 pF load	-	20	-	15	ns
$t_{w(RESET)}$	pulse width on pin RESET		10	-	5	-	ns
$t_{d(buf\_full-INTL)}$	delay time from buffer full to $\overline{INT}$ LOW	receive buffer (receive)	-	4XTAL1	-	4XTAL1	ns
$t_{d(int\_clr-INTH)}$	delay time from interrupt clear to $\overline{INT}$ HIGH	receive buffer (read)	-	300	-	300	ns
$t_{d(buf\_emp-INTL)}$	delay time from buffer empty to $\overline{INT}$ LOW	transmit buffer (transmit)	-	4XTAL2	-	4XTAL2	ns
$t_{d(int\_clr-INTH)}$	delay time from interrupt clear to $\overline{INT}$ HIGH	transmit buffer (write)	-	80	-	80	ns
$t_{su(A8)}$	address 8 set-up time		5	-	5	-	ns
$t_{su(A8-CS)}$	set-up time from address 8 to $\overline{CS}$		5	-	5	-	ns
$t_{d(SDCLK-DREQH)}$	delay time from SDCLK to DREQ HIGH		-	20	-	15	ns
$t_{d(CSH-DREQL)W}$	write delay time from $\overline{CS}$ HIGH to DREQ LOW		-	20	-	15	ns
$t_{d(CSH-DREQL)R}$	read delay time from $\overline{CS}$ HIGH to DREQ LOW		-	20	-	15	ns

Table 19. Dynamic characteristics for MMC/SD/SDIO bus interface

$V_{DD(SD)}$ = 2.7 V to 3.3 V.

Symbol	Parameter	Conditions	25 MHz		52 MHz		Unit
			Min	Max	Min	Max	
Clock							
t_{WL}	clock low time	10 pF max.	12	-	8	-	ns
t_{WH}	clock high time	10 pF max.	12	-	8	-	ns
$t_{w(clk)}$	clock pulse width	10 pF max.	40	-	18	-	ns
t_{TLH}	clock rise time	10 pF max.	-	10	-	3	ns
t_{THL}	clock fall time	10 pF max.	-	10	-	3	ns
Input CMD, DATn							
t_{ISU}	input set-up time	10 pF max.	5	-	6	-	ns
t_{IH}	input hold time	10 pF max.	5	-	2	-	ns
Output CMD, DATn							
t_{ODLY}	output delay time	during data transfer mode; 40 pF max.	0	14	-	14	ns
t_{OH}	output hold time		2.5	-	2.5	-	ns

Table 20. Dynamic characteristics for MMC/SD/SDIO bus interface

$V_{DD(SD)}$ = 1.70 V to 1.95 V.

Symbol	Parameter	Conditions	25 MHz		52 MHz		Unit
			Min	Max	Min	Max	
Clock							
t_{WL}	clock low time	10 pF max.	12	-	8	-	ns
t_{WH}	clock high time	10 pF max.	12	-	8	-	ns
$t_{w(clk)}$	clock pulse width	10 pF max.	40	-	18	-	ns
t_{TLH}	clock rise time	10 pF max.	-	10	-	3	ns
t_{THL}	clock fall time	10 pF max.	-	10	-	3	ns
Input CMD, DATn							
t_{ISU}	input set-up time	10 pF max.	5	-	6	-	ns
t_{IH}	input hold time	10 pF max.	5	-	2	-	ns
Output CMD, DATn							
t_{ODLY}	output delay time	during data transfer mode; 40 pF max.	0	14	-	14	ns
t_{OH}	output hold time		2.5	-	2.5	-	ns

12.1 Timing diagrams

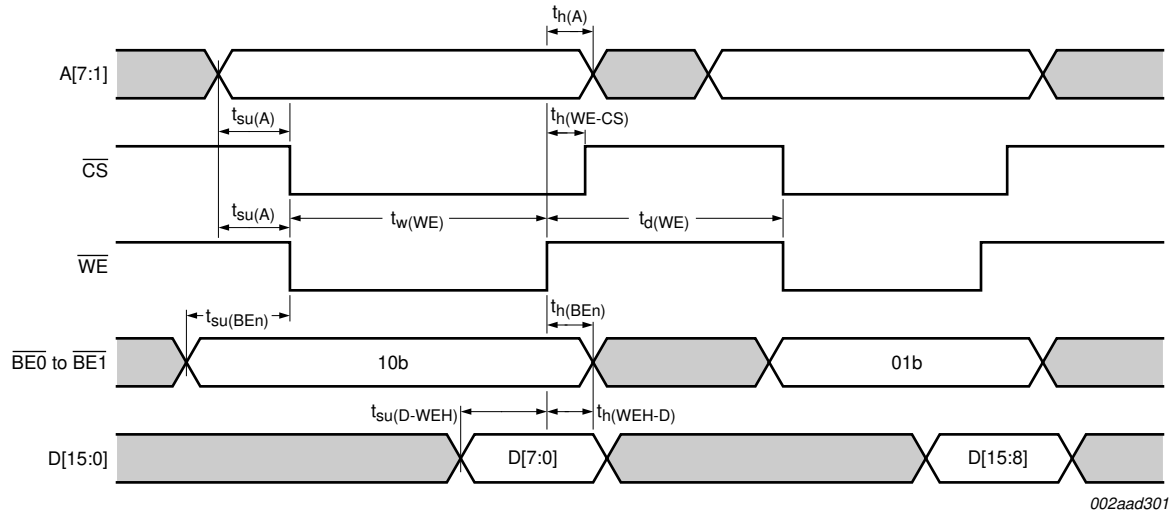


Fig 15. 8-bit write

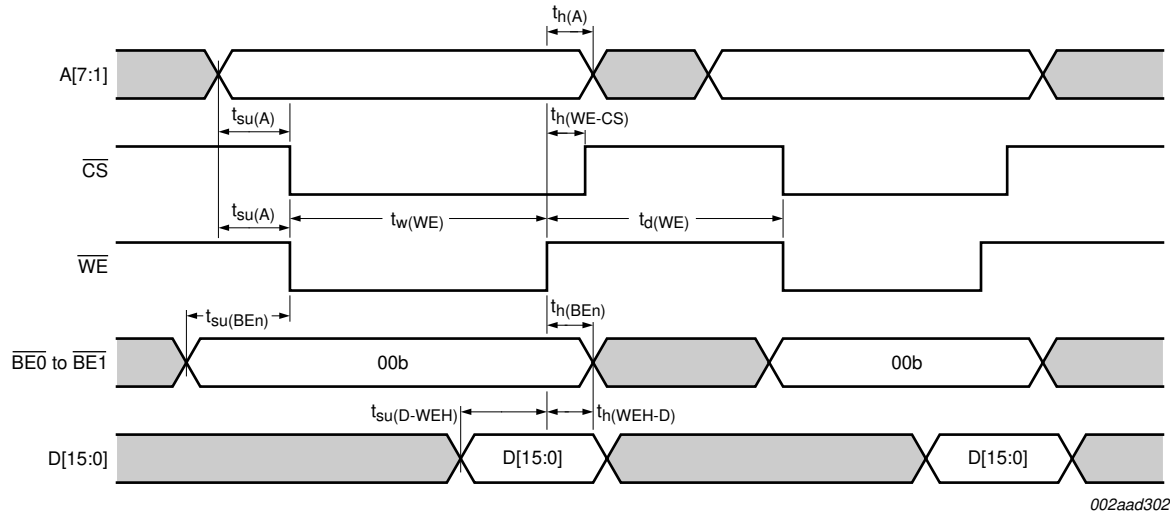


Fig 16. 16-bit write

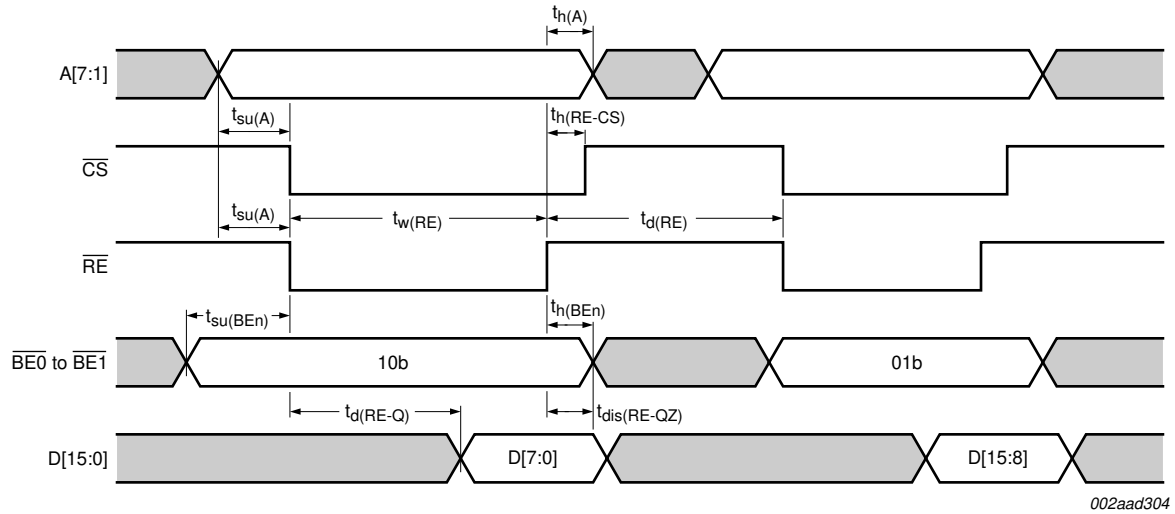


Fig 17. 8-bit read

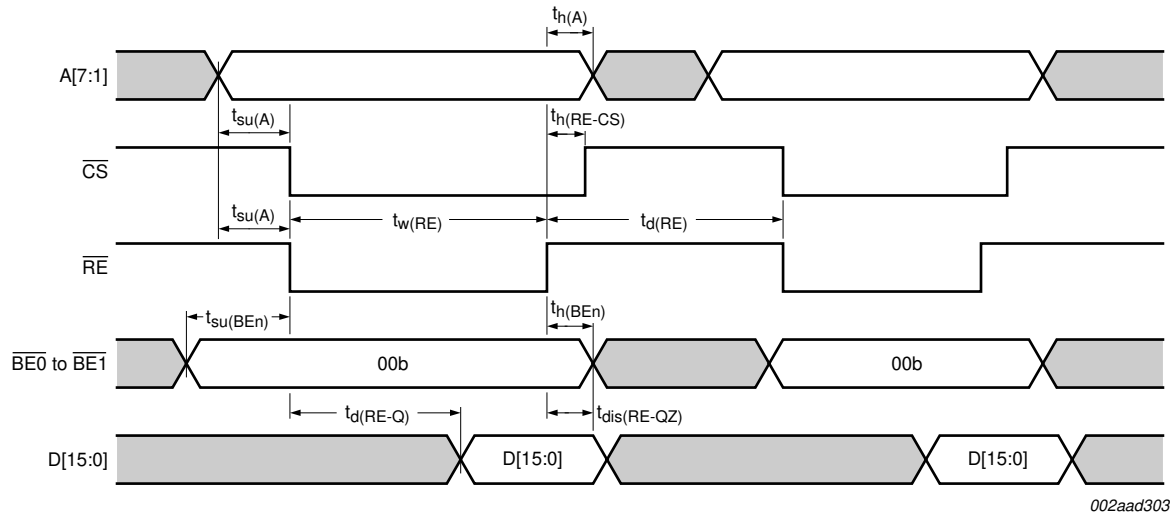


Fig 18. 16-bit read