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SIDACtor® Protection Thyristors Broadband Optimized™ Protection

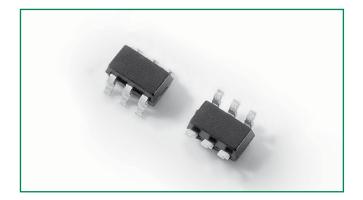
SDP Biased Series - SOT23-6







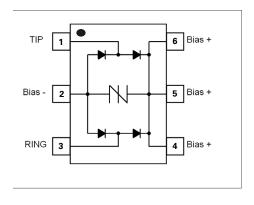




Agency Approvals

Agency	Agency File Number
71	E133083

Pinout Designation & Schematic Symbol



Description

This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount SOT23-6 package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of tertiary protectors.

Features & Benefits

- Compatible with VDSL2 (30MHz) and with G.fast (106MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile

- Response time under 500ns
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- ANSI C62.41
- IEC 61000-4-12
- IEC 61000-4-5, 30A $(t_p=8/20\mu s)$ 2nd edition
- IEC 61000-4-2 level 4
 - 15kV (air discharge)
- -- 8kV (contact discharge)

Additional Information









Absolute Maximum Ratings between pin1 and pin 3, Ta= 25°C (Unless otherwise noted)

Part Number	Marking	Maximum Junction Temperature	Storage Temperature Range	Ι _{pp} 8/20μs
		°C	°C	A Max
SDP0240T023G6RP	P24	150	-65 to 150	30 ¹

Notes:

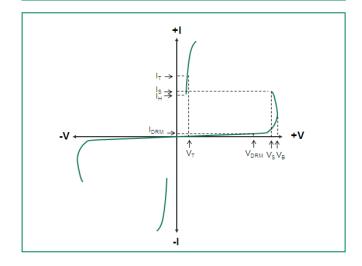
1. The device must be in thermal equilibrium at 25°C

Electrical Characteristics between pin 1 and pin 3, Ta = 25°C

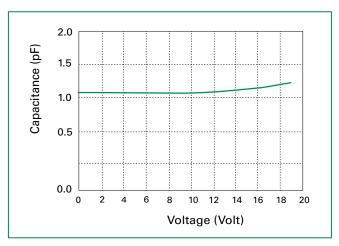
Part Number	Marking	V _{DRM} @I _{DRM} =100nA	I _{DRM} @V _{DRM} =19V	V _s @1V/μs	I _H	l _s	Co@f=1MHz,2V	Delta Co@ Line Bias = 1 V to 19 V
		V min	pA typ	V max	mA typ	mA min	pF max	pF max
SDP0240T023G6RP	P24	19	300	29	40	10	3.0	0.5



V-I: Characteristics



Typical capacitance against line voltage (without external bias)



Surge Ratings

	I _{pp}
Series	1.2/50µs ¹ / 8/20µs ²
	A min
G	30

Notes:

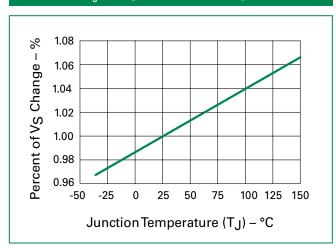
- 1 Voltage waveform in µs
- 2 Current waveform in us
- Peak pulse current rating (I_{pp}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- -The component must be in thermal equilibrium at 25°C.

Thermal Information

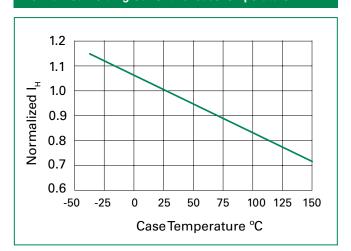
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

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Normalized V_s Change vs. Junction Temperature

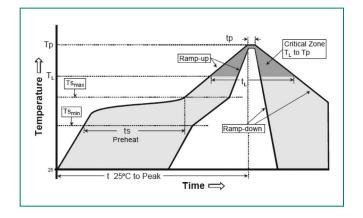


Normalized Holding Current vs. Case Temperature



Soldering Parameters

Reflow Co	ndition	Pb-Free assembly
	-Temperature Min (T _{s(min)})	150°C
Pre Heat	-Temperature Max (T _{s(max)})	200°C
	-Time (Min to Max) (t _s)	60-180 secs.
Average rate to peak)	amp up rate (Liquidus Temp (T _L)	3°C/sec. Max.
$T_{S(max)}$ to T_{L}	- Ramp-up Rate	3°C/sec. Max.
Defless	-Temperature (T _L) (Liquidus)	+217°C
Reflow	-Temperature (t _L)	60-150 secs.
PeakTemp	(T _P)	250(+0/-5)°C
Time with	in 5°C of actual PeakTemp (t _p)	20-40 secs.
Ramp-dov	vn Rate	6°C/sec. Max.
Time 25°C to PeakTemp (T _p)		8 min. Max.
Do not exc	ceed	260°C





Physical Specifications

Lead Plating	SOT23: Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	V-0

- All dimensions are in millimeters.
 Dimensions include solder plating.
- 3. Dimensions are exclusive of mold flash & metal burr.
- 4. All specifications comply to JEDEC MO-178

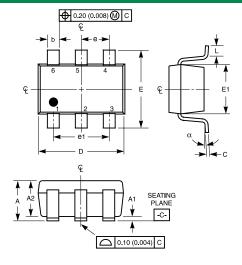
 5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.

 6. Package surface matte tine

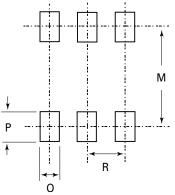
Environmental Specifications

Temp Cycling	Mil-STD-883, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102 No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103 Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020 pre&post preconditioning test.
Wet Humidity (Tin only)	JESD 201 standard: 55°C/85%RH

Dimensions - SOT23-6



К	ecommend	led	Sol	der	Pad	Layout	
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Specifications are subject to change without notice.
Pavisad: 02/22/17

.	Inc	hes	Millin	neters
Dimensions	Min	Max	Min	Max
А	0.041	0.057	1.050	1.450
A1	0.000	0.006	0.000	0.150
A2	0.041	0.051	1.050	1.300
b	0.014	0.020	0.350	0.508
С	0.004	0.008	0.090	0.200
D	0.110	0.118	2.800	3.000
E	0.102	0.118	2.600	3.000
E1	0.057	0.069	1.450	1.750
е	0.037	(BSC)	0.950	(BSC)
e1	0.071	0.075	1.800	1.900
L (note 4.5)	0.004	0.023	0.100	0.600
N (note 6)	(3	(3
α	0°C	10°C	0°C	10°C
M	-	0.102	-	2.590
0	-	0.027	-	0.690
Р	-	0.039	-	0.990
R	-	0.038	-	0.950

- 1. Dimensioning and tolearances per ANSI 14.5M-1982.
 2. Package conforms to EIAJ SC-74 (1992)
 3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
- 4. Foot lenth L measured at reference to seating plane.
- 5. "L" is the length of flat foot surface for soldering to substrate.
- 6. "N" is the number of terminal positions.
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

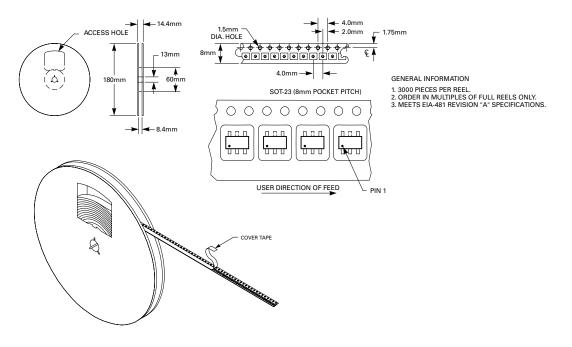
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Part Numbering SDP 024 0 T023 G 6 RP Type SIDACtor DSL Protector Nominal Working voltage: Nominal Working voltage: Surge lpp rating Package Type Package Type Part Marking Part Marking

Packing Options

PackageType	Description	Quantity
SOT23-6	Tape and Reel	3000

Embossed Carrier Tape & Reel Specification - SOT23-6



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