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SE97

DDR memory module temp sensor with integrated SPD, 3.3 V

Rev. 07 — 29 January 2010 Product data sheet

1. General description

The NXP Semiconductors SE97 measures temperature from −40 °C to +125 °C with JEDEC Grade B ±1 °C accuracy between +75 °C and +95 °C and also provide 256 bytes of EEPROM memory communicating via the I²C-bus/SMBus. It is typically mounted on a Dual In-line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Temperature Sensor Component* specification and also replacing the Serial Presence Detect (SPD) which is used to store memory module and vendor information.

The SE97 thermal sensor operates over the V_{DD} range of 3.0 V to 3.6 V and the EEPROM over the range of 3.0 V to 3.6 V write and 1.7 V to 3.6 V read.

Placing the Temp Sensor (TS) on a DIMM allows accurate monitoring of the DIMM module temperature to better estimate the DRAM case temperature (T_{case}) to prevent it from exceeding the maximum operating temperature of 85 °C. The chip set throttles the memory traffic based on the actual temperatures instead of the calculated worst-case temperature or the ambient temperature using a temp sensor mounted on the motherboard. There is up to 30 % improvement in thin and light notebooks that are using one or two 1 GB SO-DIMM modules. The TS is required on DDR3 RDIMM and RDIMM ECC. Future uses of the TS will include more dynamic control over thermal throttling, the ability to use the Alarm Window to create multiple temperature zones for dynamic throttling and to save processor time by scaling the memory refresh rate.

The TS consists of a ΔΣ Analog-to-Digital Converter (ADC) that monitors and updates its own temperature readings 10 times per second, converts the reading to a digital data, and latches them into the data temperature register. User-programmable registers, the specification of upper/lower alarm and critical temperature trip points, $\overline{\text{EVENT}}$ output control, and temperature shutdown, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE97 outputs an $\overline{\text{EVENT}}$ signal using an open-drain output that can be pulled up between 0.9 V and 3.6 V. The user has the option of setting the $\overline{\text{EVENT}}$ output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The $\overline{\text{EVENT}}$ output can even be configured as a critical temperature output.

The EEPROM is designed specifically for DRAM DIMMs SPD. The lower 128 bytes (address 00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. This allows DRAM vendor and product information to be stored and write protected. The upper 128 bytes (address 80h to FFh) are not write protected and can be used for general purpose data storage.

The SE97 has a single die for both the temp sensor and EEPROM for higher reliability and supports the industry-standard 2-wire I^{2}C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identity of the device. Three address pins allow up to eight devices to be controlled on a single bus.

2. Features

2.1 General features

- JEDEC (JC-42.4) TSE 2002B3 DIMM ± 0.5 °C (typ.) between 75 °C and 95 °C temperature sensor plus 256-byte serial EEPROM for Serial Presence Detect (SPD)
- Optimized for voltage range: 3.0 V to 3.6 V, but SPD can be read down to 1.7 V
- Shutdown current: 0.1 μA (typ.) and 5.0 μA (max.)
- 2-wire interface: I^{2}C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus ALERT Response Address and TIMEOUT (programmable)
- ESD protection exceeds 2500 V HBM per JESD22-A114, 250 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Available packages: TSSOP8, HVSON8, HXSON8, HWSON8 (JEDEC PSON8 VCED-3)

2.2 Temperature sensor features

- 11-bit ADC Temperature-to-Digital converter with 0.125 °C resolution
- Operating current: 250 μA (typ.) and 400 μA (max.)
- Programmable hysteresis threshold: off, 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature $\overline{\text{EVENT}}$ output
- B grade accuracy:
  - ±0.5 °C/±1 °C (typ./max.) → +75 °C to +95 °C
  - ±1.0 °C/±2 °C (typ./max.) → +40 °C to +125 °C
  - ±2.0 °C/±3 °C (typ./max.) → −40 °C to +125 °C

2.3 Serial EEPROM features

- Operating current:
  - Write → 0.6 mA (typ.) for 3.5 ms (typ.)
  - Read → 100 μA (typ.)
- Organized as 1 block of 256 bytes [(256 × 8) bits]
- 100,000 write/erase cycles and 10 years of data retention
- Permanent and Reversible Software Write Protect
- Software Write Protection for the lower 128 bytes

3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking
- Hard disk drives and other PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE97PW	SE97	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE97TK	SE97	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1
SE97TL[1]	97L	HXSON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.5 mm	SOT1052-1
SE97TP[1][2][3]	S97	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-1
SE97TP/S900[1][2][3]	S97	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-2

[1] SE97TL and SE97TP offer improved $V_{POR}/\overline{EVENT}$ I_{OL}.

[2] Industry standard 2 mm × 3 mm × 0.8 mm package to JEDEC VCED-3 PSON8 in 8 mm × 4 mm pitch tape 4 k quantity reels.

[3] SOT1069-1 is manufactured in APHK Hong Kong and SOT1069-2 is manufactured in APB Bangkok. The third line of the topside marking will start with ‘P’ for SPHK and ‘n’ for APB.

5. Block diagram

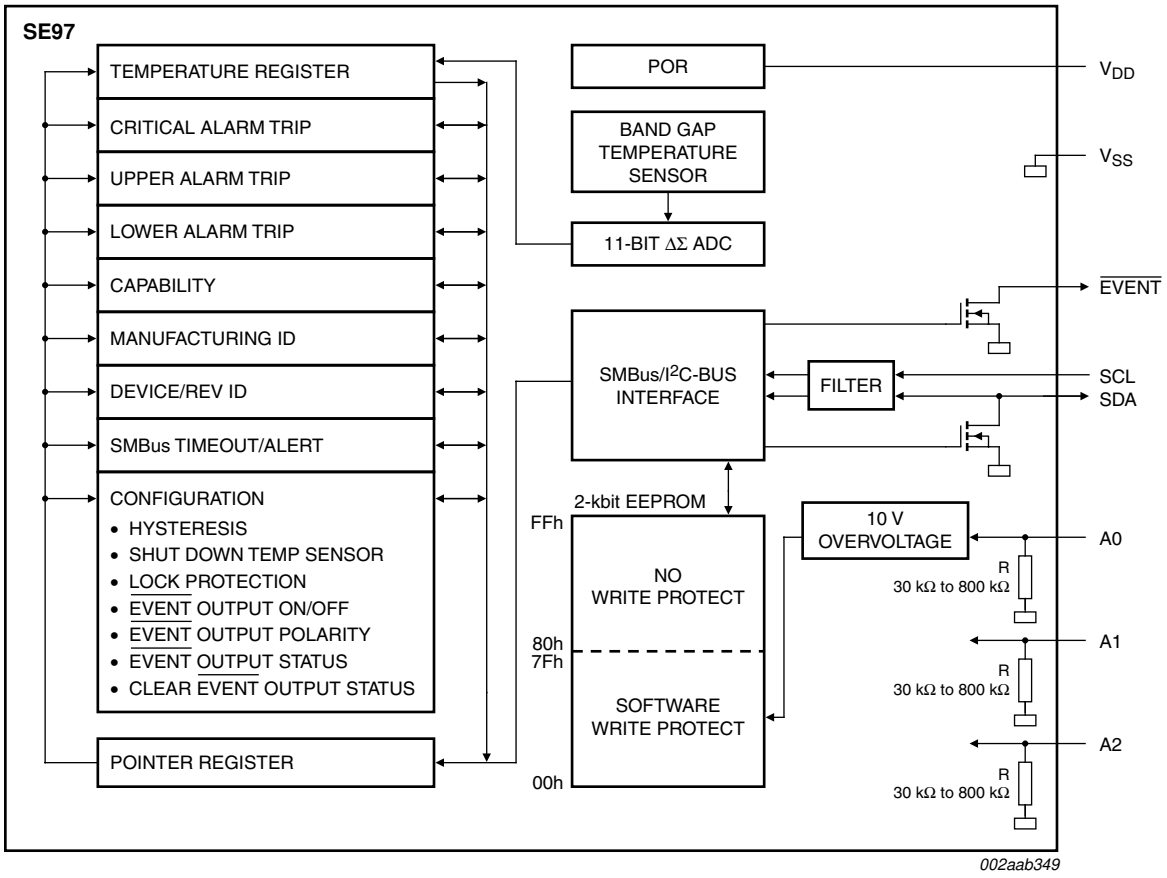


Fig 1. Block diagram of SE97

6. Pinning information

6.1 Pinning

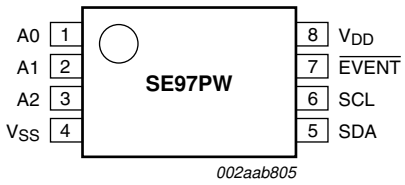


Fig 2. Pin configuration for TSSOP8

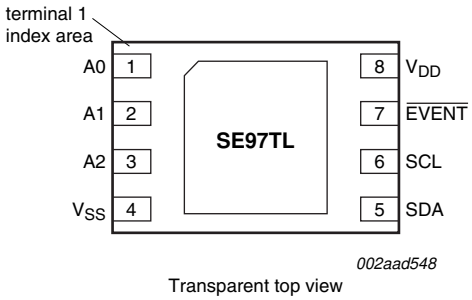


Fig 3. Pin configuration for HXSON8

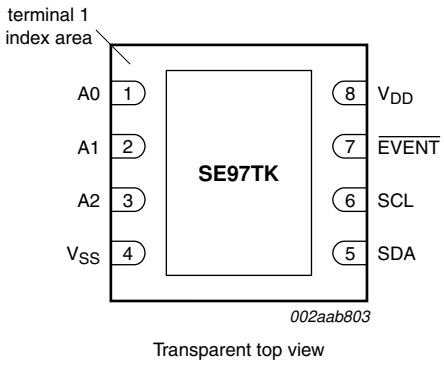


Fig 4. Pin configuration for HVSON8

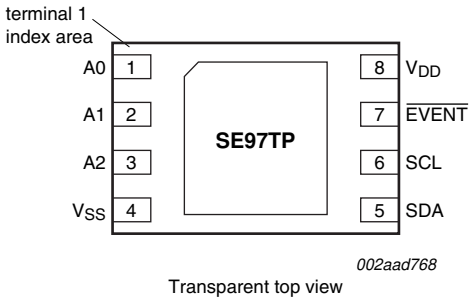


Fig 5. Pin configuration for HWSON8 (SOT1069-1)

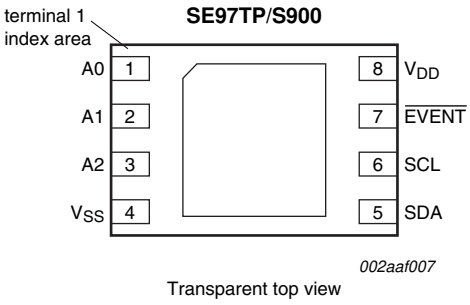


Fig 6. Pin configuration for HWSON8 (SOT1069-2)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	1	I	I^2C-bus/SMBus slave address bit 0 with internal pull-down. This input is overvoltage tolerant to support software write protection.
A1	2	I	I^2C-bus/SMBus slave address bit 1 with internal pull-down
A2	3	I	I^2C-bus/SMBus slave address bit 2 with internal pull-down
V_{SS}	4	ground	device ground
SDA	5	I/O	SMBus/I^2C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I^2C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
$\overline{\text{EVENT}}$	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V_{DD}	8	power	device power supply (3.0 V to 3.6 V); supports 1.7 V for EEPROM read only.

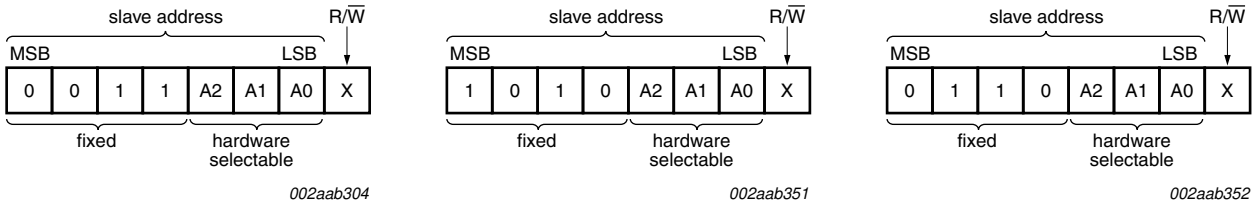
7. Functional description

7.1 Serial bus interface

The SE97 communicates with a host controller by means of the 2-wire serial bus (I^2C-bus/SMBus) that consists of a serial clock (SCL) and serial data (SDA) signals. The device supports SMBus, I^2C-bus Standard-mode and Fast-mode. The I^2C-bus standard speed is defined to have bus speeds from 0 Hz to 100 kHz, I^2C-bus fast speed from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE97 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one byte at a time with the Most Significant Bit (MSB) is transferred first. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

7.2 Slave address

The SE97 uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to coexist on the same bus. The A0, A1 and A2 pins are pulled LOW internally. The A0 pin is also overvoltage tolerant supporting 10 V software write protect. When it is driven higher than 7.8 V, writing a special command would put the EEPROM in reversible write protect mode (see Section 7.10.2 “Memory protection”). Each pin is sampled at the start of each I^2C-bus/SMBus access. The temperature sensor’s fixed address is ‘0011b’. The EEPROM’s fixed address for the normal EEPROM read/write is ‘1010b’, and for EEPROM software protection command is ‘0110b’. Refer to Figure 7.



a. Temperature sensor

b. EEPROM (normal read/write)

c. EEPROM (software protection command)

Fig 7. Slave address

7.3 $\overline{\text{EVENT}}$ output condition

The $\overline{\text{EVENT}}$ output indicates conditions such as the temperature crossing a predefined boundary. The $\overline{\text{EVENT}}$ modes are very configurable and selected using the configuration register (CONFIG). The interrupt mode or comparator mode is selected using CONFIG[0], using either TCRIT/UPPER/LOWER or TCRIT only temperature bands (CONFIG[2]) as modified by hysteresis (CONFIG[10:9]). The UPPER/LOWER (CONFIG[6]) and TCRIT (CONFIG[7]) bands can be locked. Figure 8 shows an example of the measured temperature versus time, with the corresponding behavior of the $\overline{\text{EVENT}}$ output in each of these modes.

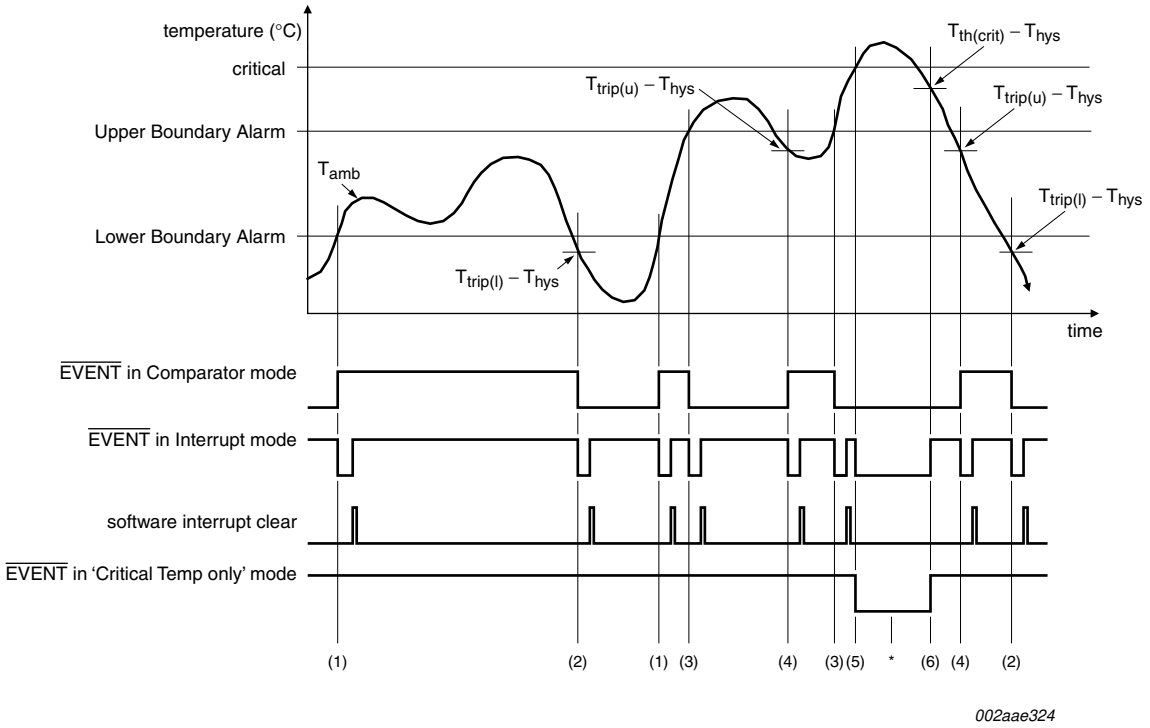
Upon device power-up, the default condition for the $\overline{\text{EVENT}}$ output is high-impedance to prevent spurious or unwanted alarms, but can be later enabled (CONFIG[3]). $\overline{\text{EVENT}}$ output polarity can be set to active HIGH or active LOW (CONFIG[1]). $\overline{\text{EVENT}}$ status can be read (CONFIG[4]) and cleared (CONFIG[5]).

- **Advisory note:**
  - NXP device: After power-up, bit 3 (1) and bit 2 or bit 0 (leave as 0 or 1) can be set at the same time (e.g., in same byte) but once bit 3 is set (1) then changing bit 2 or bit 0 has no effect on the device operation.
  - Competitor device: Does not require that bit 3 be cleared (e.g., set back to (0)) before changing bit 2 or bit 0.
  - Work-around: In order to change bit 2 or bit 0 once bit 3 (1) is set, bit 3 (0) must be cleared in one byte and then change bit 2 or bit 0 and reset bit 3 (1) in the next byte.
  - SE97B will allow bit 2 or bit 0 to be changed even if bit 3 is set.

If the device enters Shutdown mode (CONFIG[8]) with asserted $\overline{\text{EVENT}}$ output, the output remains asserted during shutdown.

7.3.1 $\overline{\text{EVENT}}$ pin output voltage levels and resistor sizing

The $\overline{\text{EVENT}}$ open-drain output is typically pulled up to a voltage level from 0.9 V to 3.6 V with an external pull-up resistor, but there is no real lower limit on the pull-up voltage for the $\overline{\text{EVENT}}$ pin since it is simply an open-drain output. It could be pulled up to 0.1 V and would not affect the output. From the system perspective, there will be a practical limit. That limit will be the voltage necessary for the device monitoring the interrupt pin to detect a HIGH on its input. A possible practical limit for a CMOS input would be 0.4 V. Another thing to consider is the value of the pull-up resistor. When a low supply voltage is applied to the drain (through the pull-up resistor) it is important to use a higher value pull-up resistor, to allow a larger maximum signal swing on the $\overline{\text{EVENT}}$ pin.



Refer to Table 3 for figure note information.

Fig 8. $\overline{\text{EVENT}}$ output condition

Table 3. $\overline{\text{EVENT}}$ output condition

Figure note	$\overline{\text{EVENT}}$ output boundary conditions	$\overline{\text{EVENT}}$ output			Temperature Register Status bits		
		Comparator mode	Interrupt mode	Critical Temp only mode	Bit 15 Above Critical Trip	Bit 14 Above Alarm Window	Bit 13 Below Alarm Window
(1)	$T_{amb} \geq T_{trip(l)}$	H	L	H	0	0	0
(2)	$T_{amb} < T_{trip(l)} - T_{hys}$	L	L	H	0	0	1
(3)	$T_{amb} > T_{trip(u)}$	L	L	H	0	1	0
(4)	$T_{amb} \leq T_{trip(u)} - T_{hys}$	H	L	H	0	0	0
(5)	$T_{amb} \geq T_{th(crit)}$	L	L	L	1	1	0
(6)	$T_{amb} < T_{th(crit)} - T_{hys}$	L	H	H	0	1	0

When $T_{amb} \geq T_{th(crit)}$ and $T_{amb} < T_{th(crit)} - T_{hys}$ the $\overline{\text{EVENT}}$ output is in Comparator mode and bit 0 of CONFIG ($\overline{\text{EVENT}}$ output mode) is ignored.

7.3.2 $\overline{\text{EVENT}}$ thresholds

7.3.2.1 Alarm window

The device provides a comparison window with an UPPER trip point and a LOWER trip point, programmed through the Upper Boundary Alarm Trip register (02h), and Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point as modified by hysteresis as programmed in the Configuration register. When enabled, the $\overline{\text{EVENT}}$ output triggers whenever entering or exiting (crossing above or below) the alarm window.

- **Advisory note:**
  - NXP Device: The $\overline{\text{EVENT}}$ output can be cleared through the Clear $\overline{\text{EVENT}}$ bit (CEVNT) or SMBus ALERT.
  - Competitor Device: The $\overline{\text{EVENT}}$ output can be cleared only through the Clear $\overline{\text{EVENT}}$ bit (CEVNT).
  - Work-around: Only clear $\overline{\text{EVENT}}$ output using the Clear $\overline{\text{EVENT}}$ bit (CEVNT).
  - There will be no change to NXP devices.

The Upper Boundary Alarm Trip should always be set above the Lower Boundary Alarm Trip.

- **Advisory note:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the alarm window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating $\overline{\text{EVENT}}$ output.
  - Competitor devices: Compares the alarm limit with temperature register at any time, so they get the $\overline{\text{EVENT}}$ output immediately when new UPPER or LOWER Alarm Windows and the $\overline{\text{EVENT}}$ output are set at the same time.
  - Work-around: Wait at least 125 ms before enabling $\overline{\text{EVENT}}$ output (EOCTL = 1).
  - SE97B will compare alarm window and temperature register immediately.

7.3.2.2 Critical trip

The $T_{th(crit)}$ temperature setting is programmed in the Critical Alarm Trip register (04h) as modified by hysteresis as programmed in the Configuration register. When the temperature reaches the critical temperature value in this register (and $\overline{\text{EVENT}}$ is enabled), the $\overline{\text{EVENT}}$ output asserts and cannot be de-asserted until the temperature drops below the critical temperature threshold. The Event cannot be cleared through the Clear $\overline{\text{EVENT}}$ bit (CEVNT) or SMBus ALERT.

The Critical Alarm Trip should always be set above the Upper Boundary Alarm Trip.

- **Advisory note:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the Alarm Window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating $\overline{\text{EVENT}}$ output.

- Competitor devices: Compares the Alarm Window with temperature register at any time, so they get the $\overline{\text{EVENT}}$ output immediately when new $T_{th(crit)}$ and $\overline{\text{EVENT}}$ output are set at the same time.
- Work-around: Wait at least 125 ms before enabling $\overline{\text{EVENT}}$ output (EOCTL = 1). Intel will change Nehalem BIOS so that $T_{th(crit)}$ is set for more than 125 ms before $\overline{\text{EVENT}}$ output is enabled and Event value is checked.
  1. Set $T_{th(crit)}$.
  2. Doing something else (make sure that exceeds 125 ms).
  3. Enable the $\overline{\text{EVENT}}$ output (EOCTL = 1).
  4. Wait 20 μs.
  5. Read Event value.
- SE97B will compare alarm window and temperature register immediately.

7.3.3 $\overline{\text{EVENT}}$ operation modes

7.3.3.1 Comparator mode

In comparator mode, the $\overline{\text{EVENT}}$ output behaves like a window-comparator output that asserts when the temperature is outside the window (e.g., above the value programmed in the Upper Boundary Alarm Trip register or below the value programmed in the Lower Boundary Alarm Trip register or above the Critical Alarm Trip resister if $T_{th(crit)}$ only is selected). Reads/writes on the registers do not affect the $\overline{\text{EVENT}}$ output in comparator mode. The $\overline{\text{EVENT}}$ signal remains asserted until the temperature goes inside the alarm window or the window thresholds are reprogrammed so that the current temperature is within the alarm window.

The comparator mode is useful for thermostat-type applications, such as turning on a cooling fan or triggering a system shutdown when the temperature exceeds a safe operating range.

7.3.3.2 Interrupt mode

In interrupt mode, $\overline{\text{EVENT}}$ asserts whenever the temperature crosses an alarm window threshold. After such an event occurs, writing a 1 to the Clear $\overline{\text{EVENT}}$ bit (CEVNT) in the configuration register de-asserts the $\overline{\text{EVENT}}$ output until the next trigger condition occurs.

In interrupt mode, $\overline{\text{EVENT}}$ asserts when the temperature crosses the alarm upper boundary. If the $\overline{\text{EVENT}}$ output is cleared and the temperature continues to increase until it crosses the critical temperature threshold, $\overline{\text{EVENT}}$ asserts again. Because the temperature is greater than the critical temperature threshold, a Clear $\overline{\text{EVENT}}$ command does not clear the $\overline{\text{EVENT}}$ output. Once the temperature drops below the critical temperature, $\overline{\text{EVENT}}$ de-asserts immediately.

- **Advisory note:**
  - NXP device: If the $\overline{\text{EVENT}}$ output is not cleared before the temperature goes above the critical temperature threshold $\overline{\text{EVENT}}$ de-asserts immediately when temperature drops below the critical temperature.
  - Competitor devices: If the $\overline{\text{EVENT}}$ output is not cleared before or when the temperature is in the critical temperature threshold, $\overline{\text{EVENT}}$ will remain asserted after the temperature drops below the critical temperature until a Clear $\overline{\text{EVENT}}$ command.

– Work-around: Always clear the $\overline{\text{EVENT}}$ output before temperature exceeds the critical temperature.
– SE97B will keep $\overline{\text{EVENT}}$ asserted after the temperature drops below the critical temperature until a Clear $\overline{\text{EVENT}}$ command de-asserts $\overline{\text{EVENT}}$.

7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE97's conversion rate is at least 8 Hz or 125 ms.

7.4.1 What temperature is read when conversion is in progress

The SE97 has been designed to ensure a valid temperature is always available. When a read to the temperature register is initiated through the SMBus, the device checks to see if the temperature conversion process (Analog-to-Digital conversion) is complete and a new temperature is available:

- If the temperature conversion process is complete, then the new temperature value is sent out on the SMBus.
- If the temperature conversion process in **not** complete, then the previous temperature value is sent out on the SMBus.

It is possible that while SMBus Master is reading the temperature register, a new temperature conversion completes. However, this will not affect the data (MSB or LSB) that is being shifted out. On the next read of the temperature register, the new temperature value will be shifted out.

7.5 Power-up default condition

After power-on, the SE97 is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared; $\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to '00h'
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to '0017h' for the B grade
- Operational mode: comparator
- SMBus register is defaulted to '00h'

7.6 Device initialization

SE97 temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain $\overline{\text{EVENT}}$ output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT

feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

Table 4 shows the default values and the example value to be programmed to these registers.

Table 4. Registers to be initialized

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register • hysteresis = 1.5 °C • $\overline{\text{EVENT}}$ output = Interrupt mode • $\overline{\text{EVENT}}$ output is enabled
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = −20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

7.7 SMBus time-out

The SE97 supports SMBus time-out feature. If the host holds SCL LOW between 25 ms and 35 ms, the SE97 would reset its internal state machine to the bus IDLE state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a '1' to bit 7 of register 22h.

Remark: When SMBus time-out is enabled, the I^2C-bus minimum bus speed is limited by the SMBus time-out specification limit of 10 kHz.

The SE97 has no SCL driver, so it cannot hold the SCL line LOW.

Remark: SMBus time-out works over the entire supply range of 1.7 V to 3.6 V unless the shutdown bit (SHMD) is set and turns off the oscillator.

7.8 SMBus ALERT Response Address (ARA)

The SE97 supports SMBus ALERT when it is programmed for the Interrupt mode and when the $\overline{\text{EVENT}}$ polarity bit is set to '0'. The $\overline{\text{EVENT}}$ pin can be ANDed with other $\overline{\text{EVENT}}$ or interrupt signals from other slave devices to signal their intention to communicate with the host controller. When the host detects $\overline{\text{EVENT}}$ or other interrupt signal LOW, it issues an ARA to which a slave device would respond with its address. When there are multiple slave devices generating an ALERT the SE97 performs bus arbitration with the other slaves. If it wins the bus, it responds to the ARA and then clears the $\overline{\text{EVENT}}$ pin.

Remark: Either in comparator mode or when the SE97 crosses the critical temperature, the host must also read the $\overline{\text{EVENT}}$ status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the $\overline{\text{EVENT}}$ pin will not get de-asserted.

Remark: In the SE97 the ARA is set to default ON. However, in the SE97B the ARA will be set to default OFF since ARA is not anticipated to be used in DDR3 DIMM applications.

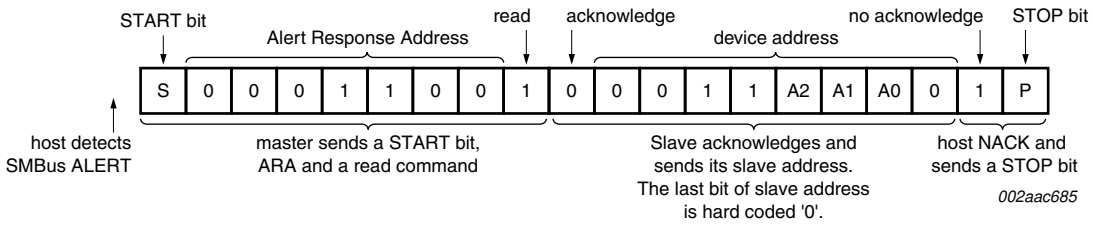


Fig 9. How SE97 responds to SMBus ALERT Response Address

7.9 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to ‘00h’, the location for the Capability register. The Pointer register latches the last location to which it was set. Each data register falls into one of three types of user accessibility:

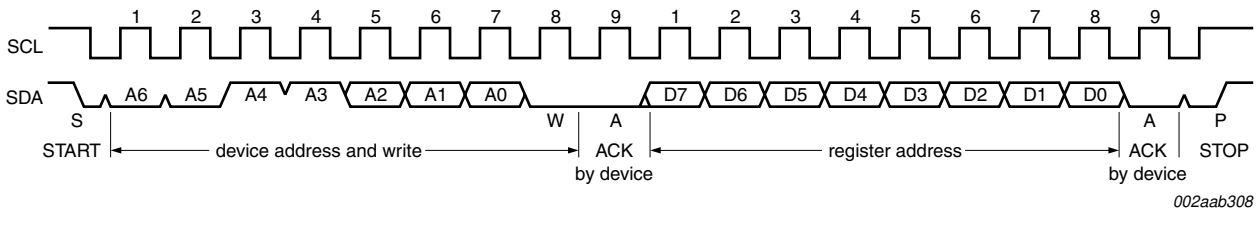
- Read only
- Write only
- Write/Read same address

A ‘write’ to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

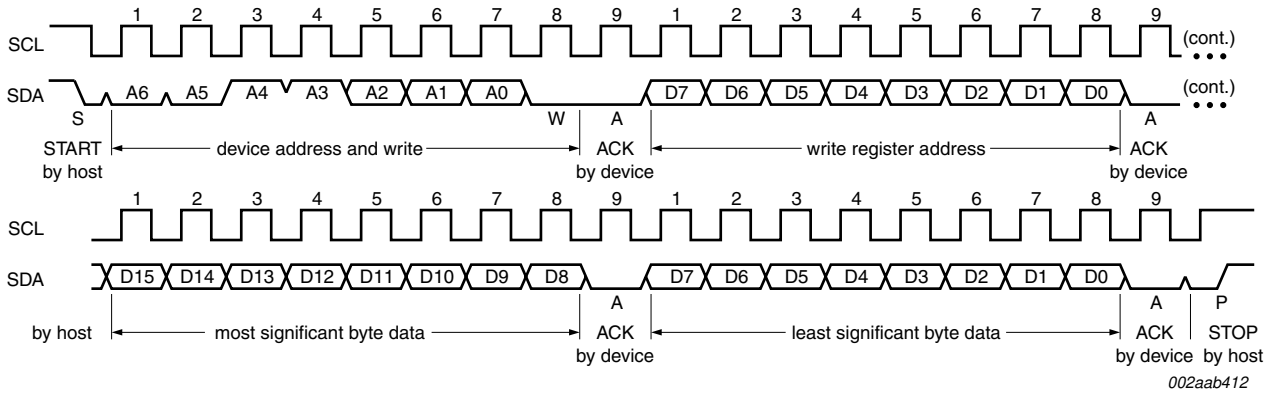
- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Temperature register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to timing diagrams Figure 10 to Figure 13 for how to program the device.



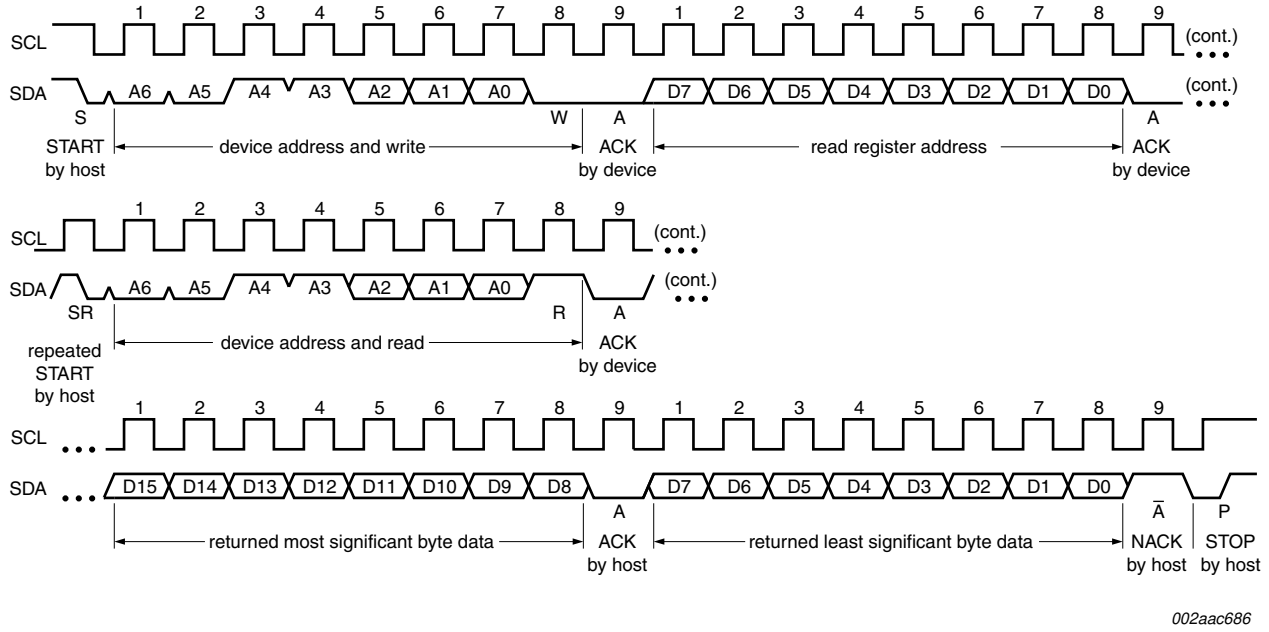
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 10. SMBus/I²C-bus write to the Pointer register



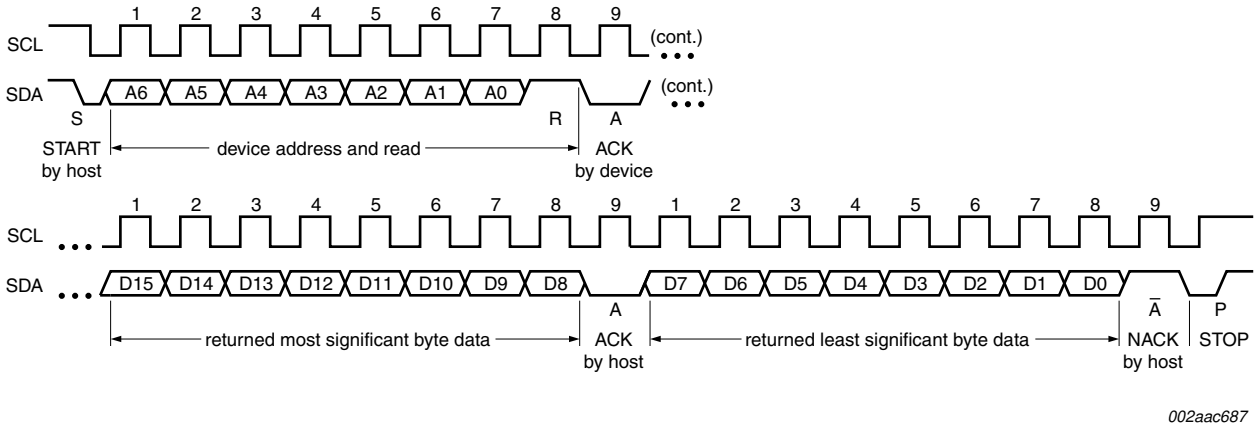
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 11. SMBus/I²C-bus write to the Pointer register followed by a write data word



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 12. SMBus/I²C-bus write to Pointer register followed by a repeated START and an immediate data word read



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 13. SMBus/I²C-bus word read from register with a pre-set pointer

7.10 EEPROM operation

The 2-kbit EEPROM is organized as either 256 bytes of 8 bits each (byte mode), or 16 pages of 16 bytes each (page mode). Accessing the EEPROM in byte mode or page mode is automatic; partial page write of 2 bytes, 4 bytes, or 8 bytes is also supported. Communication with the EEPROM is via the 2-wire serial I^{2}C-bus or SMBus. Figure 14 provides an overview of the EEPROM partitioning.

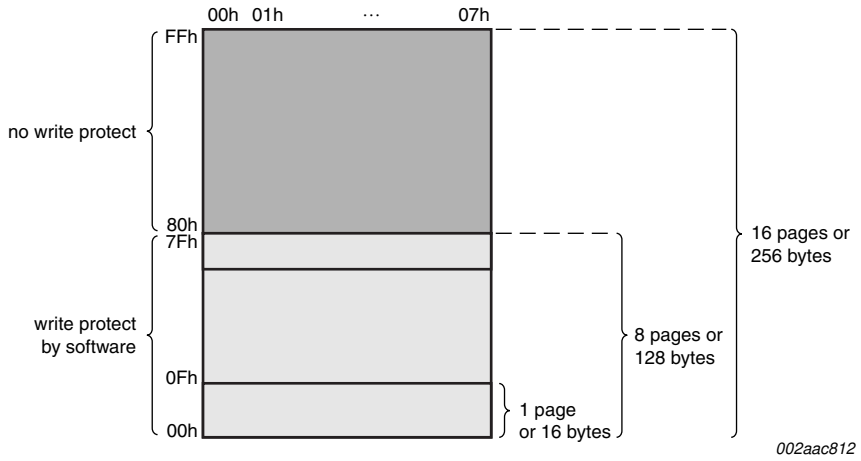


Fig 14. EEPROM partitioning

The EEPROM can be read over voltage range 1.7 V to 3.6 V, but all write operations must be done 3.0 V to 3.6 V.

7.10.1 Write operations

7.10.1.1 Byte Write

In Byte Write mode the master creates a START condition and then broadcasts the slave address, byte address, and data to be written. The slave acknowledges all 3 bytes by pulling down the SDA line during the ninth clock cycle following each byte. The master creates a STOP condition after the last ACK from the slave, which then starts the internal write operation (see Figure 15). During internal write, the slave will ignore any read/write request from the master.

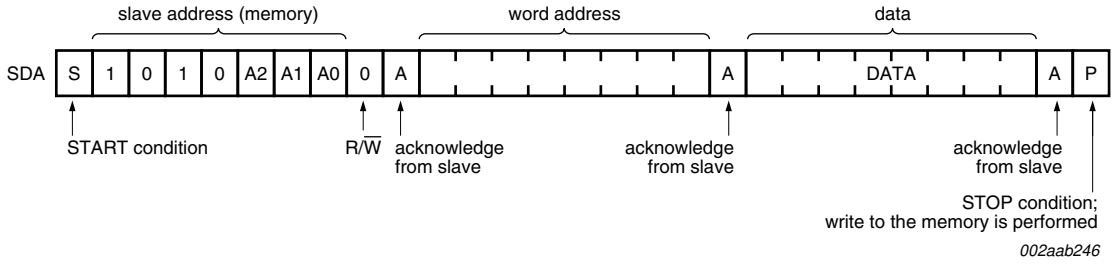


Fig 15. Byte Write timing

7.10.1.2 Page Write

The SE97 contains 256 bytes of data, arranged in 16 pages of 16 bytes each. The page is selected by the four Most Significant Bits (MSB) of the address byte presented to the device after the slave address, while the four Least Significant Bits (LSB) point to the byte within the page. By loading more than one data byte into the device, up to an entire page can be written in one write cycle (see Figure 16). The internal byte address counter will increment automatically after each data byte. If the master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a wrap-around fashion within the selected page. The internal write cycle is started following the STOP condition created by the master.

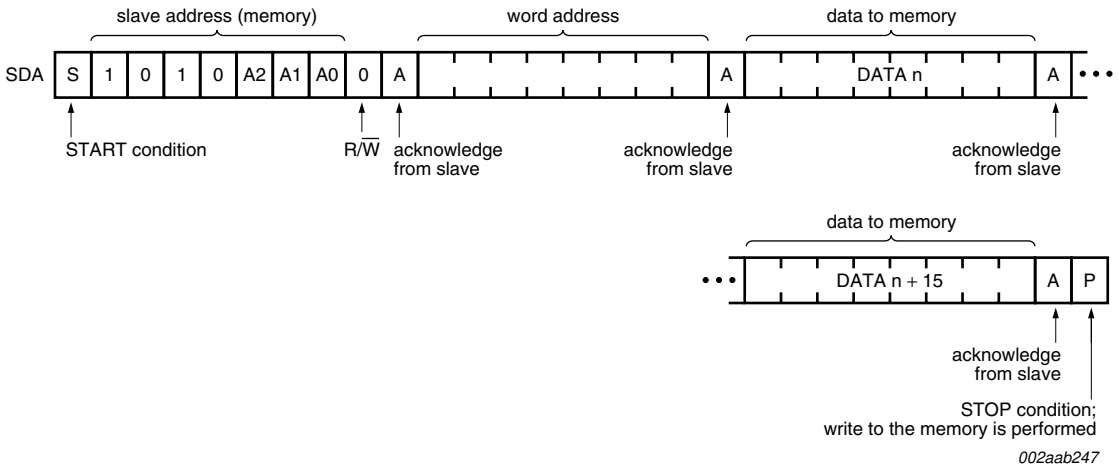


Fig 16. Page Write timing

7.10.1.3 Acknowledge polling

Acknowledge polling can be used to determine if the SE97 is busy writing or is ready to accept commands. Polling is implemented by sending a 'Selective Read' command (described in Section 7.10.3 "Read operations") to the device. The SE97 will not acknowledge the slave address as long as internal write is in progress.

7.10.2 Memory protection

The lower half (the first 128 bytes) of the memory can be write protected by special EEPROM commands without an external control pin. The SE97 features three types of memory write protection instructions, and three respective read Protection instructions. The level of write-protection (set or clear) that has been defined using these instructions remained defined even after power cycle.

The memory protection commands are:

- Permanent Write Protection (PWP)
- Reversible Write Protection (RWP)
- Clear Write Protection (CWP)
- Read Permanent Write Protection (RPWP)
- Read Reversible Write Protection (RRWP)
- Read Clear Write Protection (RCWP)

Table 5 is the summary for normal and memory protection instructions.

Table 5. EEPROM commands summary

Command	Fixed address				Hardware selectable address			R/$\overline{W}$
	Bit 7[1]	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal EEPROM read/write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Reversible Write Protection (RWP)	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	0
Clear Reversible Write Protection (CRWP)	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	0
Permanent Write Protection (PWP)[2]	0	1	1	0	A2	A1	A0	0
Read RWP	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	1
Read CRWP	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	1
Read PWP	0	1	1	0	A2	A1	A0	1

[1] The most significant bit, bit 7, is sent first.

[2] A0, A1, and A2 are compared against the respective external pins on the SE97.

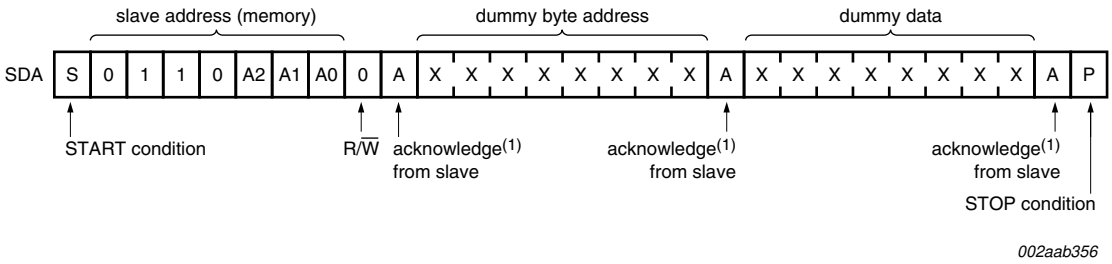
[3] $V_{I(ov)}$ ranges from 7.8 V to 10 V.

This special EEPROM command consists of a unique 4-bit fixed address (0110b) and the voltage level applied on the 3-bit hardware address. Normally, to address the memory array, the 4-bit fixed address is '1010b'. To access the memory protection settings, the 4-bit fixed address is '0110b'. Figure 17 and Figure 18 show the write and read protection sequence, respectively.

Up to eight memory devices can be connected on a single I^2C-bus. Each one is given a 3-bit on the hardware selectable address (A2, A1, A0) inputs. The device only responds when the 4-bit fixed and hardware selectable bits are matched. The 8th bit is the read/write bit. This bit is set to 1 or 0 for read and write protection, respectively.

The corresponding device acknowledges during the ninth bit time when there is a match on the 7-bit address.

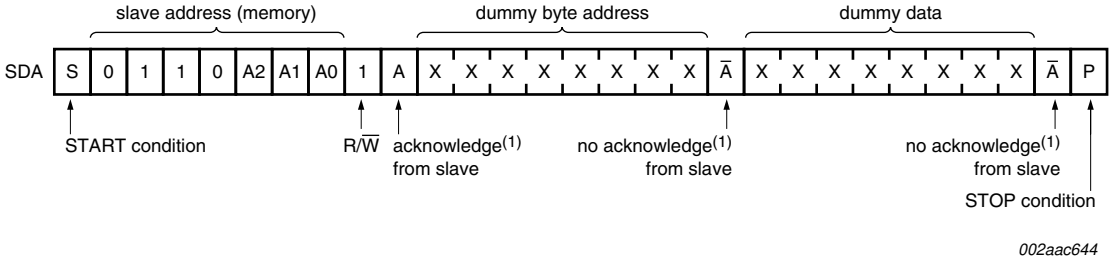
The device does not acknowledge when there is no match on the 7-bit address or when the device is already in permanent write protection mode and is programmed with any write protection instructions (i.e., PWP, RWP, CWP).



X = Don't Care

(1) Refer to Table 6 regarding the exact state of the acknowledge bit.

Fig 17. Software Write Protect (write)



X = Don't Care

(1) Refer to Table 7 regarding the exact state of the acknowledge bit.

Fig 18. Software Write Protect (read)

7.10.2.1 Permanent Write Protection (PWP)

If the software write-protection has been set with the PWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PWP instruction has been successfully executed, the device no longer acknowledges any instruction (with 4-bit fixed address of 0110b) to access the write-protection settings.

7.10.2.2 Reversible Write Protection (RWP) and Clear Reversible Write Protection (CRWP)

If the software write-protection has been set with the RWP instruction, it can be cleared again with a CRWP instruction.

The two instructions, RWP and CRWP have the same format as a Byte Write instruction, but with a different setting for the hardware address pins (as shown in Table 5). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all 'Don't Care' (Figure 17). Another difference is that the voltage, $V_{I(ov)}$, must be applied on the A0 pin, and specific logical levels must be applied on the other two (A1 and A2), as shown in Table 5.

Table 6. Acknowledge when writing data or defining write protection

Instructions with R/$\overline{W}$ bit = 0.

Status	Instruction	ACK	Address	ACK	Data byte	ACK	Write cycle ($T_{cy(W)}$)
Permanently protected	PWP, RWP or CRWP	NACK	not significant	NACK	not significant	NACK	no
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Protected with RWP	RWP	NACK	not significant	NACK	not significant	NACK	no
	CRWP	ACK	not significant	ACK	not significant	ACK	yes
	PWP	ACK	not significant	ACK	not significant	ACK	yes
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Not protected	PWP or RWP	ACK	not significant	ACK	not significant	ACK	yes
	CRWP	ACK	not significant	ACK	not significant	ACK	no
	page or byte write	ACK	address	ACK	data	ACK	yes

7.10.2.3 Read Permanent Write Protection (RPWP), Read Reversible Write Protection (RRWP), and Read Clear Reversible Write Protection (RCRWP)

Read PWP, RWP, and CRWP allow the SE97 to be read in write protection mode. The instruction format is the same as that of the write protection except that the 8th bit, R/$\overline{W}$, is set to 1. Figure 18 shows the instruction format, while Table 7 shows the responses when the instructions are issued.

Table 7. Acknowledge when reading the write protection

Instructions with R/$\overline{W}$ bit = 1.

Status	Instruction	ACK	Address	ACK	Data byte	ACK
Permanently protected	RPWP, RRWP or RCRWP	NACK	not significant	NACK	not significant	NACK
Protected with RWP	RRWP	NACK	not significant	NACK	not significant	NACK
	RCRWP	ACK	not significant	NACK	not significant	NACK
	RPWP	ACK	not significant	NACK	not significant	NACK
Not protected	RPWP, RRWP or RCRWP	ACK	not significant	NACK	not significant	NACK

7.10.3 Read operations

7.10.3.1 Current address read

In Standby mode, the SE97 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If the 'previous' byte was the last byte in memory, then the address counter will point to the first memory byte, and so on. If the SE97 decodes a slave address with a '1' in the R/$\overline{W}$ bit position (Figure 19), it will issue an Acknowledge in the ninth clock cycle and will then transmit the data byte being pointed at by the address counter. The master can then stop further transmission by issuing a No Acknowledge on the ninth bit then followed by a STOP condition.

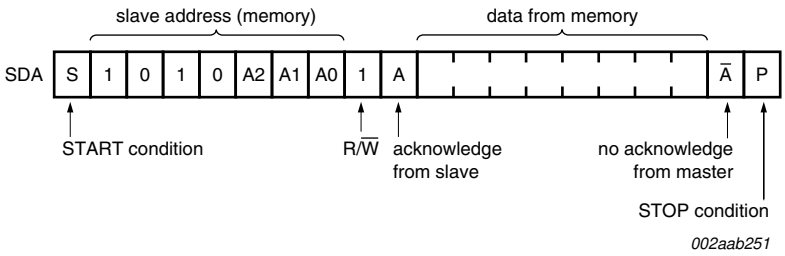


Fig 19. Current address read timing

7.10.3.2 Selective read

The read operation can also be started at an address different from the one stored in the address counter. The address counter can be 'initialized' by performing a 'dummy' write operation (Figure 20). The START condition is followed by the slave address (with the R/$\overline{W}$ bit set to '0') and the desired byte address. Instead of following-up with data, the master then issues a second START, followed by the 'Current Address Read' sequence, as described in Section 7.10.3.1.

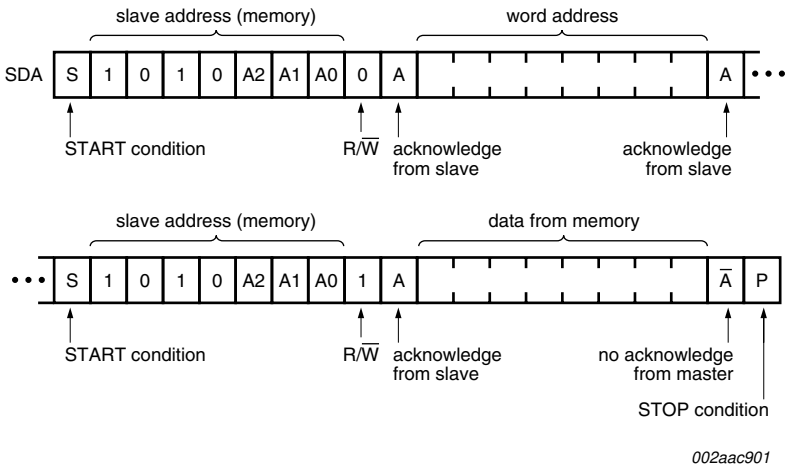


Fig 20. Selective read timing

7.10.3.3 Sequential read

If the master acknowledges the first data byte transmitted by the SE97, then the device will continue transmitting as long as each data byte is acknowledged by the master (Figure 21). If the end of memory is reached during sequential Read, the address counter will 'wrap around' to the beginning of memory, and so on. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

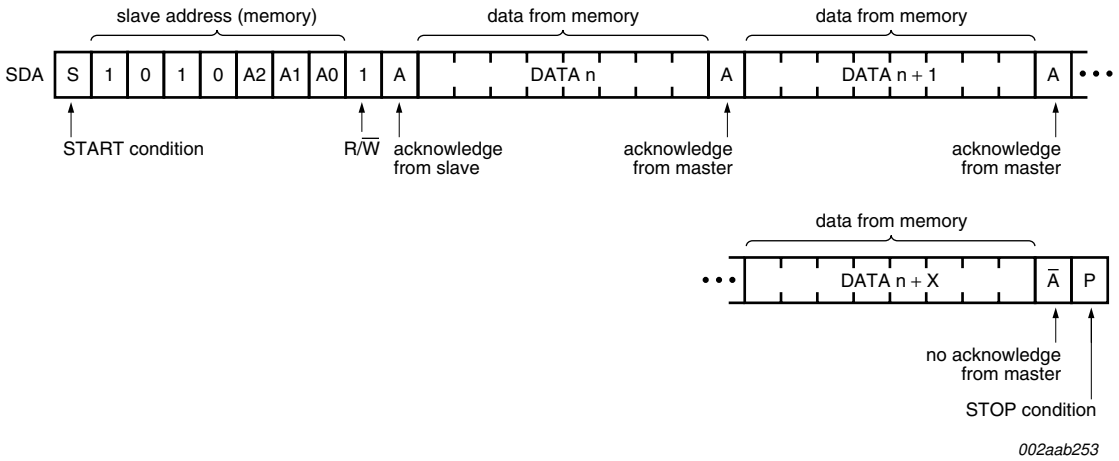


Fig 21. Sequential read timing

7.11 Hot plugging

The SE97 can be used in hot plugging applications. Internal circuitry prevents damaging current backflow through the device when it is powered down, but with the I²C-bus, $\overline{\text{EVENT}}$ or address pins still connected. The open-drain SDA and $\overline{\text{EVENT}}$ pins (SCL and address pins are input only) effectively places the outputs in a high-impedance state during power-up and power-down, which prevents driver conflict and bus contention. The 50 ns noise filter will filter out any insertion glitches from the state machine, which is very robust and not prone to false operation.

The device needs a proper power-up sequence to reset itself, not only for the device I²C-bus and I/O initial states, but also to load specific pre-defined data or calibration data into its operational registers. The power-up sequence should occur correctly with a fast ramp rate and the I²C-bus active. The SE97 might not respond immediately after power-up, but it should not damage the part if the power-up sequence is abnormal. If the SCL line is held LOW, the part will not exit the power-on reset mode since the part is held in reset until SCL is released.

8. Register descriptions

8.1 Register overview

This section describes all the registers used in the SE97. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading ‘0’s. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

Table 8. Register summary

Address (hex)	Default state (hex)	Register name
n/a	n/a	Pointer register
00h	0017h	Capability register (B grade = 0017h)
01h	0000h	Configuration register
02h	0000h	Upper Boundary Alarm Trip register
03h	0000h	Lower Boundary Alarm Trip register
04h	0000h	Critical Alarm Trip register
05h	n/a	Temperature register
06h	1131h	Manufacturer ID register
07h	A200h	Device ID/Revision register for SE97PW, SE97TK
	A201h	Device ID/Revision register for SE97TP, SE97TL
08h to 21h	0000h	reserved registers
22h	0000h	SMBus register
23h to FFh	0000h	reserved registers

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

8.2 Capability register (00h, 16-bit read-only)

Table 9. Capability register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RFU		VHV	TRES		WRNG	HACC	BCAP
Default	0	0	0[1]	1	0	1	1	1
Access	R	R	R	R	R	R	R	R

[1] The SE97 A0 pin can support up to 10 V, but the final die was already taped out before the JC42.4 ballot 1435.00 register change could be implemented. Bit 5 is changed from '0' to '1' on the future 1.7 V to 3.6 V SE97B.

Table 10. Capability register (address 00h) bit description

Bit	Symbol	Description
15:6	RFU	Reserved for future use; must be zero.
5	VHV	High voltage standoff for pin A0. 0 — default 1 — This part can support a voltage up to 10 V on the A0 pin to support JC42.4 ballot 1435.00.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB (11-bit)
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy (set during manufacture). 1 — B grade accuracy
0	BCAP	Basic capability. 1 — has Alarm and Critical Trips interrupt capability

8.3 Configuration register (01h, 16-bit read/write)

Table 11. Configuration register (address 01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HEN		SHMD
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 12. Configuration register (address 01h) bit description

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be ‘0’.
10:9	HEN	Hysteresis Enable. 00 — disable hysteresis (default) 01 — enable hysteresis at 1.5 °C 10 — enable hysteresis at 3 °C 11 — enable hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to ‘1’ (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 8 and Table 13). Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to ‘0’ (temperature is equal to or above the Alarm Window Lower Boundary Trip register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary register. As the temperature decreases, bit 13 will be set to ‘1’ when the value in the Temperature register is equal to or less than the value in the Alarm Temperature Lower Boundary register minus 3 °C. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the Critical Trip or Alarm Window lock bits is set, these bits cannot be altered until unlocked.