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# SE98A

DDR memory module temp sensor, 1.7 V to 3.6 V

Rev. 04 — 25 November 2009

Product data sheet

## 1. General description

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The NXP Semiconductors SE98A measures temperature from  $-40\text{ }^{\circ}\text{C}$  and  $+125\text{ }^{\circ}\text{C}$  with JEDEC Grade B  $\pm 1\text{ }^{\circ}\text{C}$  accuracy between  $+75\text{ }^{\circ}\text{C}$  and  $+95\text{ }^{\circ}\text{C}$  communicating via the I<sup>2</sup>C-bus/SMBus. It is typically mounted on a Dual In-Line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Thermal Sensor Component* specification.

The SE98A thermal sensor operates over the  $V_{DD}$  range of 1.7 V to 3.6 V. The SE98A does not include the 2 k SPD and is designed for custom DIMM where larger SPD is required.

The Temp Sensor (TS) consists of an Analog-to-Digital Converter (ADC) that monitors and updates its own temperature readings 8 times per second, converts the reading to a digital data, and latches them into the data temperature registers. User-programmable registers, such as Shutdown or Low-power modes and the specification of temperature event and critical output boundaries, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE98A outputs an EVENT signal using an open-drain output that can be pulled up between 0.9 V and 3.6 V. The user has the option of setting the EVENT output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The EVENT output can even be configured as a critical temperature output.

The SE98A supports the industry-standard 2-wire I<sup>2</sup>C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identify of the device. Three address pins allow up to eight devices to be controlled on a single bus.

The SE98A is an improved SE98 and is comparable to the thermal sensor in the SE97 but with voltage range of 1.7 V to 3.6 V.

## 2. Features

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- JEDEC (JC-42.4) TS3000B1 DIMM  $\pm 0.5\text{ }^{\circ}\text{C}$  (typ.) between  $75\text{ }^{\circ}\text{C}$  and  $95\text{ }^{\circ}\text{C}$  temperature sensor
- Optimized for voltage range: 1.7 V to 3.6 V
- Shutdown current:  $0.1\text{ }\mu\text{A}$  (typ.) and  $5.0\text{ }\mu\text{A}$  (max.)
- 2-wire interface: I<sup>2</sup>C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus ALERT and TIMEOUT (programmable)
- 11-bit ADC Temperature-to-Digital converter with  $0.125\text{ }^{\circ}\text{C}$  resolution

- Operating current: 250  $\mu$ A (typ.) and 400  $\mu$ A (max.)
- Programmable hysteresis threshold: 0  $^{\circ}$ C, 1.5  $^{\circ}$ C, 3  $^{\circ}$ C, 6  $^{\circ}$ C
- Over/under/critical temperature  $\overline{\text{EVENT}}$  output
- B grade accuracy:
  - ◆  $\pm 0.5$   $^{\circ}$ C/ $\pm 1$   $^{\circ}$ C (typ./max.)  $\rightarrow$  +75  $^{\circ}$ C to +95  $^{\circ}$ C
  - ◆  $\pm 1$   $^{\circ}$ C/ $\pm 2$   $^{\circ}$ C (typ./max.)  $\rightarrow$  +40  $^{\circ}$ C to +125  $^{\circ}$ C
  - ◆  $\pm 2$   $^{\circ}$ C/ $\pm 3$   $^{\circ}$ C (typ./max.)  $\rightarrow$  -40  $^{\circ}$ C to +125  $^{\circ}$ C
- ESD protection exceeds 2000 V HBM per JESD22-A114, 250 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Available packages: TSSOP8, HWSON8 (PSON8 VCED-3) and HXSON8

### 3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking
- Hard disk drives and other PC peripherals

### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE98APW	S98A	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE98ATP <sup>[1]</sup>	98A	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 $\times$ 3 $\times$ 0.8 mm	SOT1069-2
SE98ATL	8AL	HXSON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 $\times$ 3 $\times$ 0.5 mm	SOT1052-1

[1] Industry standard 2 mm  $\times$  3 mm  $\times$  0.8 mm package to JEDEC VCED-3 PSON8 in 8 mm  $\times$  4 mm pitch tape 4 k quantity reels.

## 5. Block diagram

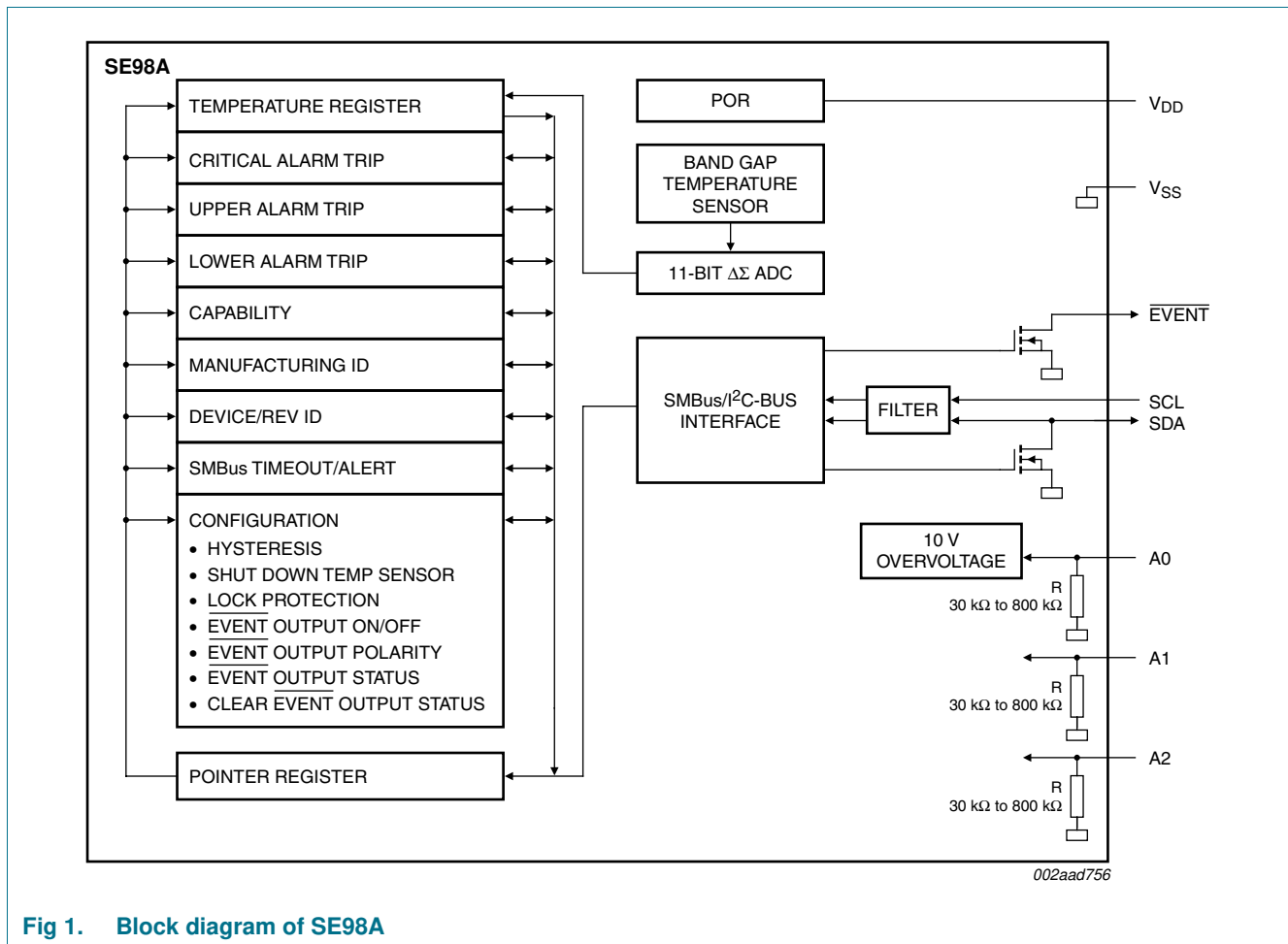
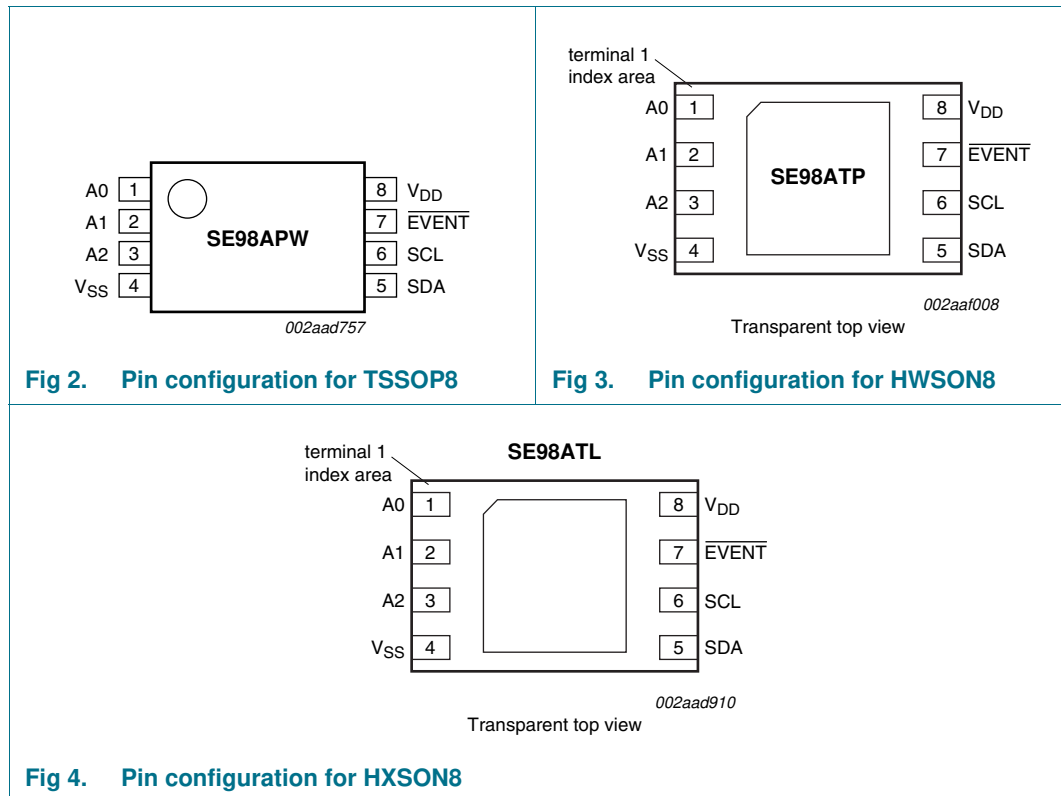


Fig 1. Block diagram of SE98A



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0 <sup>[1]</sup>	1	I	I <sup>2</sup> C-bus/SMBus slave address bit 0 with internal pull-down
A1	2	I	I <sup>2</sup> C-bus/SMBus slave address bit 1 with internal pull-down
A2	3	I	I <sup>2</sup> C-bus/SMBus slave address bit 2 with internal pull-down
V <sub>SS</sub>	4	ground	device ground
SDA	5	I/O	SMBus/I <sup>2</sup> C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I <sup>2</sup> C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
EVENT	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V <sub>DD</sub>	8	power	device power supply (1.7 V to 3.6 V)

[1] This input is overvoltage tolerant to support software write protection when applied to SPD.

## 7. Functional description

### 7.1 Serial bus interface

The SE98A uses the 2-wire serial bus (I<sup>2</sup>C-bus/SMBus) to communicate with a host controller. The serial bus consists of a clock (SCL) and data (SDA) signals. The device can operate on either the I<sup>2</sup>C-bus Standard/Fast mode or SMBus. The I<sup>2</sup>C-bus Standard-mode is defined to have bus speeds from 0 Hz to 100 kHz, I<sup>2</sup>C-bus Fast-mode from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE98A uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I<sup>2</sup>C-bus data is 1 byte. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

### 7.2 Slave address

The SE98A uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to coexist on the same bus. The input of each pin is sampled at the start of each I<sup>2</sup>C-bus/SMBus access. The A0, A1 and A2 pins are pulled LOW internally. The A0 pin is also overvoltage tolerant, supporting 10 V software write protection when applied to the SPD that shares common address lines.

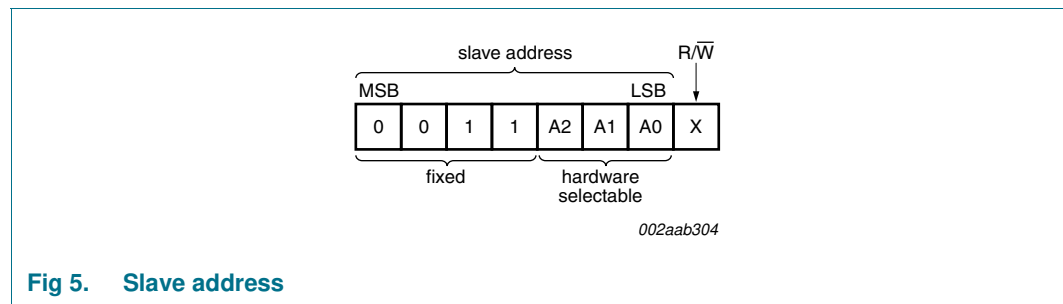


Fig 5. Slave address

### 7.3 $\overline{\text{EVENT}}$ output condition

The  $\overline{\text{EVENT}}$  output indicates conditions such as the temperature crossing a predefined boundary. The  $\overline{\text{EVENT}}$  modes are very configurable and selected using the configuration register (CONFIG). The interrupt mode or comparator mode is selected using CONFIG[0], using either TCRT/UPPER/LOWER or TCRT only temperature bands (CONFIG[2]) as modified by hysteresis (CONFIG[10:9]). The UPPER/LOWER (CONFIG[6]) and TCRT (CONFIG[7]) bands can be locked. [Figure 6](#) shows an example of the measured temperature versus time, with the corresponding behavior of the  $\overline{\text{EVENT}}$  output in each of these modes.

Upon device power-up, the default condition for the  $\overline{\text{EVENT}}$  output is high-impedance to prevent spurious or unwanted alarms, but can be later enabled (CONFIG[3]).  $\overline{\text{EVENT}}$  output polarity can be set to active HIGH or active LOW (CONFIG[1]).  $\overline{\text{EVENT}}$  status can be read (CONFIG[4]) and cleared (CONFIG[5]).

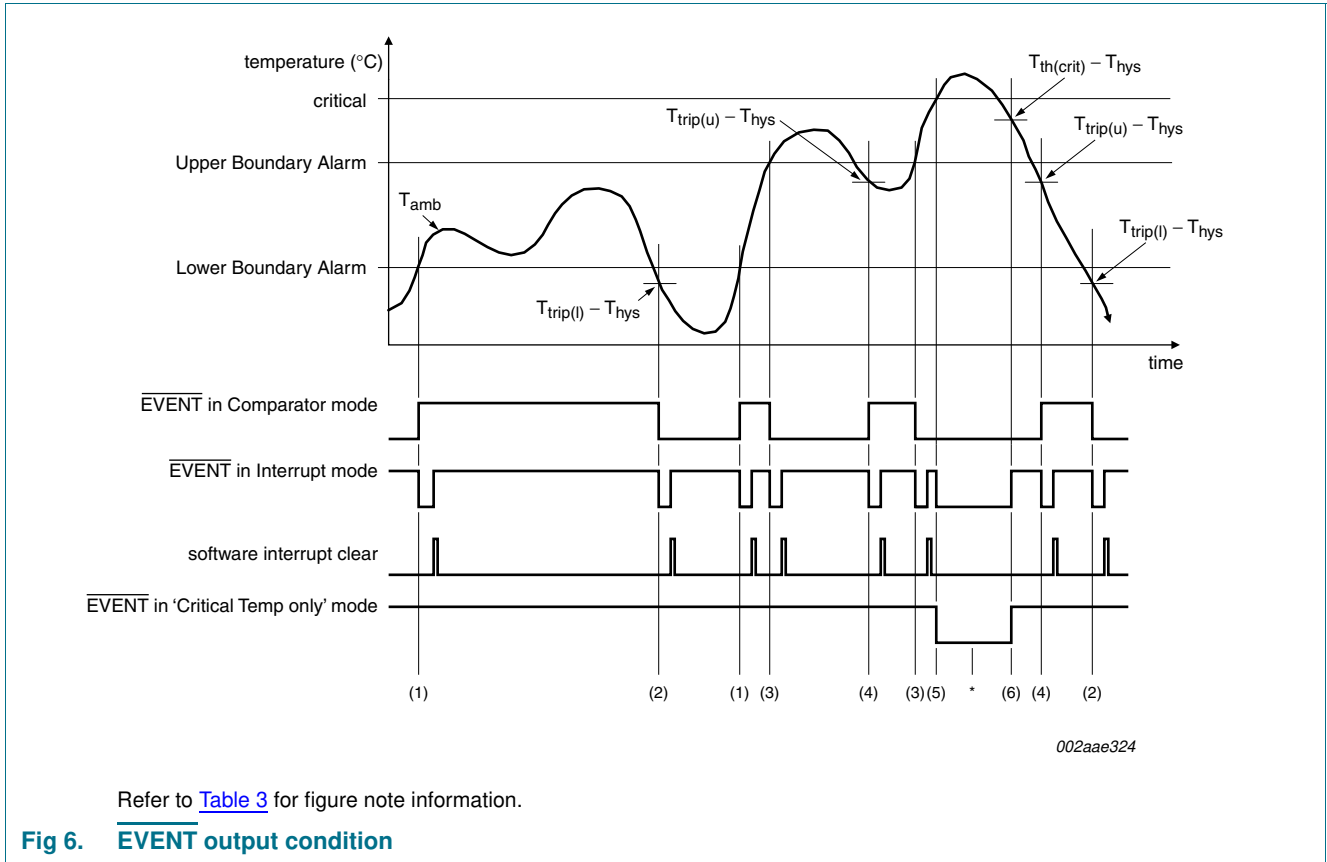
- **Advisory notification:**

- NXP device: After power-up, bit 3 (1) and bit 2 or bit 0 (leave as 0 or 1) can be set at the same time (e.g., in same byte) but once bit 3 is set (1) then changing bit 2 or bit 0 has no effect on the device operation.
- Competitor device: Does not require that bit 3 be cleared (e.g., set back to (0)) before changing bit 2 or bit 0.
- Work-around: In order to change bit 2 or bit 0 once bit 3 (1) is set, bit 3 (0) must be cleared in one byte and then change bit 2 or bit 0 and reset bit 3 (1) in the next byte.
- SE98B will allow bit 2 or bit 0 to be changed even if bit 3 is set.

If the device enters Shutdown mode (CONFIG[8]) with asserted  $\overline{\text{EVENT}}$  output, the output remains asserted during shutdown.

#### 7.3.1 $\overline{\text{EVENT}}$ pin output voltage levels and resistor sizing

The  $\overline{\text{EVENT}}$  open-drain output is typically pulled up to a voltage level from 0.9 V to 3.6 V with an external pull-up resistor, but there is no real lower limit on the pull-up voltage for the  $\overline{\text{EVENT}}$  pin since it is simply an open-drain output. It could be pulled up to 0.1 V and would not affect the output. From the system perspective, there will be a practical limit. That limit will be the voltage necessary for the device monitoring the interrupt pin to detect a HIGH on its input. A possible practical limit for a CMOS input would be 0.4 V. Another thing to consider is the value of the pull-up resistor. When a low supply voltage is applied to the drain (through the pull-up resistor) it is important to use a higher value pull-up resistor, to allow a larger maximum signal swing on the  $\overline{\text{EVENT}}$  pin.



**Table 3. EVENT output condition**

Figure note	EVENT output boundary conditions	EVENT output			Temperature Register Status bits		
		Comparator mode	Interrupt mode	Critical Temp only mode	Bit 15 Above Critical Trip	Bit 14 Above Alarm Window	Bit 13 Below Alarm Window
(1)	$T_{amb} \geq T_{trip(l)}$	H	L	H	0	0	0
(2)	$T_{amb} < T_{trip(l)} - T_{hys}$	L	L	H	0	0	1
(3)	$T_{amb} > T_{trip(u)}$	L	L	H	0	1	0
(4)	$T_{amb} \leq T_{trip(u)} - T_{hys}$	H	L	H	0	0	0
(5)	$T_{amb} \geq T_{th(crit)}$	L	L	L	1	1	0
(6)	$T_{amb} < T_{th(crit)} - T_{hys}$	L	H	H	0	1	0

When  $T_{amb} \geq T_{th(crit)}$  and  $T_{amb} < T_{th(crit)} - T_{hys}$  the  $\overline{\text{EVENT}}$  output is in Comparator mode and bit 0 of CONFIG (EVENT output mode) is ignored.



## 7.3.2 EVENT thresholds

### 7.3.2.1 Alarm window

The device provides a comparison window with an UPPER trip point and a LOWER trip point, programmed through the Upper Boundary Alarm Trip register (02h), and Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point as modified by hysteresis as programmed in the Configuration register. When enabled, the EVENT output triggers whenever entering or exiting (crossing above or below) the alarm window.

- **Advisory notification:**

- NXP device: The EVENT output can be cleared through the Clear EVENT bit (CEVNT) or SMBus ALERT.
- Competitor device: The EVENT output can be cleared only through the Clear EVENT bit (CEVNT).
- Work-around: Only clear EVENT output using the Clear EVENT bit (CEVNT).
- There will be no change to the NXP device.

The Upper Boundary Alarm Trip should always be set above the Lower Boundary Alarm Trip.

- **Advisory notification:**

- NXP device: Requires one conversion cycle (125 ms) after setting the alarm window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating EVENT output.
- Competitor devices: Compares the alarm limit with temperature register at any time, so they get the EVENT output immediately when new UPPER or LOWER Alarm Windows and the EVENT output are set at the same time.
- Work-around: Wait at least 125 ms before enabling EVENT output (EOCTL = 1).
- SE98B will compare alarm window and temperature register immediately after setting.

### 7.3.2.2 Critical trip

The  $T_{th(crit)}$  temperature setting is programmed in the Critical Alarm Trip register (04h) as modified by hysteresis as programmed in the Configuration register. When the temperature reaches the critical temperature value in this register (and  $\overline{EVENT}$  is enabled), the  $\overline{EVENT}$  output asserts and cannot be de-asserted until the temperature drops below the critical temperature threshold. The  $\overline{EVENT}$  cannot be cleared through the Clear  $\overline{EVENT}$  bit (CEVNT) or SMBus ALERT.

The Critical Alarm Trip should always be set above the Upper Boundary Alarm Trip.

- **Advisory notification:**

- NXP device: Requires one conversion cycle (125 ms) after setting the Alarm Window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating  $\overline{EVENT}$  output.
- Competitor devices: Compares the Alarm Window with temperature register at any time, so they get the  $\overline{EVENT}$  output immediately when new  $T_{th(crit)}$  and  $\overline{EVENT}$  output are set at the same time.
- Work-around: Wait at least 125 ms before enabling  $\overline{EVENT}$  output (EOCTL = 1). Intel will change Nehalem BIOS so that  $T_{th(crit)}$  is set for more than 125 ms before  $\overline{EVENT}$  output is enabled and Event value is checked.
  1. Set  $T_{th(crit)}$ .
  2. Doing something else (make sure that exceeds 125 ms).
  3. Enable the  $\overline{EVENT}$  output (EOCTL = 1).
  4. Wait 20  $\mu$ s.
  5. Read Event value.
- SE98B will compare Alarm Window and temperature register immediately after setting.

### 7.3.3 Event operation modes

#### 7.3.3.1 Comparator mode

In comparator mode, the  $\overline{EVENT}$  output behaves like a window-comparator output that asserts when the temperature is outside the window (e.g., above the value programmed in the Upper Boundary Alarm Trip register or below the value programmed in the Lower Boundary Alarm Trip register or above the Critical Alarm Trip register if  $T_{th(crit)}$  only is selected). Reads/writes on the registers do not affect the  $\overline{EVENT}$  output in comparator mode. The  $\overline{EVENT}$  signal remains asserted until the temperature goes inside the alarm window or the window thresholds are reprogrammed so that the current temperature is within the alarm window.

The comparator mode is useful for thermostat-type applications, such as turning on a cooling fan or triggering a system shutdown when the temperature exceeds a safe operating range.

#### 7.3.3.2 Interrupt mode

In interrupt mode,  $\overline{EVENT}$  asserts whenever the temperature crosses an alarm window threshold. After such an event occurs, writing a 1 to the Clear  $\overline{EVENT}$  bit in the configuration register de-asserts the  $\overline{EVENT}$  output until the next trigger condition occurs.

In interrupt mode,  $\overline{\text{EVENT}}$  asserts when the temperature crosses the alarm upper boundary. If the  $\overline{\text{EVENT}}$  output is cleared and the temperature continues to increase until it crosses the critical temperature threshold,  $\overline{\text{EVENT}}$  asserts again. Because the temperature is greater than the critical temperature threshold, a Clear  $\overline{\text{EVENT}}$  command does not clear the  $\overline{\text{EVENT}}$  output. Once the temperature drops below the critical temperature,  $\overline{\text{EVENT}}$  de-asserts immediately.

- **Advisory notification:**

- NXP device: If the  $\overline{\text{EVENT}}$  output is not cleared before the temperature goes above the critical temperature threshold  $\overline{\text{EVENT}}$  de-asserts immediately when temperature drops below the critical temperature.
- Competitor devices: If the  $\overline{\text{EVENT}}$  output is not cleared before or when the temperature is in the critical temperature threshold,  $\overline{\text{EVENT}}$  will remain asserted after the temperature drops below the critical temperature until a Clear  $\overline{\text{EVENT}}$  command.
- Work-around: Always clear the  $\overline{\text{EVENT}}$  output before temperature exceeds the critical temperature.
- SE98B will keep  $\overline{\text{EVENT}}$  asserted after the temperature drops below the critical temperature until a Clear  $\overline{\text{EVENT}}$  command de-asserts  $\overline{\text{EVENT}}$ .

## 7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE98A's conversion rate is at least 8 Hz or 125 ms.

### 7.4.1 What temperature is read when conversion is in progress

The SE98A has been designed to ensure a valid temperature is always available. When a read to the temperature register is initiated through the SMBus, the device checks to see if the temperature conversion process (Analog-to-Digital conversion) is complete and a new temperature is available:

- If the temperature conversion process is complete, then the new temperature value is sent out on the SMBus.
- If the temperature conversion process is **not** complete, then the previous temperature value is sent out on the SMBus.

It is possible that while the SMBus Master is reading the temperature register, a new temperature conversion completes. However, this will not affect the data (MSB or LSB) that is being shifted out. On the next read of the temperature register the new temperature value will be shifted out.

## 7.5 Power-up default condition

After power-on, the SE98A is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$  register is cleared— $\overline{\text{EVENT}}$  output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$  hysteresis is defaulted to 0 °C
- Command pointer is defaulted to '00h'
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to '0037h' for the B-grade and VHV capability
- Operational mode: comparator
- SMBus register is defaulted to '00h'

## 7.6 Device initialization

SE98A temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain  $\overline{\text{EVENT}}$  output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

[Table 4](#) shows the default values and the example value to be programmed to these registers.

**Table 4. Registers to be initialized**

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register <ul style="list-style-type: none"> <li>• hysteresis = 1.5 °C</li> <li>• <math>\overline{\text{EVENT}}</math> output = Interrupt mode</li> <li>• <math>\overline{\text{EVENT}}</math> output is enabled</li> </ul>
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = -20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

### 7.7 SMBus Time-out

The SE98A supports the SMBus time-out feature. If the host holds SCL LOW between 25 ms and 35 ms, the SE98A would reset its internal state machine to the bus idle state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a logic 1 to bit 7 of register 22h.

**Remark:** When SMBus time-out is enabled, the I<sup>2</sup>C-bus minimum bus speed is limited by the SMBus time-out timer, and goes down to only 10 kHz.

The SE98A has no SCL driver, so it cannot hold the SCL line LOW.

**Remark:** SMBus time-out works over the entire supply range of 1.7 V to 3.6 V unless shutdown bit (SHMD) is set and turns off the oscillator.

### 7.8 SMBus ALERT

The SE98A supports SMBus ALERT when it is programmed for the Interrupt mode and when the EVENT polarity bit is set to logic 0. The EVENT pin can be ANDed with other EVENT or ALERT signals from other slave devices to signal their intention to communicate with the host controller. When the host detects EVENT or ALERT signal LOW, it issues an Alert Response Address (ARA) to which a slave device would respond with its address. When there are multiple slave devices generating an ALERT the SE98A performs bus arbitration. If it wins the bus, it responds to the ARA and then clears the EVENT pin.

**Remark:** Either in comparator mode or when the SE98A crosses the critical temperature, the host must also read the EVENT status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the EVENT pin will not get de-asserted.

**Remark:** In the SE98A, the ARA is set to default ON. However, in the SE98B the ARA will be set to default OFF since ARA is not anticipated to be used in DDR3 DIMM applications.

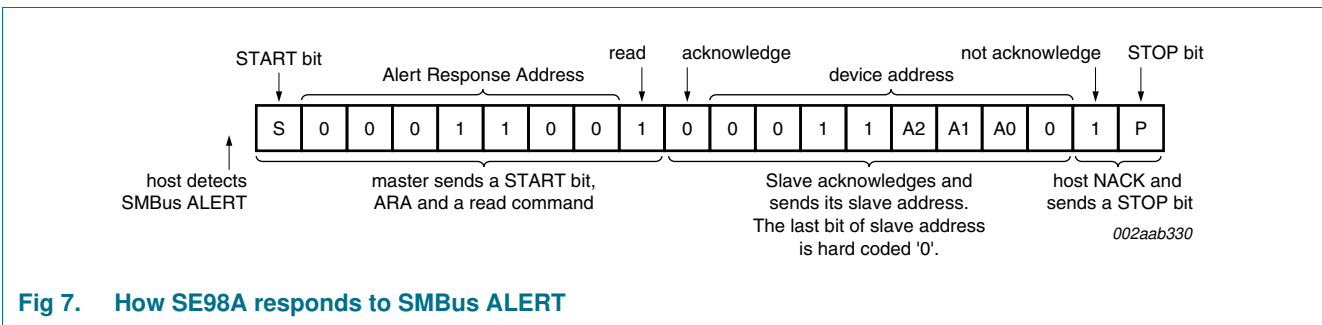


Fig 7. How SE98A responds to SMBus ALERT

### 7.9 SMBus/I<sup>2</sup>C-bus interface

The data registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to '00', the location for the Capability register. The Pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

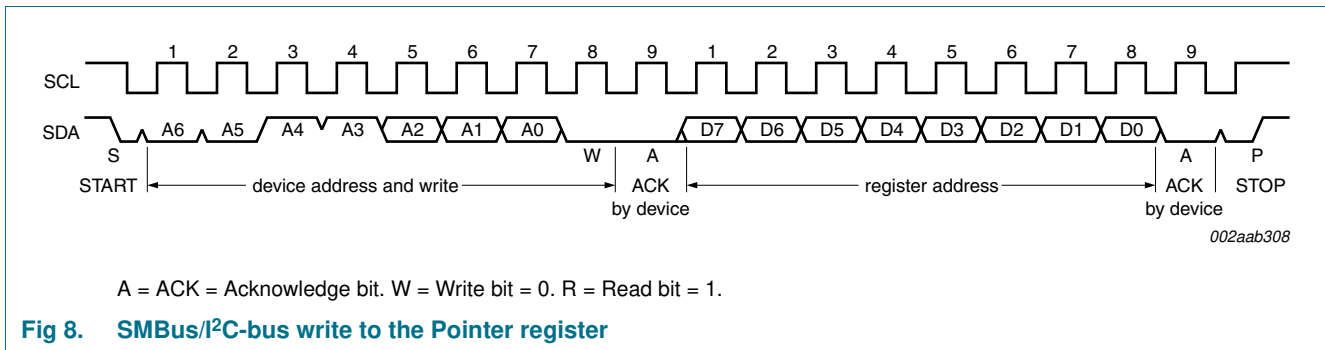
- Read only
- Write only
- Write/Read same address.

A 'write' to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

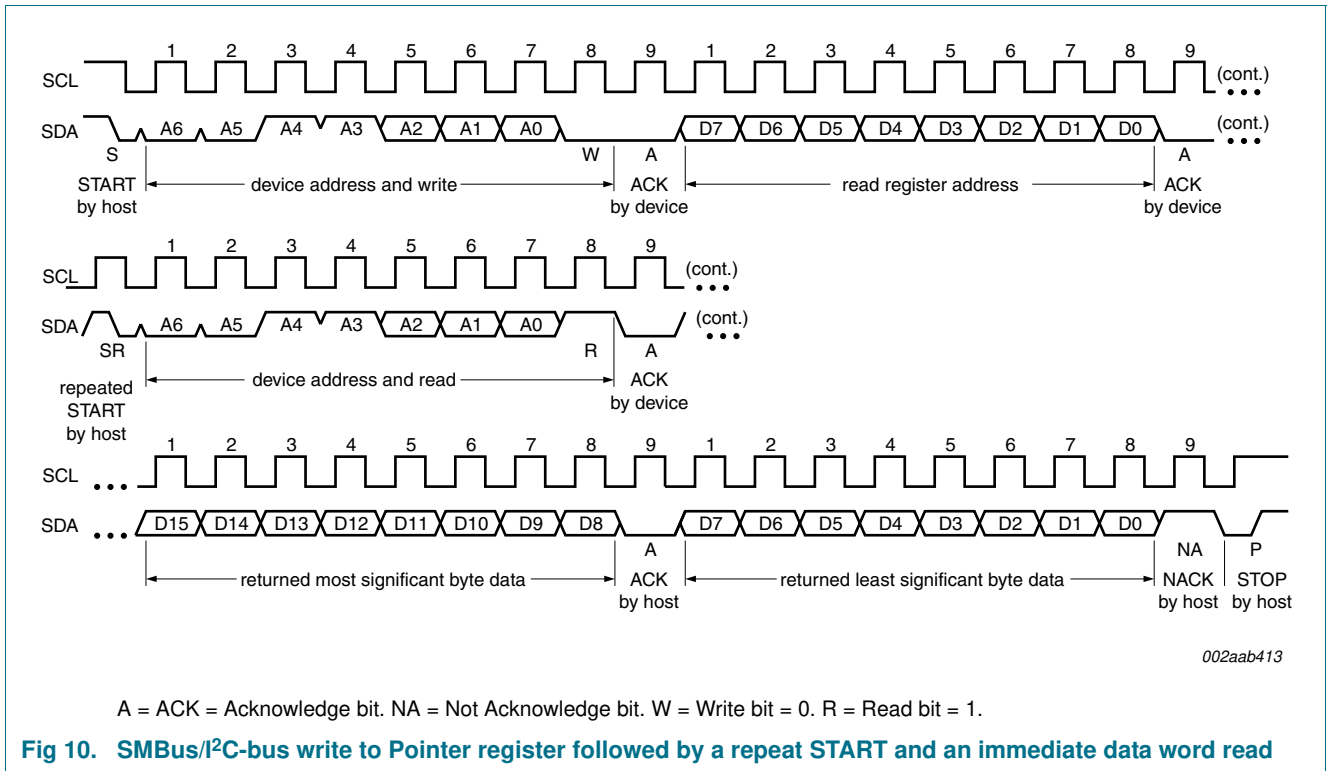
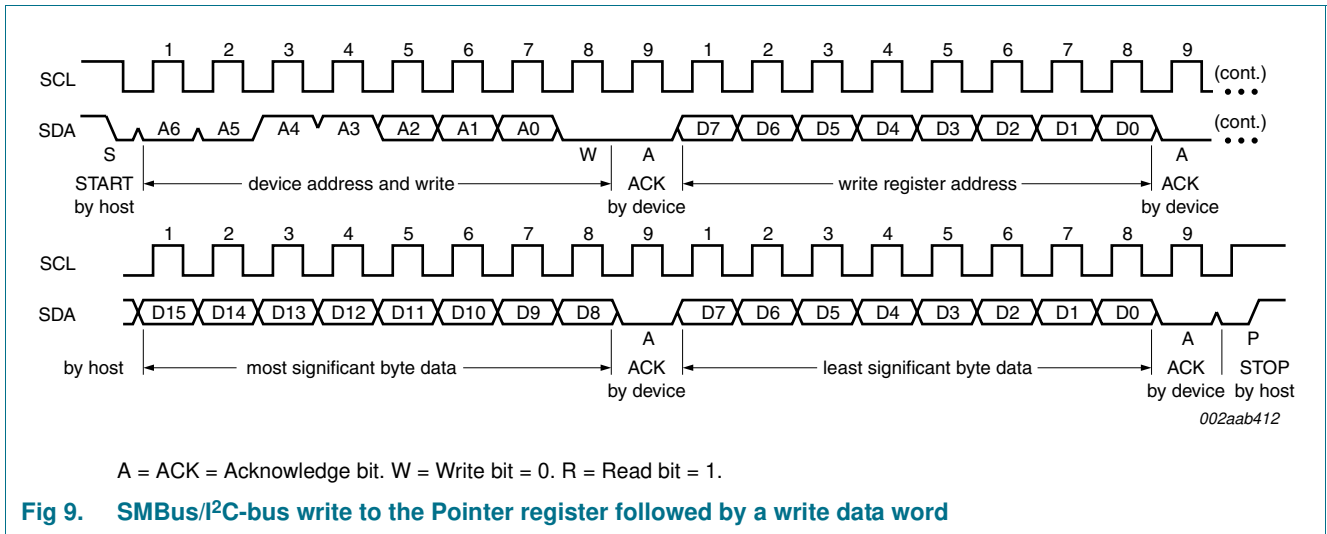
Reading this device can take place either of two ways:

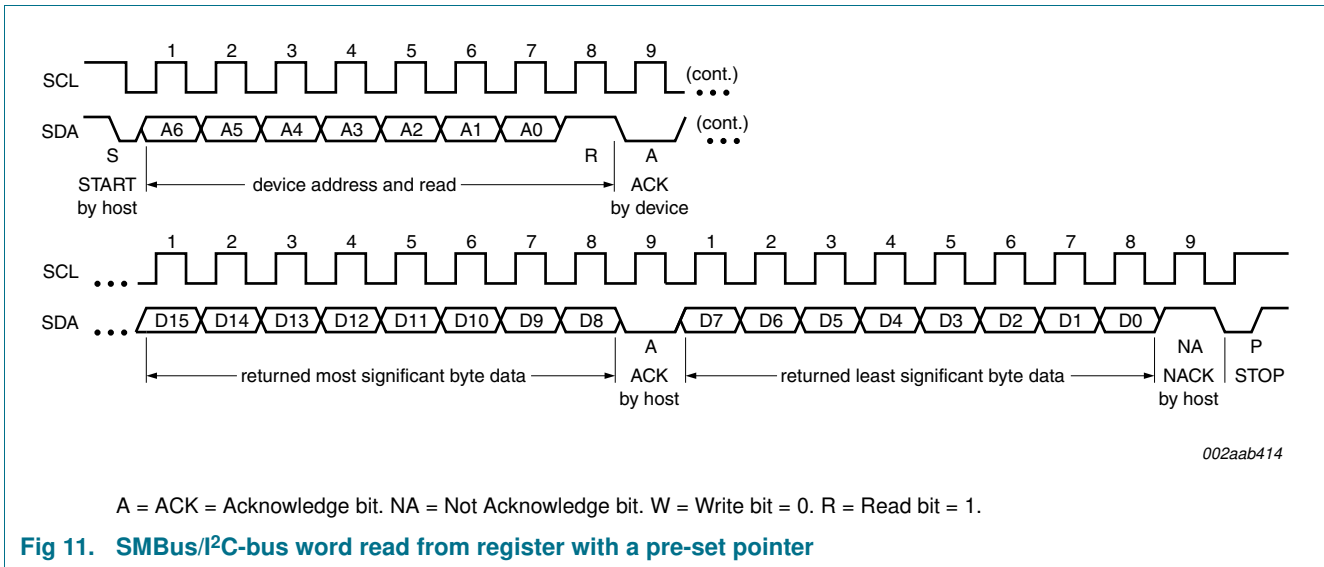
- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Temperature register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to the timing diagrams in [Figure 8](#), [Figure 9](#), [Figure 10](#) and [Figure 11](#) on how to program the device.









### 7.10 Hot plugging

The SE98A can be used in hot plugging applications. Internal circuitry prevents damaging current backflow through the device when it is powered down, but with the I<sup>2</sup>C-bus, EVENT or address pins still connected. The open-drain SDA and EVENT pins (SCL and address pins are input only) effectively places the outputs in a high-impedance state during power-up and power-down, which prevents driver conflict and bus contention. The 50 ns noise filter will filter out any insertion glitches from the state machine, which is very robust and not prone to false operation.

The device needs a proper power-up sequence to reset itself, not only for the device I<sup>2</sup>C-bus and I/O initial states, but also to load specific pre-defined data or calibration data into its operational registers. The power-up sequence should occur correctly with a fast ramp rate and the I<sup>2</sup>C-bus active. The SE98A might not respond immediately after power-up, but it should not damage the part if the power-up sequence is abnormal. If the SCL line is held LOW, the part will not exit the power-on reset mode since the part is held in reset until SCL is released.

## 8. Register descriptions

### 8.1 Register overview

This section describes all the registers used in the SE98A. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the Pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading zeroes. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

**Table 5. Register summary**

Address	POR state	Register name
n/a	n/a	Pointer register
00h	0037h	Capability register (B grade = 0037h)
01h	0000h	Configuration register
02h	0000h	Upper Boundary Alarm Trip register
03h	0000h	Lower Boundary Alarm Trip register
04h	0000h	Critical Alarm Trip register
05h	n/a	Temperature register
06h	1131h	Manufacturer ID register
07h	A102h	Device ID/Revision register
08h to 21h	0000h	reserved registers
22h	0000h	SMBus register
23h to FFh	0000h	reserved registers

A write to reserved registers may cause unexpected results which may result in requiring a reset by removing and re-applying its power.

## 8.2 Capability register (00h, 16-bit read-only)

**Table 6.** Capability register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU[9:2]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	RFU[1:0]		VHV	TRES[1:0]		WRNG	HACC	BCAP
Reset	0	0	1	1	0	1	1	1
Access	R	R	R	R	R	R	R	R

**Table 7.** Capability register (address 00h) bit description

Bit	Symbol	Description
15:6	RFU	Reserved for future use. Must be zero.
5	VHV	High voltage standoff for pin A0. 1 — This part can support a voltage up to 10 V on the A0 pin to support JC42.4 ballot 1435.00.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB (11-bit)
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy (set during manufacture). 1 — B grade accuracy
0	BCAP	Basic capability. 1 — has Alarm and Critical Trips interrupt capability.

### 8.3 Configuration register (01h, 16-bit read/write)

**Table 8. Configuration register (address 01h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	RFU				HEN[1:0]		SHMD	
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9. Configuration register (address 01h) bit description**

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be '0'.
10:9	HEN	<p>Hysteresis Enable</p> <ul style="list-style-type: none"> <li>00 — Disable hysteresis (default)</li> <li>01 — Enable hysteresis at 1.5 °C</li> <li>10 — Enable hysteresis at 3 °C</li> <li>11 — Enable hysteresis at 6 °C</li> </ul> <p>When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the 'Above Alarm Window' bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to 1 (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to <a href="#">Figure 6</a> and <a href="#">Table 10</a>).</p> <p>Similarly, the 'Below Alarm Window' bit (bit 13 of the Temperature register) will be set to 0 (temperature is equal to or above the Alarm Window Lower Boundary Trip register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary register. As the temperature decreases, bit 13 will be set to 1 when the value in the Temperature register is equal to or less than the value in the Alarm Temperature Lower Boundary register minus 3 °C. Note that hysteresis is also applied to EVENT pin functionality.</p> <p>When either of the Critical Trip or Alarm Window lock bits is set, these bits cannot be altered until unlocked.</p>
8	SHMD	<p>Shutdown Mode.</p> <ul style="list-style-type: none"> <li>0 — Enabled Temperature Sensor (default)</li> <li>1 — Disabled Temperature Sensor</li> </ul> <p>When shut down, the thermal sensor diode and Analog-to-Digital Converter (ADC) are disabled to save power, no events will be generated. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time.</p>

Table 9. Configuration register (address 01h) bit description ...continued

Bit	Symbol	Description
7	CTLB	<p>Critical Trip Lock bit.</p> <p>0 — Critical Alarm Trip register is not locked and can be altered (default). 1 — Critical Alarm Trip register settings cannot be altered.</p> <p>This bit is initially cleared. When set, this bit will return a 1, and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes.</p>
6	AWLB	<p>Alarm Window Lock bit.</p> <p>0 — Upper and Lower Alarm Trip registers are not locked and can be altered (default). 1 — Upper and Lower Alarm Trip registers setting cannot be altered.</p> <p>This bit is initially cleared. When set, this bit will return a 1 and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes.</p>
5	CEVNT	<p>Clear <math>\overline{\text{EVENT}}</math> (write only).</p> <p>0 — No effect (default). 1 — Clears active <math>\overline{\text{EVENT}}</math> in Interrupt mode. Writing to this register has no effect in Comparator mode.</p> <p>When read, this register always returns zero.</p>
4	ESTAT	<p><math>\overline{\text{EVENT}}</math> Status (read only).</p> <p>0 — <math>\overline{\text{EVENT}}</math> output condition is not being asserted by this device (default). 1 — <math>\overline{\text{EVENT}}</math> output pin is being asserted by this device due to Alarm Window or Critical Trip condition.</p> <p>The actual event causing the <math>\overline{\text{EVENT}}</math> can be determined from the Read Temperature register. Interrupt Events can be cleared by writing to the 'Clear <math>\overline{\text{EVENT}}</math>' bit (CEVNT). Writing to this bit will have no effect.</p>
3	EOCTL	<p><math>\overline{\text{EVENT}}</math> Output Control.</p> <p>0 — <math>\overline{\text{EVENT}}</math> output disabled (default). 1 — <math>\overline{\text{EVENT}}</math> output enabled.</p> <p>When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.</p>
2	CVO	<p>Critical Event Only.</p> <p>0 — <math>\overline{\text{EVENT}}</math> output on Alarm or Critical temperature event (default) 1 — <math>\overline{\text{EVENT}}</math> only if temperature is above the value in the critical temperature register</p> <p>When the Critical Trip or Alarm Window lock bit is set, this bit cannot be altered until unlocked.</p> <ul style="list-style-type: none"> <li>• <b>Advisory note:</b> <ul style="list-style-type: none"> <li>– JEDEC specification requires only the Alarm Window lock bit to be set.</li> <li>– Work-around: Clear both Critical Trip and Alarm Window lock bits.</li> <li>– Future 1.7 V to 3.6 V SE98B will require only the Alarm Window lock bit to be set.</li> </ul> </li> </ul>

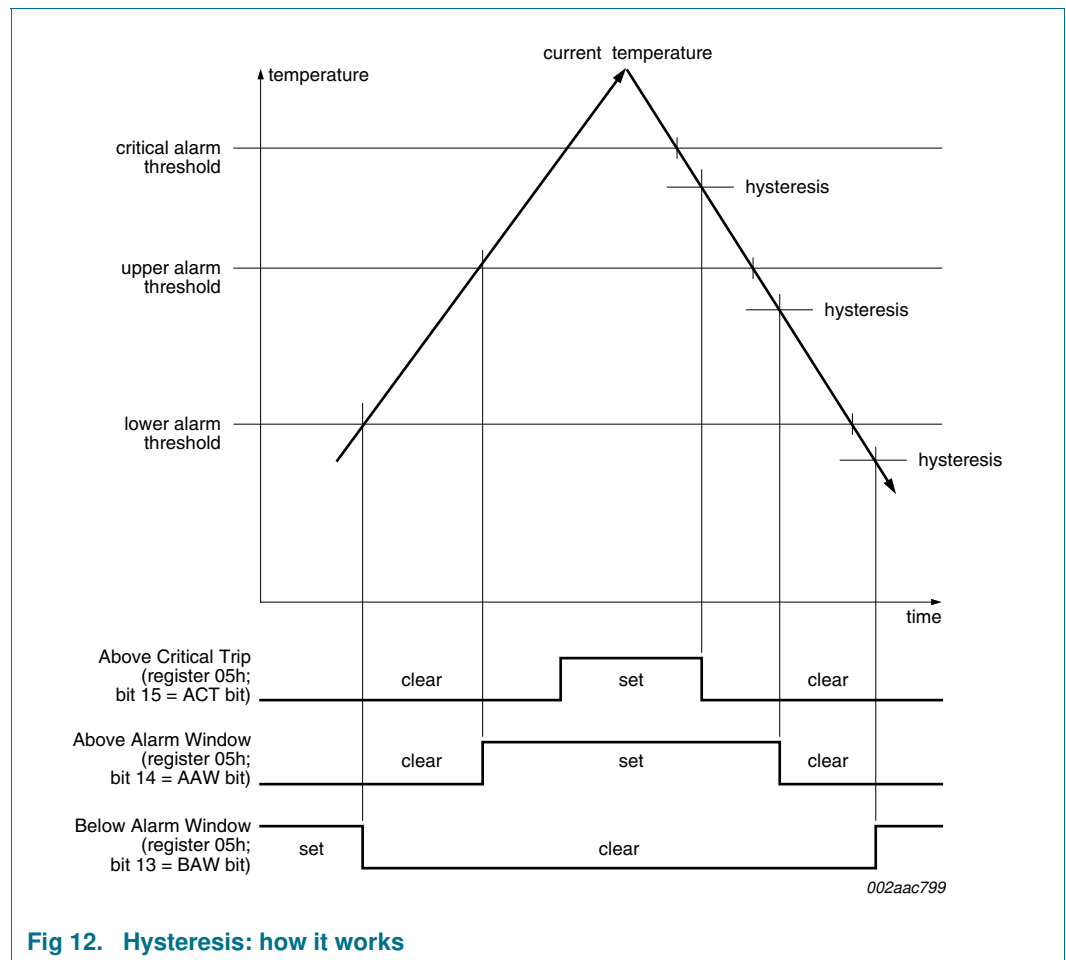


**Table 9. Configuration register (address 01h) bit description ...continued**

Bit	Symbol	Description
1	EP	<p>EVENT Polarity.</p> <p>0 — active LOW (default).</p> <p>1 — active HIGH.</p> <p>When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.</p>
0	EMD	<p>EVENT Mode.</p> <p>0 — comparator output mode (default)</p> <p>1 — interrupt mode</p> <p>When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.</p>

**Table 10. Hysteresis enable**

Action	Below Alarm Window bit (bit 13)		Above Alarm Window bit (bit 14)		Above Critical Trip bit (bit 15)	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
sets	falling	$T_{trip(l)} - T_{hys}$	rising	$T_{trip(u)}$	rising	$T_{th(crit)}$
clears	rising	$T_{trip(l)}$	falling	$T_{trip(u)} - T_{hys}$	falling	$T_{th(crit)} - T_{hys}$



**Fig 12. Hysteresis: how it works**

## 8.4 Temperature format

The 16-bit value used in the following Trip Point Set and Temperature Read-Back registers is 2's complement with the Least Significant Bit (LSB) equal to 0.0625 °C. For example:

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent -25.75 °C.

The resolution is 0.125 °C. The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the  $\overline{\text{EVENT}}$  output.

[Table 11](#) lists the examples of the content of the temperature data register for positive and negative temperature for two scenarios of status bits: status bits = 000b and status bits = 111b.

**Table 11. Degree Celsius and Temperature Data register**

Temperature	Content of Temperature Data register			
	Status bits = 000b		Status bits = 111b	
	Binary	Hex	Binary	Hex
+125 °C	000 0 01111101 000 0	07D0h	111 0 01111101 000 0	E7D0h
+25 °C	000 0 00011001 000 0	0190h	111 0 00011001 000 0	E190h
+1 °C	000 0 00000001 000 0	0010h	111 0 00000001 000 0	E010h
+0.25 °C	000 0 00000000 010 0	0004h	111 0 00000000 010 0	E004h
+0.125 °C	000 0 00000000 001 0	0002h	111 0 00000000 001 0	E002h
0 °C	000 0 00000000 000 0	0000h	111 0 00000000 000 0	E000h
-0.125 °C	000 1 11111111 111 0	1FFEh	111 1 11111111 111 0	FFFEh
-0.25 °C	000 1 11111111 110 0	1FFCh	111 1 11111111 110 0	FFCh
-1 °C	000 1 11111111 000 0	1FF0h	111 1 11111111 000 0	FFF0h
-20 °C	000 1 11110100 000 0	1F40h	111 1 11110100 000 0	FF40h
-25 °C	000 1 11100111 000 0	1E70h	111 1 11100111 000 0	FE70h
-55 °C	000 1 11001001 000 0	1C90h	111 1 11001001 000 0	FC90h

## 8.5 Temperature Trip Point registers

### 8.5.1 Upper Boundary Alarm Trip register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

**Table 12. Upper Boundary Alarm Trip register bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol		RFU		SIGN		UBT[9:6]		
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol		UBT[5:0]					RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

**Table 13. Upper Boundary Alarm Trip register bit description**

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	UBT	Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

### 8.5.2 Lower Boundary Alarm Trip register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

**Table 14. Lower Boundary Alarm Trip register bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	LBT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	LBT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

**Table 15. Lower Boundary Alarm Trip register bit description**

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	LBT	Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

### 8.5.3 Critical Alarm Trip register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

**Table 16. Lower Boundary Alarm Trip register bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	CT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	CT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

**Table 17. Critical Alarm Trip register bit description**

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	CT	Critical Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

## 8.6 Temperature register (16-bit read-only)

Table 18. Temperature register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ACT	AAW	BAW	SIGN	TEMP[10:7]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	TEMP[6:0]							RFU
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 19. Temperature register bit description

Bit	Symbol	Description
15	ACT	Above Critical Trip. Increasing $T_{amb}$ : 0 — $T_{amb} < T_{th(crit)}$ 1 — $T_{amb} \geq T_{th(crit)}$ Decreasing $T_{amb}$ : 0 — $T_{amb} < T_{th(crit)} - T_{hys}$ 1 — $T_{amb} \geq T_{th(crit)} - T_{hys}$
14	AAW	Above Alarm Window. Increasing $T_{amb}$ : 0 — $T_{amb} \leq T_{trip(u)}$ 1 — $T_{amb} > T_{trip(u)}$ Decreasing $T_{amb}$ : 0 — $T_{amb} \leq T_{trip(u)} - T_{hys}$ 1 — $T_{amb} > T_{trip(u)} - T_{hys}$
13	BAW	Below Alarm Window. Increasing $T_{amb}$ : 0 — $T_{amb} \geq T_{trip(l)}$ 1 — $T_{amb} < T_{trip(l)}$ Decreasing $T_{amb}$ : 0 — $T_{amb} \geq T_{trip(l)} - T_{hys}$ 1 — $T_{amb} < T_{trip(l)} - T_{hys}$
12	SIGN	Sign bit. 0 — positive temperature value 1 — negative temperature value
11:1	TEMP	Temperature Value (2's complement). (LSB = 0.125 °C)
0	RFU	reserved; always 0

## 8.7 Manufacturer's ID register (16-bit read-only)

The manufacturer's ID matches that assigned to NXP Semiconductors PCI-SIG (1131h), and is intended for use to identify the manufacturer of the device.

**Table 20. Manufacturer's ID register bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Reset	0	0	0	1	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	(continued)							
Reset	0	0	1	1	0	0	0	1
Access	R	R	R	R	R	R	R	R

## 8.8 Device ID register

The device ID and device revision are A1h and 02h, respectively.

**Table 21. Device ID register bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Reset	1	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	Device revision							
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R