Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SEC2410/SEC4410

HS Endpoint Processor with USB 2.0, Smart Card, & FMC for Secure Token & Storage

PRODUCT FEATURES

Datasheet

General Description

The SMSC SEC2410/SEC4410 are USB 2.0 compliant, hi-speed bulk-only mass storage class peripheral controllers. They are intended to be used to read and write to popular flash media, including Secure Digital (SD), and MultiMediaCard™ (MMC) families.

The SMSC SEC2410/SEC4410 are fully integrated, single-chip solutions capable of ultra-high performance operation. Average sustained transfer rates exceeding 35 MB/s are possible if the media and host can support those rates. The SMSC SEC2410/SEC4410 includes provisions to read/write to secure media formats, as well as support AES encryption, without performance impact.

General Features

- The SEC2410/SEC4410 is available in two lead-free RoHS compliant packages:
  - 64-pin QFN (9x9 mm) package
  - 72-pin QFN (10x10 mm) package that includes debug pins to interface to standard ARM debug tools
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media
- Order number (see next page) with *i* denote the products that support the industrial temperature range of -40ºC to 85ºC
- Support included for secure media format on a licensed, customized basis
  - SD Secure

Hardware Features

- Single-chip flash media controller containing:
  - A multiplexed interface for use with combo card sockets
  - SD/MMC flash media reader/writer
- SDIO and MMC streaming mode support
- Extended configuration options
- Media Activity LED
- GPIO configuration and polarity
  - Up to 32 GPIOs for special function use
  - One GPIO with up to 200 mA drive
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
- Internal card power FET
  - 200 mA
  - "Fold-back" short circuit protection
- ARM M3 32-bit microprocessor
  - 60 MHz execution speed at 1 cycle per instruction (minimum)
  - 32 KBytes of internal SRAM for a general purpose scratchpad
  - 96 KByte SRAM available for code execution
  - 32 KByte internal code ROM
  - JTAG interface
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage for additional bill of materials and power savings
- Optimized pinout improves signal routing, easing implementation for improved signal integrity
- 1.2 V reference voltage for HSIC (SEC4410 only)

Flash Media Specification Compliance

- Secure Digital 2.0
  - HS-SD, SDHC, SDXC
  - TransFlash™ and reduced form factor media
- MultiMediaCard
  - MMC version 4.2: 1/4/8-bit
  - eMMC version 4.4

Software Features

- Customizable vendor-specific data
- Reduced memory footprint

Applications

- Secure dongles and storage
- Flash media card reader/writers
- Desktop and mobile PCs
- Consumer A/V and media players/viewers
- Compatible with
  - Microsoft® Vista™ and Vista ReadyBoost™
  - Windows® 7, XP, ME, 2K SP4
  - Apple Mac OSx®
  - Linux Mass Storage Class Drivers

Order Numbers:

ORDER NUMBERS	LEAD-FREE ROHS COMPLIANT PACKAGE	PACKAGE SIZE (mm)	TEMPERATURE RANGE
SEC2410/SEC2410-JZX	64QFN	9x9	0ºC to 85ºC
SEC4410/SEC4410i-JZX			-40ºC to 85ºC
SEC2410/SEC2410-AKZE	72QFN	10x10	0ºC to 85ºC
SEC4410/SEC4410i-AKZE			-40ºC to 85ºC

This product meets the halogen maximum concentration values per IEC61249-2-21.

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Section Name	Section or Document name
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

Chapter 1 General Description

SEC2410/SEC4410 is a flash media card reader solution intended to provide a flexible means of providing embedded Audio/video systems (TVs, DVD players, STBs, Portable Media Copiers or Players, etc.) access to Media files stored on Flash Media Cards such as Secure Digital/MultiMediaCard (SD/MMC), and NAND Flash.

SEC2410/SEC4410 is fully compliant with the *USB 2.0 Specification*. All required transivers and resistors of the USB ports are integrated into the device. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors. One Control, One interrupt Pair, and Two Bulk Pair Endpoints are provided with reconfigurable Endpoint Buffers.

SEC2410/SEC4410 incorporates a powerfull ARM M3 32-bit microprocessor with 60 MHz execution speed at 1 cycles per instruction (minimum).

Following memories are embedded:

- 32 KBytes of internal SRAM for general purpose scratchpad
- 96 KByte SRAM available for code execution
- 32 KByte Internal Code ROM
- 10 KBytes of reconfigurable Endpoint Buffers
- 2 KByte OTP

It also supports optional 4 MByte External Code Space using SPI Flash memory.

SEC2410/SEC4410 has on-chip SD/MMC Controller. It supports:

- High-Speed MMC version 4.2: 1/4/8 bit MMC
- eMMC version 4.4
- High-Speed SD card, SDHC
- SDXC in SDR25 Mode (no support for SD card UHS25, SDR50, or SDR100).
- TransFlash™ and reduced form factor media.
- Hardware support for Secure Digital(SD) Pass-Through
- Hardware support for SD Security Command Extensions
- Hardware support for SDIO (SD Input/Output)

It has on-chip power FET's for supplying flash media card power with minimum board components.

SEC2410/SEC4410 supports SmartCard interface, ISO/IEC 7816 compliant and has Integrated 3/1.8 Volt regulator.

Integrated cryptographical module offers AES encryption with AES 128, AES 192, AES 256 key sizes and ECB, CBC or CTR implementation.

SEC2410/SEC4410 offers up to 32 GPIOs with diverse configuration and polarity options for special function such as LED indicators, button inputs, and power control to memory devices. The number of actual GPIOs depends on the implemented configuration. One GPIO available with up to 200 mA drive and “fold-back” short circuit protection

SEC2410/SEC4410 has a 24 MHz Crystal Driver Circuit and internal PLL for 480 MHz USB 2.0 Sampling on board.

It supports a single external 3.3 V supply source. Internal regulators provide 1.2 V internal core voltage for additional bill of materials and power savings.

SEC2410/SEC4410 is offered as a single chip flash media controller in 64-pin and 72-pin QFN, lead-free RoHS compliant packages in either SEC2410/SEC4410 commercial temperature range from 0°C to +70°C or industri alfrom -40°C to +85°C.

It supports USB Mass Storage Compliant Bootable BIOS, firmware upgrade via USB bus for SPI Flash and SD/MMC cards (“boot block flash” not required).

Compatible with Microsoft Vista; Windows 7, XP, and 2K SP3&4; Mac OS X 10; and Linux Multi-LUN Mass Storage Class Drivers

1.1 SEC2410 Block Diagram

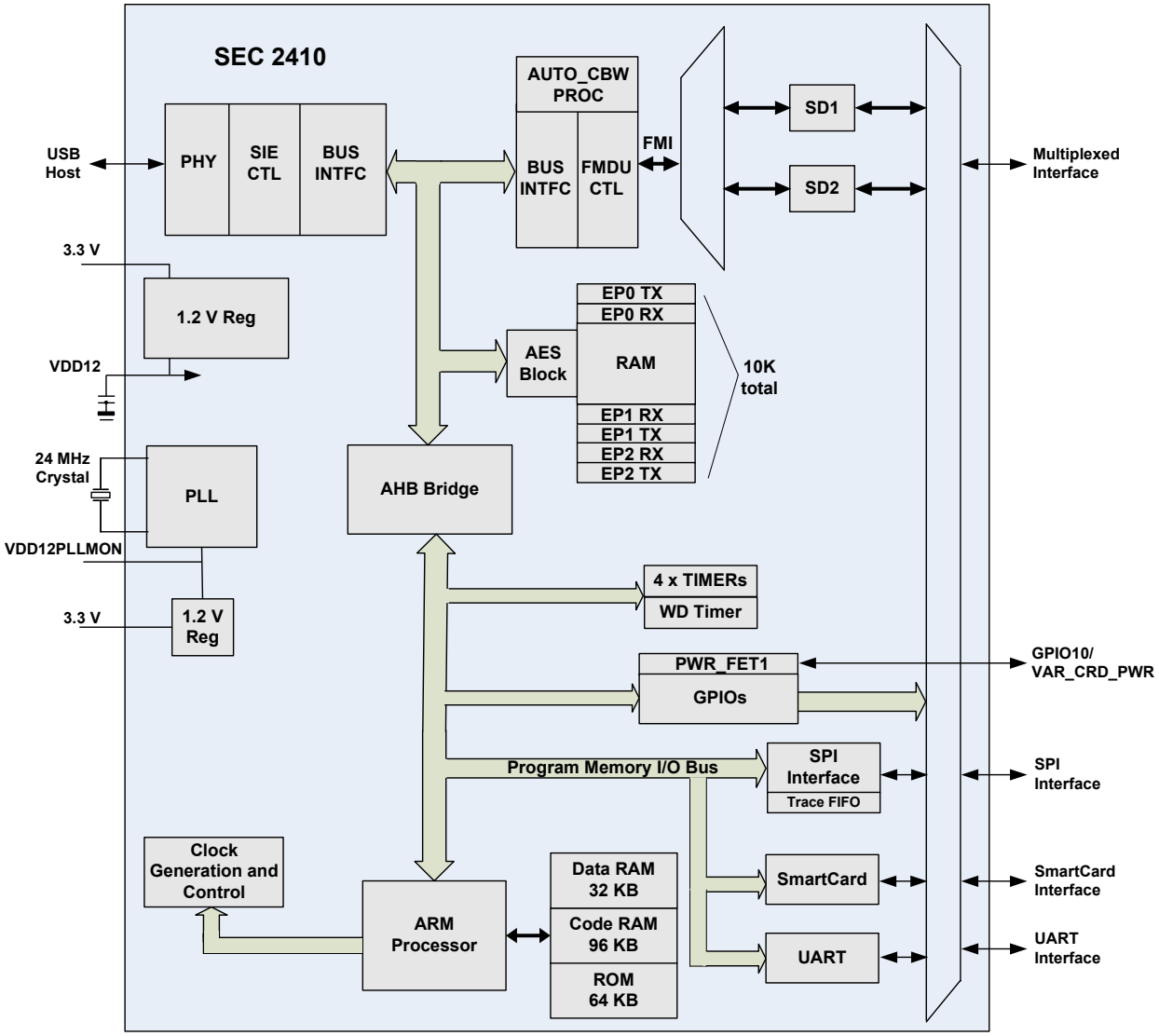

Figure 1.1 SEC2410 Block Diagram

1.2 SEC4410 Block Diagram

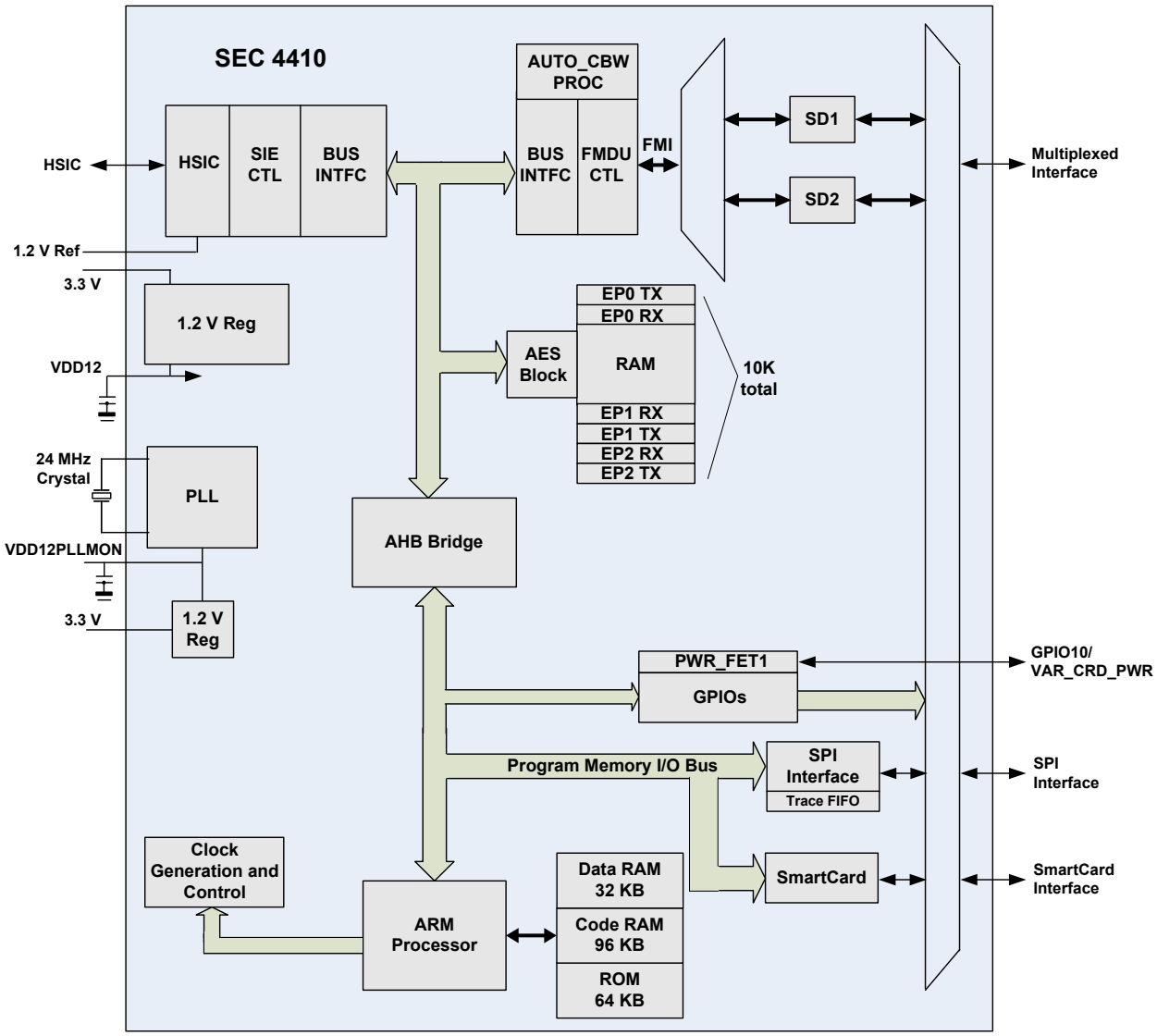

Figure 1.2 SEC4410 Block Diagram

Chapter 2 Configuration Options

The SEC2410/SEC4410 can be configured to support the desired interfaces as outlined in the sections below. The SEC2410/SEC4410 can be programmed using one of the configured interfaces as outlined in Chapter 22: *Bootloader* on page 290. Programming the SEC2410/SEC4410 using any of the described interfaces is outlined in the *Software Development Reference Guide* [6].

2.1 SPI ROM

The SPI ROM must be 1 Mbit or larger and support either 30 MHz or 60 MHz. The frequency used is set using **SPD_SEL**. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor. During **RESET_N** assertion, the **SPD_SEL** pin is tri-stated. When **RESET_N** is negated, the value on the pin is internally latched, and the pin reverts to **SPI_DO** functionality.

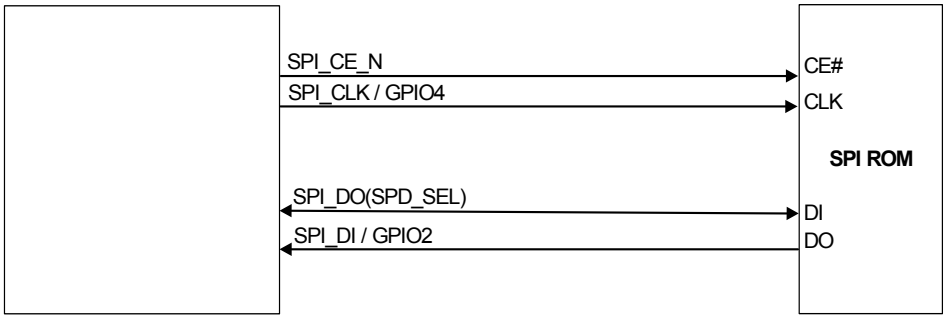

Figure 2.1 SPI ROM Connection

2.2 Supported System Configurations

This chapter illustrates some possible configurations available for SEC2410/SEC4410.

2.2.1 SD Plus SC Configuration

This one one SD interface, Smartcard and rest are 3.3 Volt GPIOs.

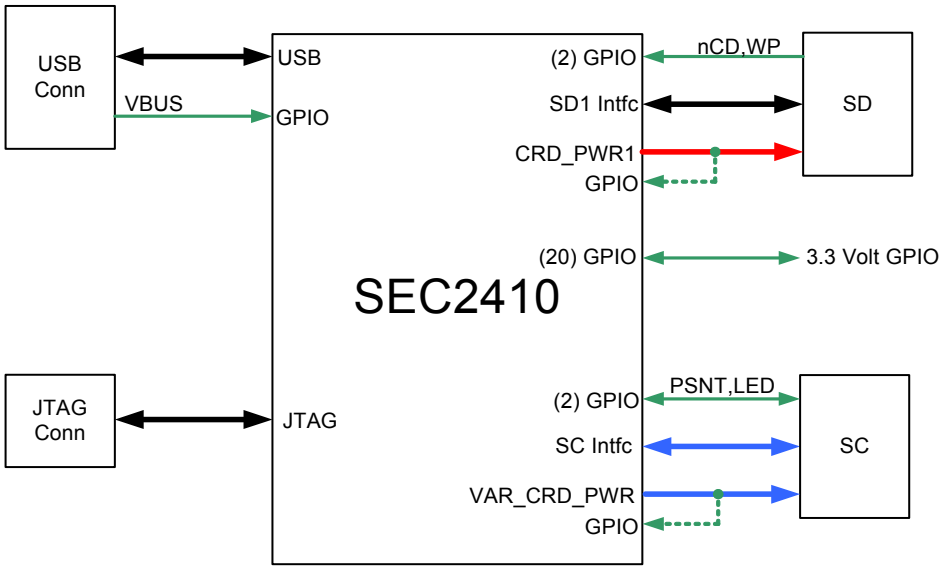

Figure 2.2 SD Plus SC Configuration

2.2.2 Dual SD Configuration

In this configuration two SD/MMC cards are supported. There are 5 variable voltage GPIOs available and 6 fixed voltage GPIOs.

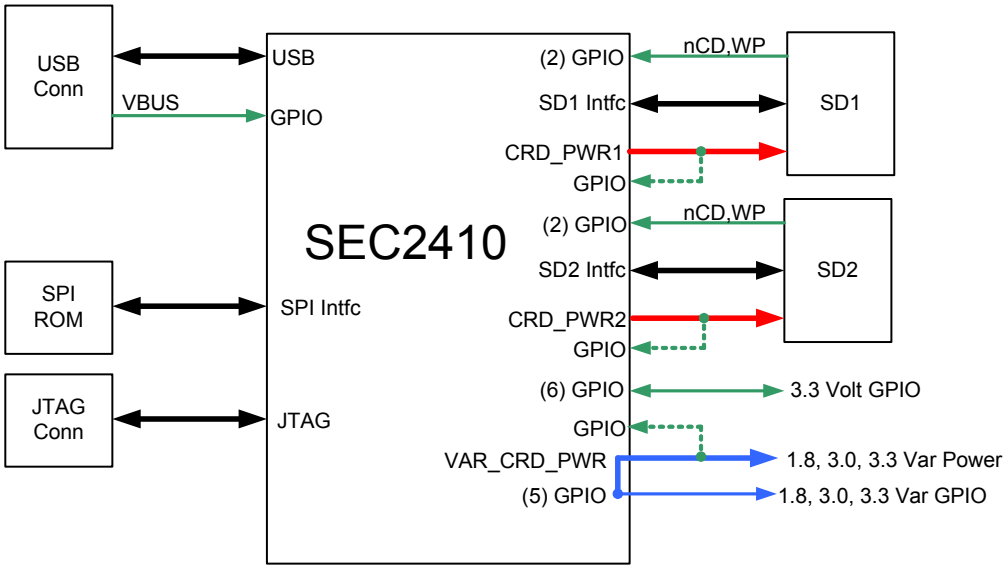

Figure 2.3 Dual SD Configuration

2.2.3 GPIO Only Configuration

In this configuration, the device would have to boot from USB and would be used as a GPIO controller.

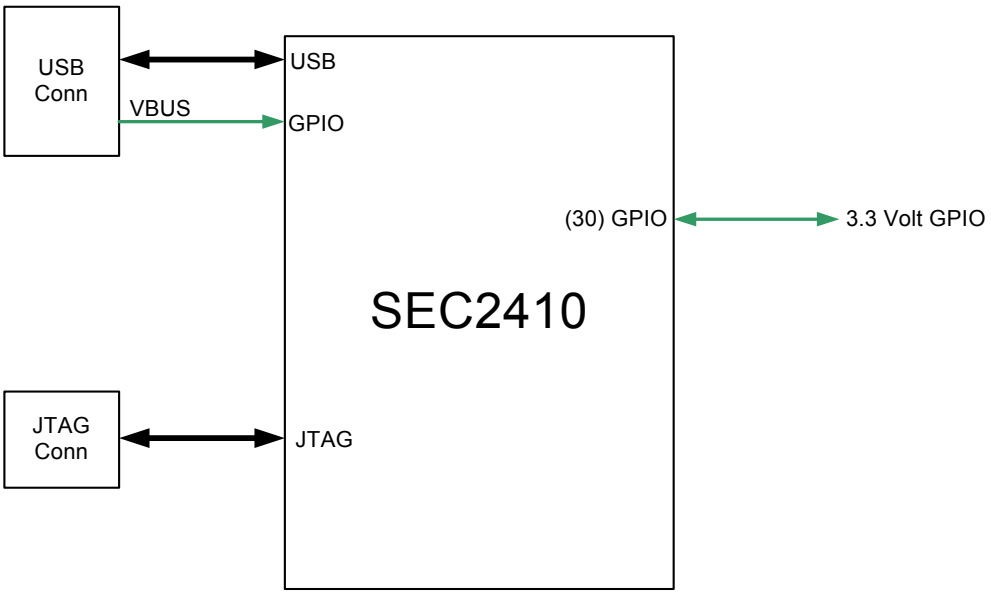

Figure 2.4 GPIO Only Configuration

Chapter 3 Pin Information

This chapter outlines the pin configurations for each package type available, followed by a corresponding pin list organized by group. The detailed pin descriptions are then outlined in Section 3.3: *Pin Descriptions* on page 16.

3.1 Pin Configurations

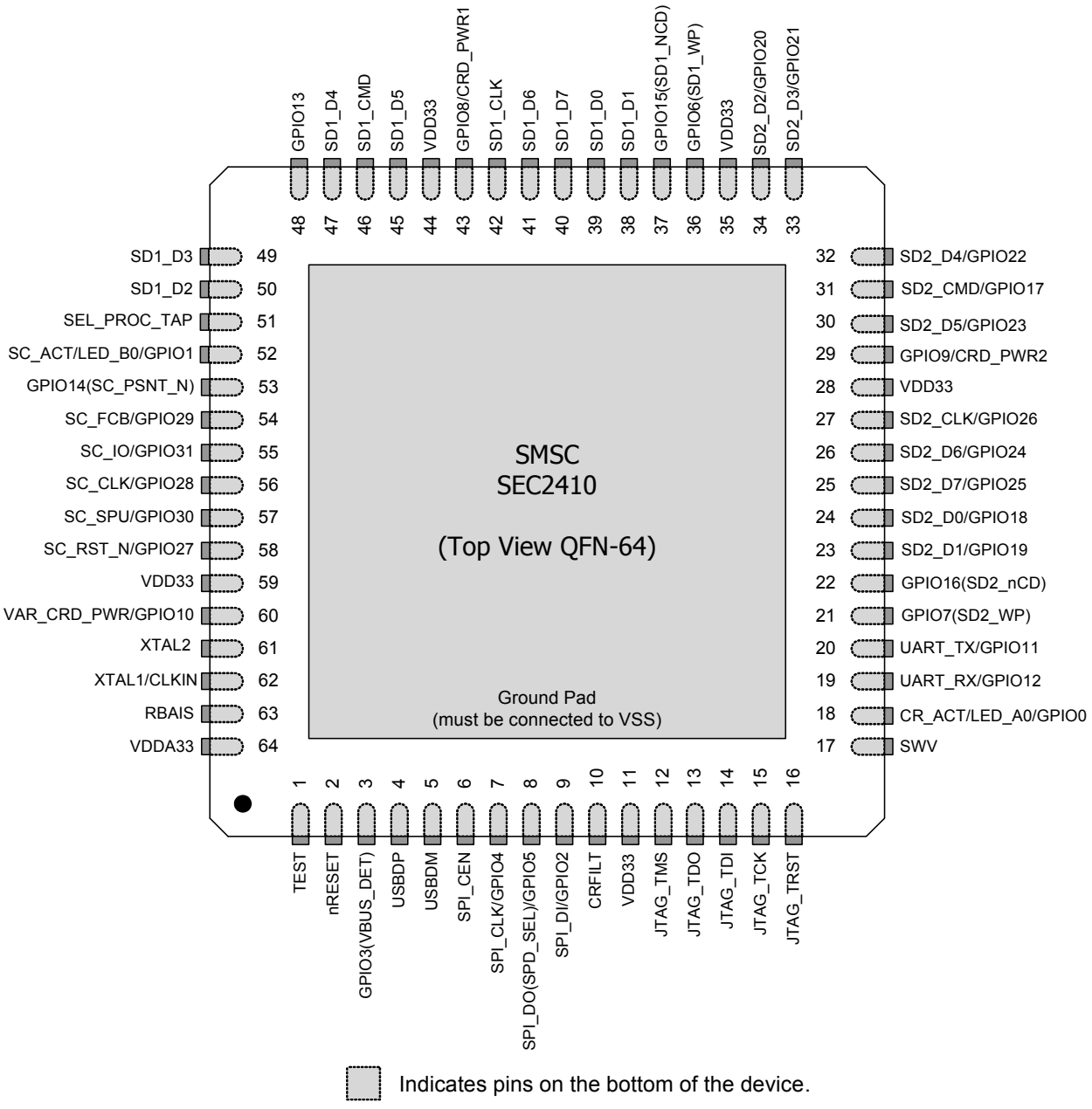

Figure 3.1 SEC2410 64-Pin QFN Package

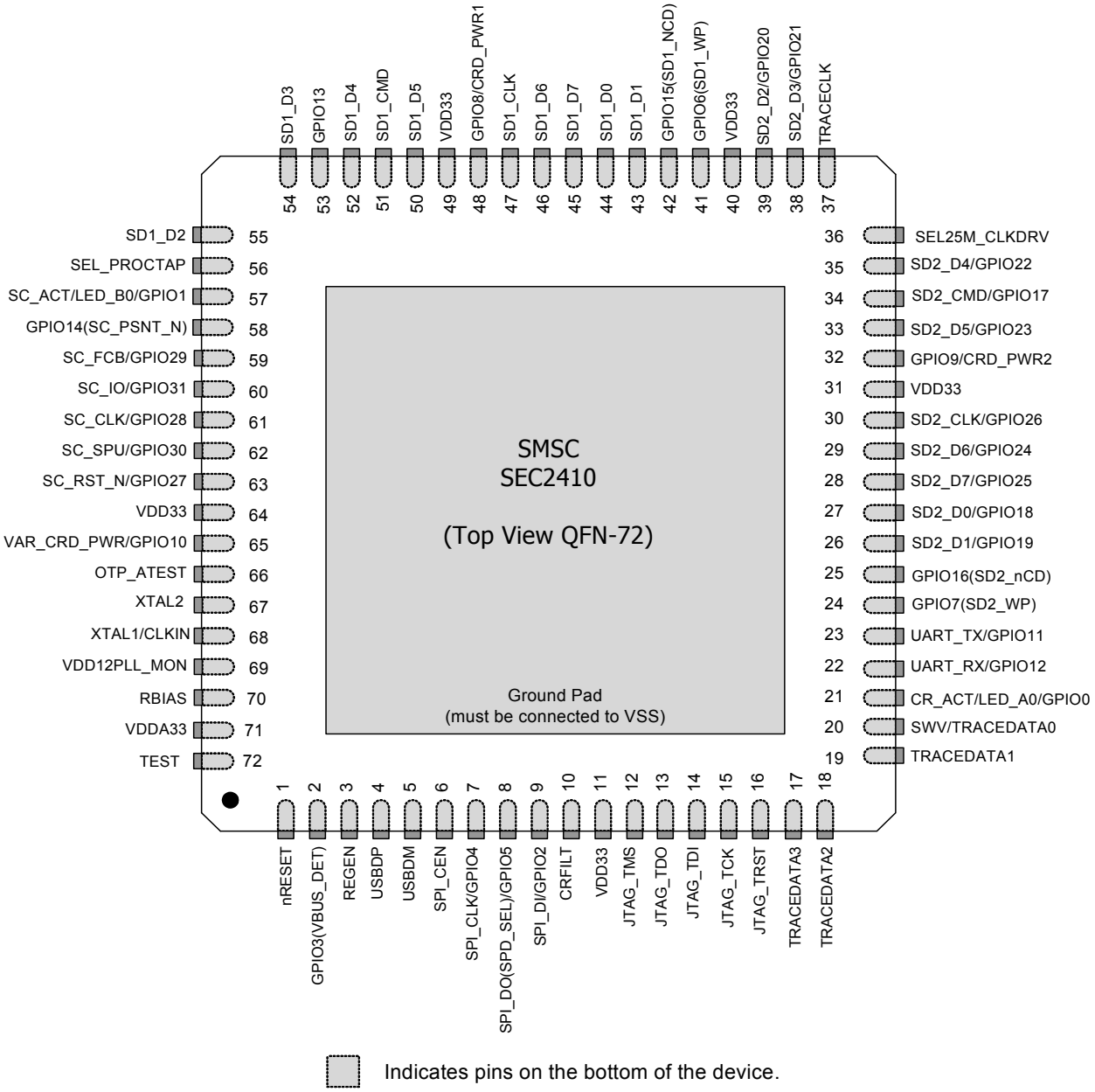

Figure 3.2 SEC2410 72-Pin QFN Package

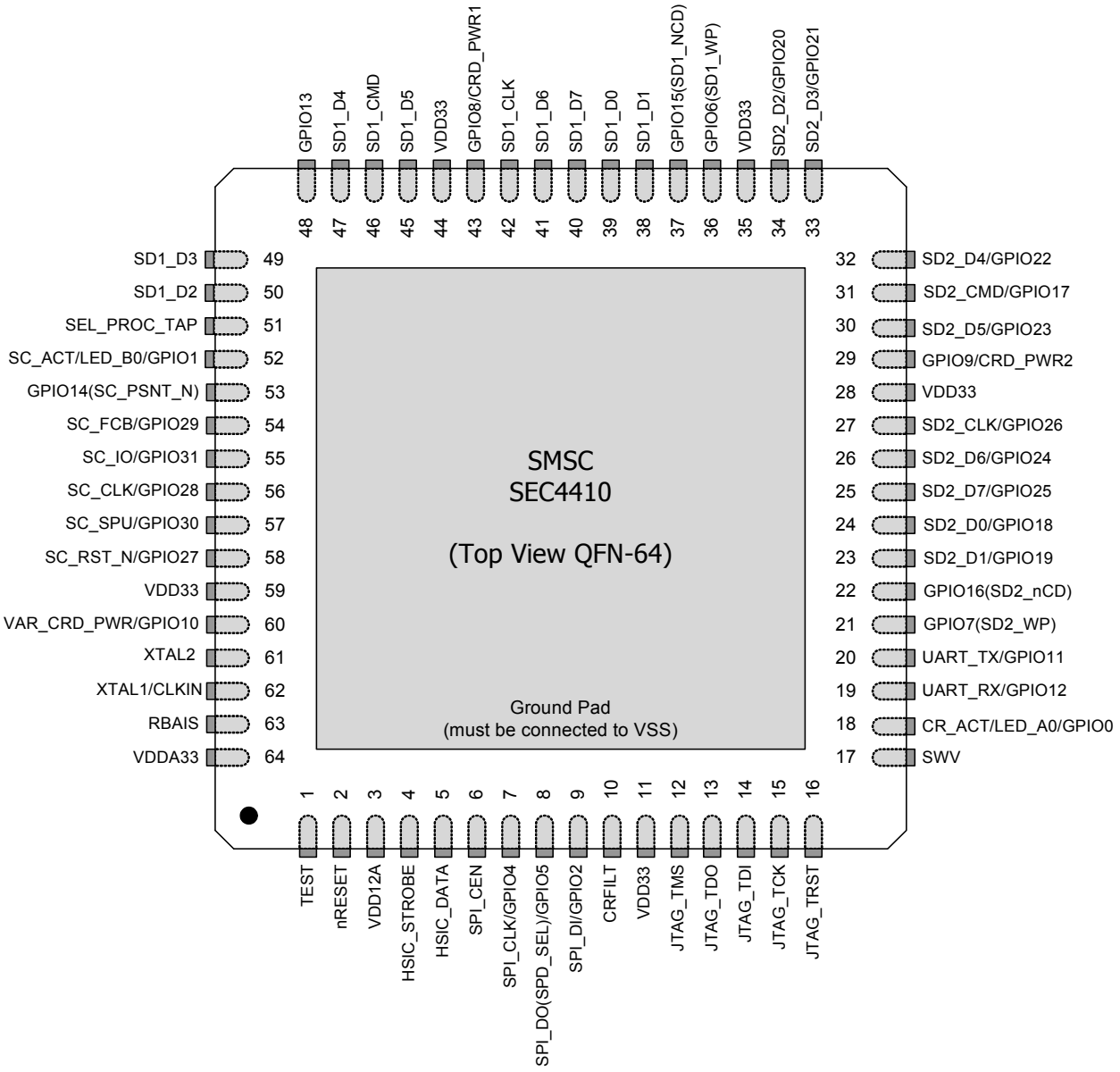

Figure 3.3 SEC4410 64-Pin QFN Package

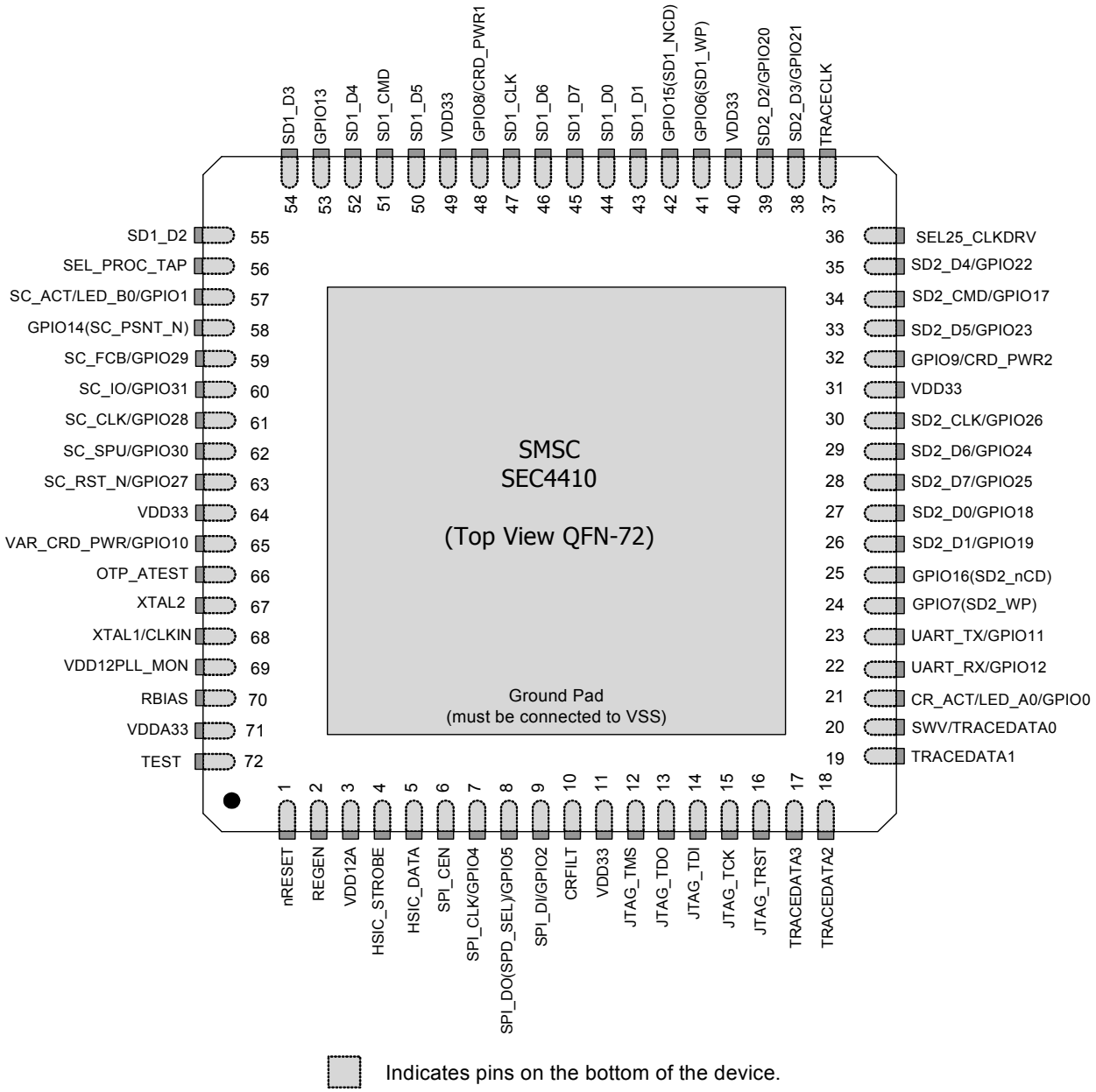

Figure 3.4 SEC4410 72-Pin QFN Package

3.2 Pin List (Grouped by Function)

Table 3.1 SEC2410 Pins Grouped by Function

SECURE DIGITAL/MULTIMEDIACARD INTERFACE (12 PINS)			
SD1_D0	SD1_D1	SD1_D2	SD1_D3
SD1_D4	SD1_D5	SD1_D6	SD1_D7
SD1_CMD	SD1_CLK	GPIO6 (SD1_WP)	GPIO15 (SD1_nCD)
SECOND SECURE DIGITAL INTERFACE (12 PINS)			
SD2_D0/ GPIO18	SD2_D1/ GPIO19	SD2_D2/ GPIO20	SD2_D3/ GPIO21
SD2_D4/ GPIO22	SD2_D5/ GPIO23	SD2_D6/ GPIO24	SD2_D7/ GPIO25
SD2_CLK/ GPIO26	SD2_CMD/ GPIO17	GPIO7 (SD2_WP)	GPIO16 (SD2_nCD)
SPI MASTER/I^{2}C INTERFACE (4 PINS)			
SPI_CEN	SPI_CLK/ GPIO4	SPI_DI/ GPIO2	SPI_DO (SPD_SEL)/ GPIO5
SMARTCARD (8 PINS)			
SC_RST_N/ GPIO27	SC_CLK/ GPIO28	SC_IO/ GPIO31	VAR_CRD_PWR/ GPIO10
SC_SPU/ GPIO30	GPIO14 (SC_PSNT_N)	SC_ACT/ LED_B0 GPIO1	SC_FCB/ GPIO29
USB INTERFACE (7 PINS)			
USBDP	USBDM	RBIAS	VDDA33
GPIO3 (VBUS_DET)	XTAL1/CLKIN	XTAL2	
JTAG INTERFACE (5 PINS)			
JTAG_TMS	JTAG_TDO	JTAG_TDI	JTAG_TCK
JTAG_TRST			
MISC (9 PINS)			
RESET_N	CR_ACT/ LED_A0/ GPIO0	TEST	GPIO9/ CRD_PWR
UART_TX/ GPIO11	UART_RX/ GPIO12	GPIO13	SEL_PROC_TAP
NC			

Table 3.1 SEC2410 Pins Grouped by Function (continued)

DIGITAL, POWER (6 PINS)			
(5) VDD33	(1) VDD12PLL_MON		
TOTAL 64			
EXTRA PINS FOR 72-PIN PACKAGE			
SWV/TRACEDATA0	TRACEDATA1	TRACEDATA2	TRACEDATA3
TRACECLK	SEL25M_CLKDRIVE		

Table 3.2 SEC4410 Pins Grouped by Function

SECURE DIGITAL/MULTIMEDIACARD INTERFACE (12 PINS)			
SD1_D0	SD1_D1	SD1_D2	SD1_D3
SD1_D4	SD1_D5	SD1_D6	SD1_D7
SD1_CMD	SD1_CLK	GPIO6 (SD1_WP)	GPIO15 (SD1_nCD)
SECOND SECURE DIGITAL INTERFACE (12 PINS)			
SD2_D0/ GPIO18	SD2_D1/ GPIO19	SD2_D2/ GPIO20	SD2_D3/ GPIO21
SD2_D4/ GPIO22	SD2_D5/ GPIO23	SD2_D6/ GPIO24	SD2_D7/ GPIO25
SD2_CLK/ GPIO26	SD2_CMD/ GPIO17	GPIO7 (SD2_WP)	GPIO16 (SD2_nCD)
SPI MASTER/I2C INTERFACE (4 PINS)			
SPI_CEN	SPI_CLK/ GPIO4	SPI_DI/ GPIO2	SPI_DO (SPD_SEL)/ GPIO5
SMARTCARD (8 PINS)			
SC_RST_N/ GPIO27	SC_CLK/ GPIO28	SC_IO/ GPIO31	VAR_CRD_PWR/ GPIO10
SC_SPU/ GPIO30	GPIO14 (SC_PSNT_N)	SC_ACT/ LED_B0 GPIO1	SC_FCB/ GPIO29
USB INTERFACE (8 PINS)			
HSIC_DATA	HSIC_STROBE	VDD12A	VDDA33
GPIO3 (VBUS_DET)	XTAL1/CLKIN	XTAL2	RBIAS

Table 3.2 SEC4410 Pins Grouped by Function (continued)

JTAG INTERFACE (5 PINS)			
JTAG_TMS	JTAG_TDO	JTAG_TDI	JTAG_TCK
JTAG_TRST			
MISC (9 PINS)			
RESET_N	CR_ACT/ LED_A0/ GPIO0	TEST	GPIO9/ CRD_PWR
UART_TX/ GPIO11	UART_RX/ GPIO12	GPIO13	SEL_PROC_TAP
NC			
DIGITAL, POWER (6 PINS)			
(5) VDD33	(1) VDD12PLL_MON		
TOTAL 64			
EXTRA PINS FOR 72-PIN PACKAGE			
SWV/TRACEDATA0	TRACEDATA1	TRACEDATA2	TRACEDATA3
TRACECLK	SEL25M_CLKDRIVE		

Note: Pads required for bond options are not listed in the above tables.

3.3 Pin Descriptions

Table 3.3 SEC2410 Pin Descriptions

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
1	72	TEST	I	TEST Input This pin should be tied to ground for normal operation.
2	1	RESET_N	IS	RESET Input This active low signal is used by the system to reset the chip, where the active low pulse should be at least 1 µs wide.
3	2	GPIO3 (VBUS_DET)	I/O12	Detect Upstream VBUS Power Detects the state of the upstream VBUS power. The SMSC hub monitors **VBUS_DET** to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically **VDD33**).
-	3	REG_EN	IPU	Regulator Enable This pin is internally pulled up to enable the internal 1.2 V regulators, and should be treated as a no-connect. In order to disable the regulators, this pin will need to be externally connected to ground. When the internal regulator is enabled, the 1.2 V power pins must be left unconnected, except for the required bypass capacitors.
4		USBDP	I/O-U	USB Data Plus Connect to the upstream USB bus data signals (host, port, or upstream hub).
5		USBDM	I/O-U	USB Data Minus Connect to the upstream USB bus data signals (host, port, or upstream hub).
6		SPI_CEN	I/O12	SPI Chip Enable Active low chip enable output. If the SPI interface is enabled, this pin must be driven high in power down states.
7		SPI_CLK/ GPIO4	I/O12	SPI Clock Out Clock signal out to the serial ROM. **Note:** During reset, this pin must be driven low.

Table 3.3 SEC2410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
8		SPI_DO/ (SPD_SEL)/ GPIO5	I/O12	SPI Serial Data Out The output for the SPI port. SPI Speed Select Selects the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, where the internal pull-down will be disabled. 0 : 30 MHz (no external resistor should be applied) 1 : 60 MHz (a 10 kΩ external pull-up resistor must be applied) If the latched value is 1, then the pin is tri-stated when the chip is in the suspend state. If the latched value is 0, then the pin is driven low during a suspend state.
9		SPI_DI/ GPIO2	I/O12PD	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
10		CRFILT		+1.2 V Core Power Bypass This pin must have a 1.0 µF (or greater) ± 20% (ESR < 0.1 Ω) capacitor to VSS.
11		VDD33		3.3 V Power
12		JTAG_TMS	I	JTAG Mode Select The JTAG mode select to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.
13		JTAG_TDO	O12	JTAG Data Out The JTAG data out from the internal debug/test controller, which must be disabled during reset.
14		JTAG_TDI	I	JTAG Data In The JTAG data in to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.
15		JTAG_TCK	I	JTAG Clock The JTAG clock input to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.
16		JTAG_TRST	I	JTAG Reset The JTAG reset input to the internal debug/test controller, which must be tied low on the PCB when no debugger is used.
-	17	TRACEDATA3	O12	Trace Output Data Trace output data bit 3 from internal trace module when enabled.
-	18	TRACEDATA2	O12	Trace Output Data Trace output data bit 2 from internal trace module when enabled.

Table 3.3 SEC2410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
-	19	TRACEDATA1	O12	Trace Output Data Trace output data bit 1 from internal trace module when enabled.
17	20	SWV/	I/O12	Serial Wire Viewer Single wire output of the internal trace module, when enabled for single wire operation.
-		TRACEDATA0	O12	Trace Output Data Trace output data bit 0 from internal trace module when enabled.
18	21	CR_ACT/	I/O12	Card Reader Activity LED This pin can be configured to indicate card reader activity.
		LED_A0/ GPIO0		LED A0 This pin can be configured as a general purpose LED.
19	22	UART_RX/ GPIO12	I	UART Receive This is a 3.3 V receive signal for the internal UART. For RS232 operation, an external 12 V translator is required.
20	23	UART_TX/ GPIO11	O12	UART Transmit This is a 3.3 V transmit signal for the internal UART. For RS232 operation, an external 12 V driver is required.
21	24	GPIO7 (SD2_WP)	I/O12	SD2 Write Protect Detection The secure digital card mechanical write protect detection pin.
22	25	GPIO16 (SD2_nCD)	IPU	SD2 Card Detect The secure digital card detection pin.
23	26	SD2_D1/ GPIO19	I/O12PU	SD2 Data 1 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
24	27	SD2_D0/ GPIO18	I/O12PU	SD2 Data 0 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
25	28	SD2_D7/ GPIO25	I/O12PU	SD2 Data 7 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
26	29	SD2_D6/ GPIO24	I/O12PU	SD2 Data 6 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
27	30	SD2_CLK/ GPIO26	O12	SD2 Clock An output clock signal to SD2/MMC device, where the clock frequency is software configurable.
28	31	VDD33		3.3 V Power
29	32	GPIO9/ CRD_PWR	I/O200	Card Power 2 Drive The card power drive of 3.3 V at 200 mA.
30	33	SD2_D5/ GPIO23	I/O12PU	SD2 Data 5 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.

Table 3.3 SEC2410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
31	34	SD2_CMD/ GPIO17	I/O12PU	SD2 Command A bi-directional signal that connects to the CMD signal of the SD2/MMC device and has a weak internal pull-up resistor.
32	35	SD2_D4/ GPIO22	I/O12PU	SD2 Data 4 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
-	36	SEL25M_CLKDRIVE	I	Select 25 MHz Clock This pin selects the 25 MHz OSC as the clock source. 0 : clock source is 24 Hz XTAL 1 : clock source is 25MHz OSC on **XTAL1/CLKIN** (**XTAL2** is not used) When present on a package this pin MUST be tied high or tied low (direct connection 3.3 V or ground is acceptable). There is no internal pull-up or pull-down.
-	37	TRACECLK	O12	Debug Trace Clock The clock out of the ETM trace module when debugging is enabled.
33	38	SD2_D3/ GPIO21	I/O12PU	SD2 Data 3 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
34	39	SD2_D2/ GPIO20	I/O12PU	SD2 Data 2 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
35	40	VDD33		3.3 V Power
36	41	GPIO6 (SD1_WP)	I/O12	SD1 Write Protect Detection The secure digital card mechanical write protect detection pin.
37	42	GPIO15 (SD1_nCD)	IPU	SD1 Card Detect This secure digital card detection pin.
38	43	SD1_D1	I/O12PU	SD1 Data 1 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
39	44	SD1_D0	I/O12PU	SD1 Data 0 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
40	45	SD1_D7	I/O12PU	SD1 Data 7 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
41	46	SD1_D6	I/O12PU	SD1 Data 6 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
42	47	SD1_CLK	O12	SD1 Clock An output clock signal to SD1/MMC device, where the clock frequency is software configurable.
43	48	NC		No Connect
44	49	VDD33		3.3 V Power

Table 3.3 SEC2410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
45	50	SD1_D5	I/O12PU	SD1 Data 5 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
46	51	SD1_CMD	I/O12PU	SD1 Command A bi-directional signal that connects to the CMD signal of the SD1/MMC device and has a weak internal pull-up resistor.
47	52	SD1_D4	I/O12PU	SD1 Data 4 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
48	53	GPIO13	IPU	General Purpose I/O Pin
49	54	SD1_D3	I/O12PU	SD1 Data 3 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
50	55	SD1_D2	I/O12PU	SD1 Data 2 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
51	56	SEL_PROC_TAP	I	Processor Test Controller Select This pin must be tied low (direct connection to ground is acceptable) for normal operation. This pin should only be pulled high when debugging.
52	57	SC_ACT/	O12	SmartCard Active This signal indicates that the SmartCard is active and selects the 25 MHz OSC as the clock source. 0 : clock source is 24 Hz XTAL 1 : clock source is 25MHz OSC on **XTAL1/CLKIN** (**XTAL2** is not used) When present on a package this pin MUST be tied high or tied low (direct connection to ground or 3.3 V is acceptable). **Note:** There is no internal pull-up or pull-down.
		LED_B0/ GPIO1		LED B0 This pin can be configured as a general purpose LED.
53	58	GPIO14 (SC_PSNT_N)	IPU	SmartCard Insertion This pin is designated as the SmartCard card detection pin and can be left unconnected if the socket is not used.
54	59	SC_FCB/ GPIO29	O12	SmartCard Function Code This pin is used in conjuction with **SC_RST_N** for type 2 synchronous cards to indicate the type of command to be executed. This pin is held low while **SC_PSNT_N** is low and card power has not been applied, or while SmartCard block is deactivated.
55	60	SC_IO/ GPIO31	VIO12	SmartCard Bidirectional Serial Data The SmartCard bidirectional serial data pin should be held low when the interface is not active.

Table 3.3 SEC2410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
56	61	SC_CLK/ GPIO28	VIO12	SmartCard Clock Output This pin is the clock reference for communication with the flash media card. This pin should be held low when the interface is not active.
57	62	SC_SPU/ GPIO30	VIO12	SmartCard Standard or Proprietary Use This pin is held low while **SC_PSNT_N** is low and card power has not been applied, or while SmartCard block is deactivated.
58	63	SC_RST_N/ GPIO27	VIO12	SmartCard Reset Output A low pulse resets the card and triggers an ATR response message. This pin should be held low when the interface is not active.
59	64	VDD33		3.3 V Power
60	65	VAR_CRD_PWR/ GPIO10	I/O200	Variable Voltage Card Power: 1.8 V, 3.0 V, 3.3 V (200 mA) This pin should have a 1.0 µF Ceramic low ESR Capacitor when configured for output.
-	66	OTP_ATEST		This is a test pin and should be left un-connected for normal operation.
61	67	XTAL2	OCLKx	24 MHz Crystal This is the other terminal of the crystal, or can be left open when an external clock source is used to drive **XTAL1/CLKIN**.
62	68	XTAL1/ CLKIN	ICLKx	24 MHz Crystal (External Clock Input) This pin can be connected to one terminal of the crystal or can be connected to an external 24 MHz clock when a crystal is not used.
-	69	VDD12PLL_MON		This pin should be left unconnected - for testing only.
63	70	RBIAS	I-R	USB Transceiver Bias A 12.0 kΩ, ± 1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
64	71	VDDA33		3.3 V Analog Power

Table 3.4 SEC4410 Pin Descriptions

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
1	72	TEST	I	TEST Input This pin should be tied to ground for normal operation.
2	1	RESET_N	IS	RESET Input This active low signal is used by the system to reset the chip, where the active low pulse should be at least 1 µs wide.

Table 3.4 SEC4410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
-	2	REG_EN	IPU	Regulator Enable This pin is internally pulled up to enable the internal 1.2 V regulators, and should be treated as a no-connect. In order to disable the regulators, this pin will need to be externally connected to ground. When the internal regulator is enabled, the 1.2 V power pins must be left unconnected, except for the required bypass capacitors.
3		VDD12A		1.2 V HSIC Reference Voltage In
4		HSIC_STROBE	I/O	HSIC Strobe Bi-directional data strobe signal defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
5		HSIC_DATA	I/O	HSIC Data Bi-directional double data rate (DDR) data signal that is synchronous to the **HSIC_STROBE** signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
6		SPI_CEN	I/O12	SPI Chip Enable Active low chip enable output. If the SPI interface is enabled, this pin must be driven high in power down states.
7		SPI_CLK/ GPIO4	I/O12	SPI Clock Out Clock signal out to the serial ROM. **Note:** During reset, this pin must be driven low.
8		SPI_DO	I/O12	SPI Serial Data Out The output for the SPI port.
		(SPD_SEL)/ GPIO5		SPI Speed Select Selects the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, where the internal pull-down will be disabled. 0 : 30 MHz (no external resistor should be applied) 1 : 60 MHz (a 10 kΩ external pull-up resistor must be applied) If the latched value is 1, then the pin is tri-stated when the chip is in the suspend state. If the latched value is 0, then the pin is driven low during a suspend state.
9		SPI_DI/ GPIO2	I/O12PD	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
10		CRFILT		VDD Core Regulator Filter Capacitor: this pin must have a 1.0 µF (or greater) ± 20% (ESR < 0.1 Ω) capacitor to VSS.
11		VDD33		3.3 V Power
12		JTAG_TMS	I	JTAG Mode Select The JTAG mode select to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.

Table 3.4 SEC4410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
13		JTAG_TDO	O12	JTAG Data Out The JTAG data out from the internal debug/test controller, which must be disabled during reset.
14		JTAG_TDI	I	JTAG Data In The JTAG data in to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.
15		JTAG_TCK	I	JTAG Clock The JTAG clock input to the internal debug/test controller, which must have a pull-up resistor enabled during normal operation. The pull-up and the input must be disabled during reset.
16		JTAG_TRST	I	JTAG Reset The JTAG reset input to the internal debug/test controller, which must be tied low on the PCB when no debugger is used.
-	17	TRACEDATA3	O12	Trace Output Data Trace output data bit 3 from internal trace module when enabled.
-	18	TRACEDATA2	O12	Trace Output Data Trace output data bit 2 from internal trace module when enabled.
-	19	TRACEDATA1	O12	Trace Output Data Trace output data bit 1 from internal trace module when enabled.
17	20	SWV/	I/O12	Serial Wire Viewer Single wire output of the internal trace module, when enabled for single wire operation.
-		TRACEDATA0	O12	Trace Output Data Trace output data bit 0 from internal trace module when enabled.
18	21	CR_ACT/	I/O12	Card Reader Activity LED This pin can be configured to indicate card reader activity.
		LED_A0/ GPIO0		LED A0 This pin can be configured as a general purpose LED.
19	22	UART_RX/ GPIO12	I	UART Receive This is a 3.3 V receive signal for the internal UART. For RS232 operation, an external 12 V translator is required.
20	23	UART_TX/ GPIO11	O12	UART Transmit This is a 3.3 V transmit signal for the internal UART. For RS232 operation, an external 12 V driver is required.
21	24	GPIO7 (SD2_WP)	I/O12	SD2 Write Protect Detection The secure digital card mechanical write protect detection pin.
22	25	GPIO6 (SD2_nCD)	IPU	SD2 Card Detect The secure digital card detection pin.

Table 3.4 SEC4410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
23	26	SD2_D1/ GPIO19	I/O12PU	SD2 Data 1 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-up resistors.
24	27	SD2_D0/ GPIO18	I/O12PU	SD2 Data 0 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
25	28	SD2_D7/ GPIO25	I/O12PU	SD2 Data 7 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
26	29	SD2_D6/ GPIO24	I/O12PU	SD2 Data 6 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
27	30	SD2_CLK/ GPIO26	O12	SD2 Clock An output clock signal to SD2/MMC device, where the clock frequency is software configurable.
28	31	VDD33		3.3 V Power
29	32	GPIO9/ CRD_PWR	I/O200	Card Power 2 Drive The card power drive of 3.3 V at 200 mA.
30	33	SD2_D5/ GPIO23	I/O12PU	SD2 Data 5 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
31	34	SD2_CMD/ GPIO17	I/O12PU	SD2 Command A bi-directional signal that connects to the CMD signal of the SD2/MMC device and has a weak internal pull-up resistor.
32	35	SD2_D4/ GPIO22	I/O12PU	SD2 Data 4 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
-	36	SEL25M_CLKDRIVE	I	Select 25 MHz Clock This pin selects the 25 MHz OSC as the clock source. 0 : clock source is 24 Hz XTAL 1 : clock source is 25MHz OSC on **XTAL1/CLKIN** (**XTAL2** is not used) When present on a package this pin MUST be tied high or tied low (direct connection 3.3 V or ground is acceptable). There is no internal pull-up or pull-down.
-	37	TRACECLK	O12	Debug Trace Clock The clock out of the ETM trace module when debugging is enabled.
33	38	SD2_D3/ GPIO21	I/O12PU	SD2 Data 3 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
34	39	SD2_D2/ GPIO20	I/O12PU	SD2 Data 2 The **SD2_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
35	40	VDD33		3.3 V Power

Table 3.4 SEC4410 Pin Descriptions (continued)

PIN		NAME	BUFFER TYPE	DESCRIPTION
64-QFN	72-QFN			
36	41	GPIO6 (SD1_WP)	I/O12	SD1 Write Protect Detection The secure digital card mechanical write protect detection pin.
37	42	GPIO15 (SD1_nCD)	IPU	SD1 Card Detect This secure digital card detection pin.
38	43	SD1_D1	I/O12PU	SD1 Data 1 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
39	44	SD1_D0	I/O12PU	SD1 Data 0 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
40	45	SD1_D7	I/O12PU	SD1 Data 7 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
41	46	SD1_D6	I/O12PU	SD1 Data 6 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
42	47	SD1_CLK	O12	SD1 Clock An output clock signal to SD1/MMC device, where the clock frequency is software configurable.
43	48	NC		No Connect
44	49	VDD33		3.3 V Power
45	50	SD1_D5/	I/O12PU	SD1 Data 5 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
46	51	SD1_CMD/	I/O12PU	SD1 Command A bi-directional signal that connects to the CMD signal of the SD1/MMC device and has a weak internal pull-up resistor.
47	52	SD1_D4/	I/O12PU	SD1 Data 4 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
48	53	GPIO13	IPU	General Purpose I/O Pin
49	54	SD1_D3	I/O12PU	SD1 Data 3 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
50	55	SD1_D2/	I/O12PU	SD1 Data 2 The **SD1_D[7:0]** pins are bi-directional data signals that have weak pull-down resistors.
51	56	SEL_PROC_TAP	I	Processor Test Controller Select This pin must be tied low (direct connection to ground is acceptable) for normal operation. This pin should only be pulled high when debugging.