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MPU-9250
Register Map and Descriptions
Revision 1.6

CONTENTS

1 Revision History

Revision Date	Revision	Description
9/9/2013	1.4	Initial release
11/05/2014	1.5	Updated Section 4
01/07/2015	1.6	Updated Section 2

2 Purpose and Scope

This document provides information regarding the register map and descriptions for the Motion Processing Unit™ MPU-9250™. This document should be used in conjunction with the MPU-9250 Product Specification (PS-MPU-9250A-00) for detailed features, specifications, and other product information.

3 Register Map for Gyroscope and Accelerometer

The following table lists the register map for the gyroscope and accelerometer in the MPU-9250 MotionTracking device.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	SELF_TEST_X_GYRO	R/W	xg_st_data [7:0]							
01	1	SELF_TEST_Y_GYRO	R/W	yg_st_data [7:0]							
02	2	SELF_TEST_Z_GYRO	R/W	zg_st_data [7:0]							
0D	13	SELF_TEST_X_ACCEL	R/W	XA_ST_DATA [7:0]							
0E	14	SELF_TEST_Y_ACCEL	R/W	YA_ST_DATA [7:0]							
0F	15	SELF_TEST_Z_ACCEL	R/W	ZA_ST_DATA [7:0]							
13	19	XG_OFFSET_H	R/W	X_OFFS_USR [15:8]							
14	20	XG_OFFSET_L	R/W	X_OFFS_USR [7:0]							
15	21	YG_OFFSET_H	R/W	Y_OFFS_USR [15:8]							
16	22	YG_OFFSET_L	R/W	Y_OFFS_USR [7:0]							
17	23	ZG_OFFSET_H	R/W	Z_OFFS_USR [15:8]							
18	24	ZG_OFFSET_L	R/W	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	XGYRO_Cten	YGYRO_Cten	ZGYRO_Cten	GYRO_FS_SEL [1:0]		-	FCHOICE_B[1:0]	
1C	28	ACCEL_CONFIG	R/W	ax_st_en	ay_st_en	az_st_en	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	R/W	-				ACCEL_FCHOICE_B	A_DLPF_CFG		
1E	30	LP_ACCEL_ODR	R/W	-				Lposc_clksel [3:0]			
1F	31	WOM_THR	R/W	WOM_Threshold [7:0]							
23	35	FIFO_EN	R/W	TEMP_FIFO_EN	GYRO_XOUT	GYRO_YOUT	GYRO_ZOUT	ACCEL	SLV2	SLV1	SLV0
24	36	I2C_MST_CTRL	R/W	MULT_MST_EN	WAIT_FOR_ES	SLV_3_FIFO_EN	I2C_MST_P_NSR	I2C_MST_CLK[3:0]			
25	37	I2C_SLV0_ADDR	R/W	I2C_SLV0_RNW	I2C_ID_0 [6:0]						
26	38	I2C_SLV0_REG	R/W	I2C_SLV0_REG[7:0]							
27	39	I2C_SLV0_CTRL	R/W	I2C_SLV0_EN	I2C_SLV0_BYTE_SW	I2C_SLV0_REG_DIS	I2C_SLV0_GRP	I2C_SLV0_LENG[3:0]			
28	40	I2C_SLV1_ADDR	R/W	I2C_SLV1_RNW	I2C_ID_1 [6:0]						
29	41	I2C_SLV1_REG	R/W	I2C_SLV1_REG[7:0]							
2A	42	I2C_SLV1_CTRL	R/W	I2C_SLV1_EN	I2C_SLV1_BYTE_SW	I2C_SLV1_REG_DIS	I2C_SLV1_GRP	I2C_SLV1_LENG[3:0]			
2B	43	I2C_SLV2_ADDR	R/W	I2C_SLV2_RNW	I2C_ID_2 [6:0]						
2C	44	I2C_SLV2_REG	R/W	I2C_SLV2_REG[7:0]							
2D	45	I2C_SLV2_CTRL	R/W	I2C_SLV2_EN	I2C_SLV2_BYTE_SW	I2C_SLV2_REG_DIS	I2C_SLV2_GRP	I2C_SLV2_LENG[3:0]			
2E	46	I2C_SLV3_ADDR	R/W	I2C_SLV3_RNW	I2C_ID_3 [6:0]						
2F	47	I2C_SLV3_REG	R/W	I2C_SLV3_REG[7:0]							
30	48	I2C_SLV3_CTRL	R/W	I2C_SLV3_EN	I2C_SLV3_BYTE_SW	I2C_SLV3_REG_DIS	I2C_SLV3_GRP	I2C_SLV3_LENG [3:0]			
31	49	I2C_SLV4_ADDR	R/W	I2C_SLV4_RNW	I2C_ID_4 [6:0]						
32	50	I2C_SLV4_REG	R/W	I2C_SLV4_REG[7:0]							
33	51	I2C_SLV4_DO	R/W	I2C_SLV4_DO[7:0]							
34	52	I2C_SLV4_CTRL	R/W	I2C_SLV4_EN	SLV4_DONE_INT_EN	I2C_SLV4_REG_DIS	I2C_MST_DLY[4:0]				

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35	53	I2C_SLV4_DI	R	I2C_SLV4_DI[7:0]							
36	54	I2C_MST_STATUS	R	PASS_ THROUGH	I2C_SLV4 _DONE	I2C_LOST _ARB	I2C_SLV4 _NACK	I2C_SLV3 _NACK	I2C_SLV2 _NACK	I2C_SLV1 _NACK	I2C_SLV0 _NACK
37	55	INT_PIN_CFG	R/W	ACTL	OPEN	LATCH _INT_EN	INT_ANYR D _2CLEAR	ACTL_FSY NC	FSYNC _INT_MOD E_EN	BYPASS _EN	-
38	56	INT_ENABLE	R/W	-	WOM_EN	-	FIFO _OFLOW _EN	FSYNC_INT _EN	-	-	RAW_RDY_ EN
3A	58	INT_STATUS	R	-	WOM_INT	-	FIFO _OFLOW _INT	FSYNC _INT	-	-	RAW_DATA _RDY_INT
3B	59	ACCEL_XOUT_H	R	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	R	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	R	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	R	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	R	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	R	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	R	TEMP_OUT_H[15:8]							
42	66	TEMP_OUT_L	R	TEMP_OUT_L[7:0]							
43	67	GYRO_XOUT_H	R	GYRO_XOUT_H[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT_L[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT_H[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT_L[7:0]							
47	71	GYRO_ZOUT_H	R	GYRO_ZOUT_H[15:8]							
48	72	GYRO_ZOUT_L	R	GYRO_ZOUT_L[7:0]							
49	73	EXT_SENS_DATA_00	R	EXT_SENS_DATA_00[7:0]							
4A	74	EXT_SENS_DATA_01	R	EXT_SENS_DATA_01[7:0]							
4B	75	EXT_SENS_DATA_02	R	EXT_SENS_DATA_02[7:0]							
4C	76	EXT_SENS_DATA_03	R	EXT_SENS_DATA_03[7:0]							
4D	77	EXT_SENS_DATA_04	R	EXT_SENS_DATA_04[7:0]							
4E	78	EXT_SENS_DATA_05	R	EXT_SENS_DATA_05[7:0]							
4F	79	EXT_SENS_DATA_06	R	EXT_SENS_DATA_06[7:0]							
50	80	EXT_SENS_DATA_07	R	EXT_SENS_DATA_07[7:0]							
51	81	EXT_SENS_DATA_08	R	EXT_SENS_DATA_08[7:0]							
52	82	EXT_SENS_DATA_09	R	EXT_SENS_DATA_09[7:0]							
53	83	EXT_SENS_DATA_10	R	EXT_SENS_DATA_10[7:0]							
54	84	EXT_SENS_DATA_11	R	EXT_SENS_DATA_11[7:0]							
55	85	EXT_SENS_DATA_12	R	EXT_SENS_DATA_12[7:0]							
56	86	EXT_SENS_DATA_13	R	EXT_SENS_DATA_13[7:0]							
57	87	EXT_SENS_DATA_14	R	EXT_SENS_DATA_14[7:0]							
58	88	EXT_SENS_DATA_15	R	EXT_SENS_DATA_15[7:0]							
59	89	EXT_SENS_DATA_16	R	EXT_SENS_DATA_16[7:0]							
5A	90	EXT_SENS_DATA_17	R	EXT_SENS_DATA_17[7:0]							
5B	91	EXT_SENS_DATA_18	R	EXT_SENS_DATA_18[7:0]							
5C	92	EXT_SENS_DATA_19	R	EXT_SENS_DATA_19[7:0]							
5D	93	EXT_SENS_DATA_20	R	EXT_SENS_DATA_20[7:0]							
5E	94	EXT_SENS_DATA_21	R	EXT_SENS_DATA_21[7:0]							
5F	95	EXT_SENS_DATA_22	R	EXT_SENS_DATA_22[7:0]							
60	96	EXT_SENS_DATA_23	R	EXT_SENS_DATA_23[7:0]							
63	99	I2C_SLV0_DO	R/W	I2C_SLV0_DO[7:0]							
64	100	I2C_SLV1_DO	R/W	I2C_SLV1_DO[7:0]							
65	101	I2C_SLV2_DO	R/W	I2C_SLV2_DO[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66	102	I2C_SLV3_DO	R/W	I2C_SLV3_DO[7:0]							
67	103	I2C_MST_DELAY_CTRL	R/W	DELAY_ES _SHADOW	-	-	I2C_SLV4 _DLY_EN	I2C_SLV3 _DLY_EN	I2C_SLV2 _DLY_EN	I2C_SLV1 _DLY_EN	I2C_SLV0 _DLY_EN
68	104	SIGNAL_PATH_RESET	R/W	-	-	-	-	-	GYRO _RST	ACCEL _RST	TEMP _RST
69	105	MOT_DETECT_CTRL	R/W	ACCEL_INT EL_EN	ACCEL_INT EL_MODE	-		-		-	
6A	106	USER_CTRL	R/W	-	FIFO_EN	I2C_MST _EN	I2C_IF _DIS	-	FIFO _RST	I2C_MST _RST	SIG_COND _RST
6B	107	PWR_MGMT_1	R/W	H_RESET	SLEEP	CYCLE	GYRO_ STANDBY	PD_PTAT	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	R/W	-		DIS_XA	DIS_YA	DIS_ZA	DIS_XG	DIS_YG	DIS_ZG
72	114	FIFO_COUNTH	R/W	-			FIFO_CNT[12:8]				
73	115	FIFO_COUNTL	R/W	FIFO_CNT[7:0]							
74	116	FIFO_R_W	R/W	D[7:0]							
75	117	WHO_AM_I	R	WHOAMI[7:0]							
77	119	XA_OFFSET_H	R/W	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	R/W	XA_OFFS [6:0]							-
7A	122	YA_OFFSET_H	R/W	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	R/W	YA_OFFS [6:0]							-
7D	125	ZA_OFFSET_H	R/W	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	R/W	ZA_OFFS [6:0]							-

Table 1 MPU-9250 mode register map for Gyroscope and Accelerometer

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below.

- Register 107 (0x01) Power Management 1
- Register 117 (0x71) WHO_AM_I

4 Register Descriptions

This section describes the function and contents of each register within the MPU-9250. All the descriptions relate to the default MPU-9250 mode of operation.

4.1 Registers 0 to 2 – Gyroscope Self-Test Registers

Serial IF: R/W

Reset value: 0x00

REGISTER	BITS	FUNCTION
SELF_TEST_X_GYRO	XG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Y_GYRO	YG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Z_GYRO	ZG_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.

For details of the MPU-9250 self-test implementation, please refer to the following document: AN-MPU-9250A-03, MPU-9250 Accelerometer, Gyroscope and Compass Self-Test Implementation.

4.2 Registers 13 to 15 – Accelerometer Self-Test Registers

Serial IF: R/W

Reset value: 0x00

REGISTER	BITS	FUNCTION
SELF_TEST_X_ACCEL	XA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Y_ACCEL	YA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.
SELF_TEST_Z_ACCEL	ZA_ST_DATA[7:0]	The value in this register indicates the self test output generated during manufacturing tests. This value is to be used to check against subsequent self test outputs performed by the end user.

For details of the MPU-9250 self-test implementation, please refer to the following document: AN-MPU-9250A-03, MPU-9250 Accelerometer, Gyroscope and Compass Self-Test Implementation.

4.3 Registers 19 to 24 – Gyro Offset Registers

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	High byte, Low byte in USR register (14h) **OffsetLSB=** X_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** X_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	X_OFFS_USR[7:0]	Low byte, High byte in USR register (13h)
[7:0]	Y_OFFS_USR[15:8]	High byte, Low byte in USR register (16h) **OffsetLSB=** Y_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** Y_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	Y_OFFS_USR[7:0]	Low byte, High byte in USR register (15h)
[7:0]	Z_OFFS_USR[15:8]	High byte, Low byte in USR register (18h) **OffsetLSB=** Z_OFFS_USR * 4 / 2^FS_SEL **OffsetDPS=** Z_OFFS_USR * 4 / 2^FS_SEL / Gyro_Sensitivity Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 2^16 LSB / 500dps Max 999.969 dps Min -1000 dps Step 0.0305 dps
[7:0]	Z_OFFS_USR[7:0]	Low byte, High byte in USR register (17h)

These registers are used to remove DC bias from the gyro sensor data output for X, Y and Z axes. The values in these registers are subtracted from the gyro sensor values before going into the sensor registers. Please refer to registers 67 to 72 for units.

4.4 Register 25 – Sample Rate Divider

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. NOTE: This register is only effective when Fchoice = 2'b11 (fchoice_b register bits are 2'b00), and (0 < dlpf_cfg < 7), such that the average filter's output is selected (see chart below). This is the update rate of sensor register. **SAMPLE_RATE=** Internal_Sample_Rate / (1 + SMPLRT_DIV)

Data should be sampled at or above sample rate; SMPLRT_DIV is only used for1kHz internal sampling.

4.5 Register 26 – Configuration

BIT	NAME	FUNCTION
[7]	-	Reserved
[6]	FIFO_MODE	When set to '1', when the fifo is full, additional writes will not be written to fifo. When set to '0', when the fifo is full, additional writes will be written to the fifo, replacing the oldest data.

<table>
<tr><td>[5:3]</td><td>EXT_SYNC_SET[2:0]</td><td>Enables the FSYNC pin data to be sampled.

<table><tr><th>EXT_SYNC_SET</th><th>FSYNC bit location</th></tr><tr><td>0</td><td>function disabled</td></tr><tr><td>1</td><td>TEMP_OUT_L[0]</td></tr><tr><td>2</td><td>GYRO_XOUT_L[0]</td></tr><tr><td>3</td><td>GYRO_YOUT_L[0]</td></tr><tr><td>4</td><td>GYRO_ZOUT_L[0]</td></tr><tr><td>5</td><td>ACCEL_XOUT_L[0]</td></tr><tr><td>6</td><td>ACCEL_YOUT_L[0]</td></tr><tr><td>7</td><td>ACCEL_ZOUT_L[0]</td></tr></table>Fsync will be latched to capture short strobes. This will be done such that if Fsync toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe. This is a requirement for working with some 3rd party devices that have fsync strobes shorter than our sample rate.</td></tr>
<tr><td>[2:0]</td><td>DLPF_CFG[2:0]</td><td>For the DLPF to be used, fchoice[1:0] must be set to 2'b11, fchoice_b[1:0] is 2'b00.

See table 3 below.</td></tr>
</table>

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below. Note that FCHOICE mentioned in the table below is the inverted value of *FCHOICE_B* (e.g. FCHOICE=2b'00 is same as FCHOICE_B=2b'11).

FCHOICE		DLPF_CFG	Gyroscope			Temperature Sensor	
<1>	<0>		Bandwidth (Hz)	Delay (ms)	Fs (kHz)	Bandwidth (Hz)	Delay (ms)
x	0	x	8800	0.064	32	4000	0.04
0	1	x	3600	0.11	32	4000	0.04
1	1	0	250	0.97	8	4000	0.04
1	1	1	184	2.9	1	188	1.9
1	1	2	92	3.9	1	98	2.8
1	1	3	41	5.9	1	42	4.8
1	1	4	20	9.9	1	20	8.3
1	1	5	10	17.85	1	10	13.4
1	1	6	5	33.48	1	5	18.6
1	1	7	3600	0.17	8	4000	0.04

4.6 Register 27 – Gyroscope Configuration

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	XGYRO_Cten	X Gyro self-test
[6]	YGYRO_Cten	Y Gyro self-test
[5]	ZGYRO_Cten	Z Gyro self-test
[4:3]	GYRO_FS_SEL[1:0]	Gyro Full Scale Select: 00 = +250dps 01= +500 dps 10 = +1000 dps 11 = +2000 dps
[2]	-	Reserved
[1:0]	Fchoice_b[1:0]	Used to bypass DLPF as shown in table 1 above. NOTE: Register is Fchoice_b (inverted version of Fchoice), table 1 uses Fchoice (which is the inverted version of this register).

4.7 Register 28 – Accelerometer Configuration

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	ax_st_en	X Accel self-test
[6]	ay_st_en	Y Accel self-test
[5]	az_st_en	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	-	Reserved

4.8 Register 29 – Accelerometer Configuration 2

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:6]	Reserved	
[5:4]	Reserved	
[3]	accel_fchoice_b	Used to bypass DLPF as shown in table 2 below. NOTE: This register contains accel_fchoice_b (the inverted version of accel_fchoice as described in the table below).
[2:0]	A_DLPFCFG	Accelerometer low pass filter setting as shown in table 2 below.

Accelerometer Data Rates and Bandwidths (Normal Mode)

ACCEL_FCHOICE	A_DLPF_CFG	Output				
		3dB BW (Hz)	Rate (kHz)	Filter Block	Delay (ms)	Noise Density (µg/rtHz)
0	x	1,046	4	Dec1	0.503	300
1	0	218.1	1	DLPF	1.88	300
1	1	218.1	1	DLPF	1.88	300
1	2	99	1	DLPF	2.88	300
1	3	44.8	1	DLPF	4.88	300
1	4	21.2	1	DLPF	8.87	300
1	5	10.2	1	DLPF	16.83	300
1	6	5.05	1	DLPF	32.48	300
1	7	420	1	Dec2	1.38	300

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the normal mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K

The following table lists the approximate accelerometer filter bandwidths available in the low-power mode of operation.

In the low-power mode of operation, the accelerometer is duty-cycled. Fchoice=0 for all options.

Accelerometer Data Rates and Bandwidths (Low-Power Mode)

ACCEL_FCHOICE	ODR (Hz)	Output	
		Bandwidth (Hz)	Delay (ms)

0	0.24	1.1 k	1
0	0.49	1.1 k	1
0	0.98	1.1 k	1
0	1.95	1.1 k	1
0	3.91	1.1 k	1
0	7.81	1.1 k	1
0	15.63	1.1 k	1
0	31.25	1.1 k	1
0	62.50	1.1 k	1
0	125	1.1 k	1
0	250	1.1 k	1
0	500	1.1 kHz	1

As you can see from the tables above, some of the ODRs can be configured in the normal accelerometer mode as well as low power mode.

For further details on how to configure the individual ODRs, please refer to register 30 Low Power Accelerometer ODR Control.

4.9 Register 30 – Low Power Accelerometer ODR Control

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:4]	Reserved	

[3:0]	lposc_clksel[3:0]	Sets the frequency of waking up the chip to take a sample of accel data – the low power accel Output Data Rate.

Lposc_clksel	Output Frequency (Hz)
0	0.24
1	0.49
2	0.98
3	1.95
4	3.91
5	7.81
6	15.63
7	31.25
8	62.50
9	125
10	250
11	500
12-15	RESERVED

4.10 Register 31 – Wake-on Motion Threshold

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	WOM_Threshold	This register holds the threshold value for the Wake on Motion Interrupt for accel x/y/z axes. LSB = 4mg. Range is 0mg to 1020mg.

For more details on how to configure the Wake-on-Motion interrupt, please refer to section 5 in the MPU-9250 Product Specification document.

4.11 Register 35 – FIFO Enable

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION

BIT	NAME	FUNCTION
[7]	TEMP_OUT	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[6]	GYRO_XOUT	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[5]	GYRO_YOUT	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled NOTE: Enabling any one of the bits corresponding to the Gyros or Temp data paths, data is buffered into the FIFO even though that data path is not enabled.
[4]	GYRO_ZOUT	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[3]	ACCEL	1 – write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate; 0 – function is disabled
[2]	SLV_2	1 – write EXT_SENS_DATA registers associated to SLV_2 (as determined by I2C_SLV0_CTRL, I2C_SLV1_CTRL, and I2C_SL20_CTRL) to the FIFO at the sample rate; 0 – function is disabled
[1]	SLV_1	1 – write EXT_SENS_DATA registers associated to SLV_1 (as determined by I2C_SLV0_CTRL and I2C_SLV1_CTRL) to the FIFO at the sample rate; 0 – function is disabled
[0]	SLV_0	1 – write EXT_SENS_DATA registers associated to SLV_0 (as determined by I2C_SLV0_CTRL) to the FIFO at the sample rate; 0 – function is disabled NOTE: See I2C_SLV3_CTRL register to enable this feature for SLV_3

Note: For further information regarding the association of EXT_SENS_DATA registers to particular slave devices, please refer to Registers 73 to 96.

4.12 Register 36 – I2C Master Control

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	MULT_MST_EN	Enables multi-master capability. When disabled, clocking to the I2C_MST_IF can be disabled when not in use and the logic to detect lost arbitration is disabled.
[6]	WAIT_FOR_ES	Delays the data ready interrupt until external sensor data is loaded. If I2C_MST_IF is disabled, the interrupt will still occur.
[5]	SLV_3_FIFO_EN	1 – write EXT_SENS_DATA registers associated to SLV_3 (as determined by I2C_SLV0_CTRL and I2C_SLV1_CTRL and I2C_SLV2_CTRL) to the FIFO at the sample rate; 0 – function is disabled
[4]	I2C_MST_P_NSR	This bit controls the I2C Master's transition from one slave read to the next slave read. If 0, there is a restart between reads. If 1, there is a stop between reads.
[3:0]	I2C_MST_CLK [3:0]	*I2C_MST_CLK* is a 4 bit unsigned value which configures a divider on the MPU-9250 internal 8MHz clock. It sets the I^2C master clock speed according to the following table:

I2C_MST_CLK	I^2C Master Clock Speed	8MHz Clock Divider
0	348 kHz	23
1	333 kHz	24
2	320 kHz	25
3	308 kHz	26
4	296 kHz	27
5	286 kHz	28
6	276 kHz	29
7	267 kHz	30
8	258 kHz	31
9	500 kHz	16
10	471 kHz	17
11	444 kHz	18
12	421 kHz	19
13	400 kHz	20
14	381 kHz	21
15	364 kHz	22

Note: For further information regarding the association of EXT_SENS_DATA registers to particular slave devices, please refer to Registers 73 to 96.

4.13 Registers 37 to 39 – I²C Slave 0 Control

Register 37 - I2C_SLV0_ADDR

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV0_RNW	1 – Transfer is a read 0 – Transfer is a write
[6:0]	I2C_ID_0[6:0]	Physical address of I2C slave 0

Register 38 - I2C_SLV0_REG

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	I2C_SLV0_REG[7:0]	I2C slave 0 register address from where to begin data transfer

Register 39 - I2C_SLV0_CTRL

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV0_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I2C slave 0. 0 – function is disabled for this slave

BIT	NAME	FUNCTION
[6]	I2C_SLV0_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV0_REG[0] = 1, or if the last byte read has a register address lsb = 0. For example, if I2C_SLV0_REG = 0x1, and I2C_SLV0_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00, 2) the second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03 0 – no swapping occurs, bytes are written in order read.
[5]	I2C_SLV0_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
[4]	I2C_SLV0_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
[3:0]	I2C_SLV0_LENG[3:0]	Number of bytes to be read from I2C slave 0

4.14 Registers 40 to 42 – I^2C Slave 1 Control

Register 40 - I2C_SLV1_ADDR

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV1_RNW	1 – Transfer is a read 0 – Transfer is a write
[6:0]	I2C_ID_1[6:0]	Physical address of I2C slave 1

Register 41 - I2C_SLV1_REG

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	I2C_SLV1_REG[7:0]	I2C slave 1 register address from where to begin data transfer

Register 42 - I2C_SLV1_CTRL

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV1_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV1_EN and I2C_SLV1_LENG. 0 – function is disabled for this slave

BIT	NAME	FUNCTION
[6]	I2C_SLV1_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV1_REG[0] = 1, or if the last byte read has a register address lsb = 0. For example, if I2C_SLV1_EN = 0x1, and I2C_SLV1_LENG = 0x3 (to show swap has to do with I2C slave address not EXT_SENS_DATA address), and if I2C_SLV1_REG = 0x1, and I2C_SLV1_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_03 (slave 0's data will be in EXT_SENS_DATA_00, EXT_SENS_DATA_01, and EXT_SENS_DATA_02), 2) the second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_04, and the data read from address 0x3 will be stored at EXT_SENS_DATA_05, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_06 0 – no swapping occurs, bytes are written in order read.
[5]	I2C_SLV1_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
[4]	I2C_SLV1_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
[3:0]	I2C_SLV1_LENG[3:0]	Number of bytes to be read from I2C slave 1

4.15 Registers 43 to 45 – I²C Slave 2 Control

Register 43 - I2C_SLV2_ADDR

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV2_RNW	1 – Transfer is a read 0 – Transfer is a write
[6:0]	I2C_ID_2[6:0]	Physical address of I2C slave 2

Register 44 - I2C_SLV2_REG

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	I2C_SLV2_REG[7:0]	I2C slave 2 register address from where to begin data transfer

Register 45 - I2C_SLV2_CTRL

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV2_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN, I2C_SLV0_LENG, I2C_SLV1_EN and I2C_SLV1_LENG. 0 – function is disabled for this slave
[6]	I2C_SLV2_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV2_REG[0] = 1, or if the last byte read has a register address lsb = 0. See I2C_SLV1_CTRL for an example. 0 – no swapping occurs, bytes are written in order read.
[5]	I2C_SLV2_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data

BIT	NAME	FUNCTION
[4]	I2C_SLV2_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
[3:0]	I2C_SLV2_LENG[3:0]	Number of bytes to be read from I2C slave 2

4.16 Registers 46 to 48 – I^2C Slave 3 Control

Register 46 - I2C_SLV3_ADDR

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7]	I2C_SLV3_RNW	1 – Transfer is a read 0 – Transfer is a write
[6:0]	I2C_ID_3[6:0]	Physical address of I2C slave 3

Register 47 - I2C_SLV3_REG

Serial IF: R/W

Reset value: 0x00

BIT	NAME	FUNCTION
[7:0]	I2C_SLV3_REG[7:0]	I2C slave 3 register address from where to begin data transfer

Register 48 - I2C_SLV3_CTRL

Serial IF: R/W

Reset value: 0x00