Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

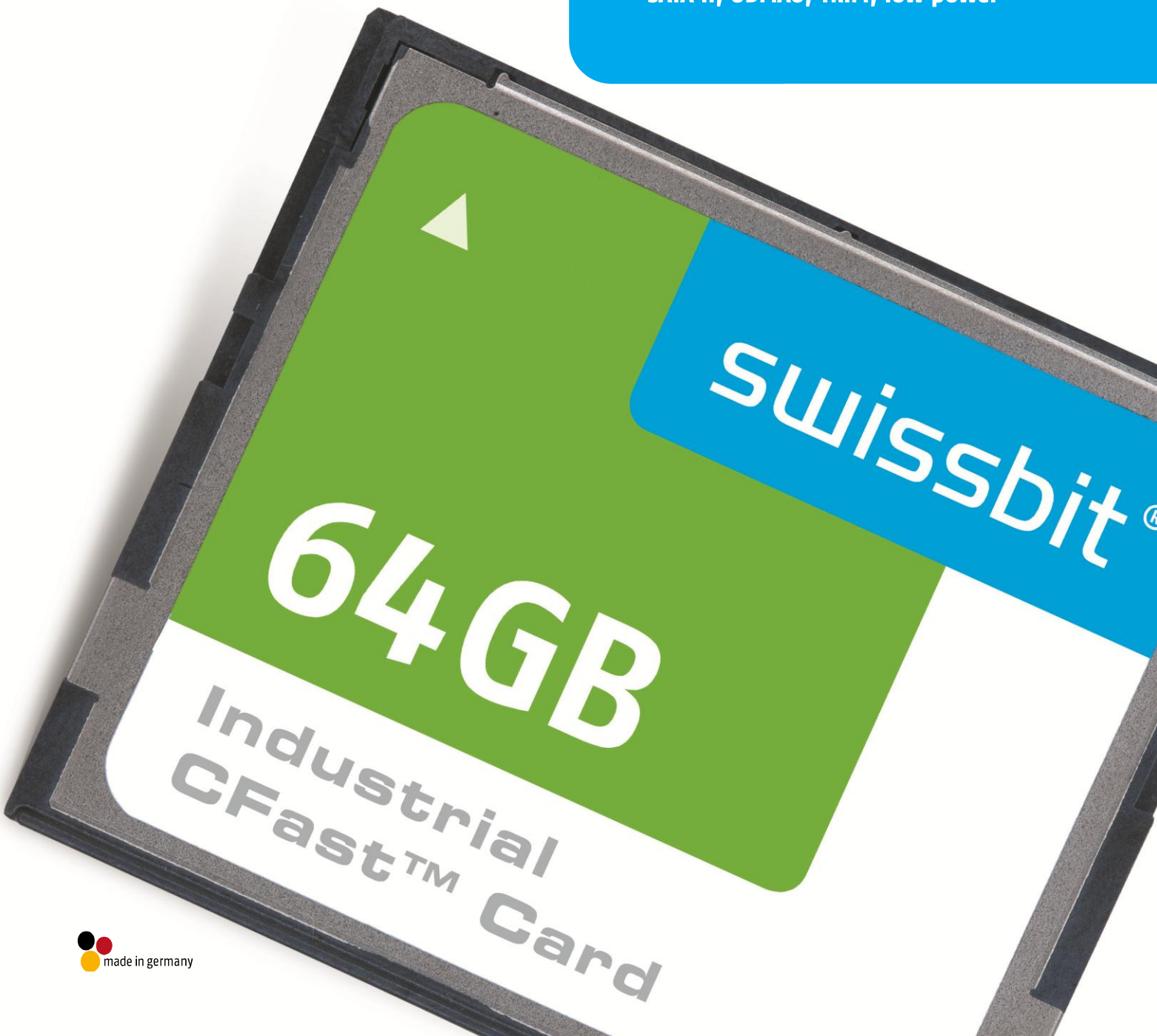
swissbit®

Product Data Sheet

Industrial CFast™ Card

F-240 Series

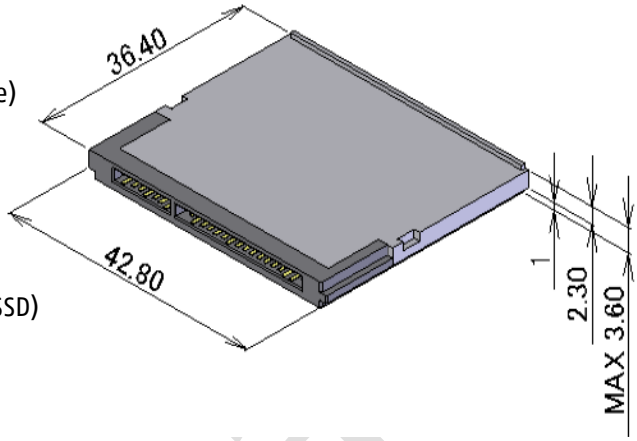
SATA II, UDMA6, TRIM, low power



made in germany

F-240 Series – Industrial CFast™ Card with SATA interface

1 Features



- Highly-integrated memory controller
  - SATA Rev 2.6 – 3Gbit/s (1.5Gbit/s compatible)
  - max. UDMA6 MDMA2, PIO4, supported
  - Hardware BCH-code ECC (24bit correction per double sector or 6bit per sector)
  - Fix drive configuration
- Small form factor:
  - CompactFlash card sized Solid State Drive (SSD) with SATA interface
  - 42.8mm x 36.4mm x 3.3mm (max. 3.6mm)
- 7+17 pin (SATA+power) CFast connector
- 3.3V ± 5% power supply
- Very low Power, typical 250mA in transfer operation (CFAST Power level 0)
- CFast PHYSLP supported (<20 mA)
- Activity and SATAlink LED output at LED1 and LED2 pin
- write protect at connector I01 pin
- Special features
  - S.M.A.R.T. support with additional vendor information, interpretation with Swissbit life time monitoring tool
  - TRIM command
  - NCQ queue depth 32
  - HPA (Host protected area)
  - Security mode feature set
  - LBA48 command set
  - host initiated power management requests
  - write protection with vendor command
- Wear Leveling: active wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Read disturb management (refresh data when flash often read)
- High reliability
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF > 2,500,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of connector insertions/removals: >10,000
- High performance
  - Up to 300MB/s burst transfer rate in SATA II – 3.0Gb/sec
  - Sustained Write performance: up to 100MB/s (4channel)
  - Sustained Read Performance: up to 130MB/s (4channel)
- Available densities
  - 2GByte up to 64GByte (SLC NAND Flash)
- 2 Temperature ranges
  - Commercial Temperature range 0 ... +70°C
  - Industrial Temperature range -40 ... +85°C
- Life Cycle Management
- Controlled BOM
- RoHS compatible

2 Table of Contents

3 Order Information

3.1 Available Standard part numbers

FIX / SATA II/ UDMA6, MDMA2, PIO4

Density	Part Number
F-240 Series CFast Card	
2GB	SFCA2048HgBV4TO-t-MS-2y6-STD
4GB	SFCA4096HgBV4TO-t-MS-2y6-STD
8GB	SFCA8192HgBV4TO-t-DT-2y6-STD
16GB	SFCA16GBHgBV4TO-t-QT-2y6-STD
32GB	SFCA32GBHgBV4TO-t-NC-2y6-STD
64GB	SFCA64GBHgBV4TO-t-NC-2y6-STD

Table 1: Standard temperature product list

g= depends on product generation (currently g=2)
t= Temperature "C" commercial (0°c – +70°C) "I" industrial (-40°C – +85°C)
y= depends on firmware generation

3.2 Offered OEM options

- Customer specified drive size and drive geometry (C/H/S – cylinder/head/sector)
- Customer specified drive ID (Strings)
- Preload service (also drive images with any file system)
- ...

4 Product Specification

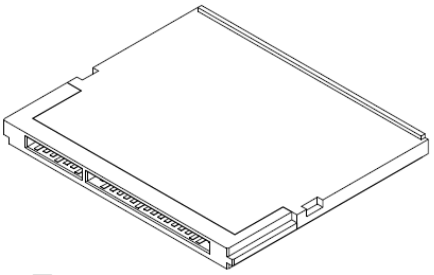
The CFAST™ card is a small form factor non-volatile memory drive which provides high capacity data storage. It has a standard CFAST connector with SATA and power/control part. The card works at a supply voltage of 3.3V.
The drive with the SATA interface operates in Mode 2.0 (1.5 or 3.0 Gb/s burst).
With an adapter (e.g. Swissbit CFAST Adapter) the drive behaves as a standard SATA disk drive.
The adapter can be mounted in Swissbit 2.5'' SSD housing.
The drive has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware BCH-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to detect and correct **24random bits per double sector or 6 random bits per sector (depending on the flash type)**.
The drive has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The specification has been realized and approved by the ATA/ATAPI-8 specification.
The system highlights are shown in Table 2 ...Table 9.

Related Documentation

- CFAST specification 1.1 (www.compactflash.org)
- Serial ATA International Organization: Serial ATA Revision 2.6 (www.serialata.org)
- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8 to ATA/ATAPI-5) (www.t13.org)
- Electronic Industries Alliance (www.eia.org)

4.1 Physical description

The CFAST™ card contains a flash controller and Flash memory modules. The controller interfaces with a host system allowing data to be written to and read from the Flash memory modules.
The CFAST™ card is offered in a Compact Flash size package with a standard CFAST connector with a 7-pin SATA connector and a 17-pin power and control connector with 15 pins. Figure 6 and Figure 7 show CFAST™ card dimensions and connector location.



4.2 System Performance

Table 2: System Performance

System Performance		Typ.	Max.	Unit
Data transfer Rate (SATA burst (1.5 or 3.0Gb/s))		150 or 300	300	MB/s
Sustained Sequential Read 128kB Block size [1]	2GB	94	preliminary	MB/s
	4...16GB	108	preliminary	
	32...64GB	TBD	preliminary	
Sustained Sequential Write 128kB Block size [1]	2GB	37	preliminary	
	4...16GB	46	preliminary	
	32...64GB	TBD	preliminary	
Sustained Sequential Read 4kB Block size [1]	2GB	33	preliminary	MB/s
	4...16GB	33	preliminary	
	32...64GB	TBD	preliminary	
Sustained Sequential Write 4kB Block size [1]	2GB	9	preliminary	
	4...16GB	3.7	preliminary	
	32...64GB	TBD	preliminary	
Sustained Random Read 4kB Block size [1]	2GB	9	preliminary	MB/s
	4...16GB	7.6	preliminary	
	32...64GB	6.4	preliminary	
Sustained Random Write 4kB Block size [1] [2]	2GB	0.16	preliminary	MB/s
	4...16GB	0.13	preliminary	
	32...64GB	0.10	preliminary	
Trimmed Random Write [1] [2] 4kB Block size	2GB	0.76	preliminary	MB/s
	4...16GB	0.63	preliminary	
	32...64GB	TBD	preliminary	

1. All values refer to Toshiba Flash chips in UDMA5 mode (SATA 3.0Gbit/s) with Sequential write/read test (256 sectors multiple commands) and sequential and random write/read test (8 sectors multiple commands).Sustained Speed depends on flash type and number, file/cluster size, and burst speed.
2. The typical random write speed values are really random access across the whole drive. Random write speed values in file systems are much larger.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage	3.3V ±10%

Table 4: Current consumption (1)

Current Consumption (type)	3.3V	Unit
Read (typ/max)	170/200	mA
Write (typ/max)	180/200	
Idle Mode (typ/max)	85/100	
PHYSLP mode	<20	

1. All values are typical at 25° C and nominal supply voltage and refer to 8GByte CFAST card at SATA II interface.

4.3.2 Recommended Storage Conditions

Table 5: Recommended Storage Conditions

Parameter	Value
Storage Temperature	-50°C to 100°C

4.3.3 Shock, Vibration, and Humidity

Table 6: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20G Peak, 10...2000Hz
Shock	1500G, 0.5ms duration, half sine wave

4.4 Physical Dimensions

Table 7: Physical Dimensions

Physical Dimensions		Unit
Length	36.4±0.1	mm
Width	42.8±0.1	
Thickness	3.6±0.1	
Weight (typ.)	10	g

4.5 Reliability

Table 8: System Reliability and Maintenance (1)

Parameter	Value
MTBF (at 25°C)	> 2,500,000 hours
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read
Data Retention	10 year (JESD47)

1. Dependent on final system qualification data.

4.6 Drive geometry / CHS parameter

Table 9: CFAST card capacity specification

Capacity	Default_cylinders	Default_heads	Default_sectors _track	Sectors_drive	Total addressable capacity (Byte)
F-240 Series					
2GB	3,970	16	63	4,001,760	2,048,901,120
4GB	7,732	16	63	7,793,856	3,990,454,272
8GB	15,498	16	63	15,621,984	7,998,455,808
16GB	16,383*)	16	63	31,277,056	16,013,852,672
32GB	16,383*)	16	63	62,586,880	32,044,482,560
64GB	16,383*)	16	63	125,304,832	64,156,073,984

*) The CHS access is limited to about 8GB. Above 8GB the drive must be addressed in LBA mode.

5 Electrical interface

5.1 Electrical description

The CFAST CARD is connected with a standard 7 pin SATA connector and a standard 15 pin SATA power connector.

The signal/pin assignments and descriptions are listed in Table 10.

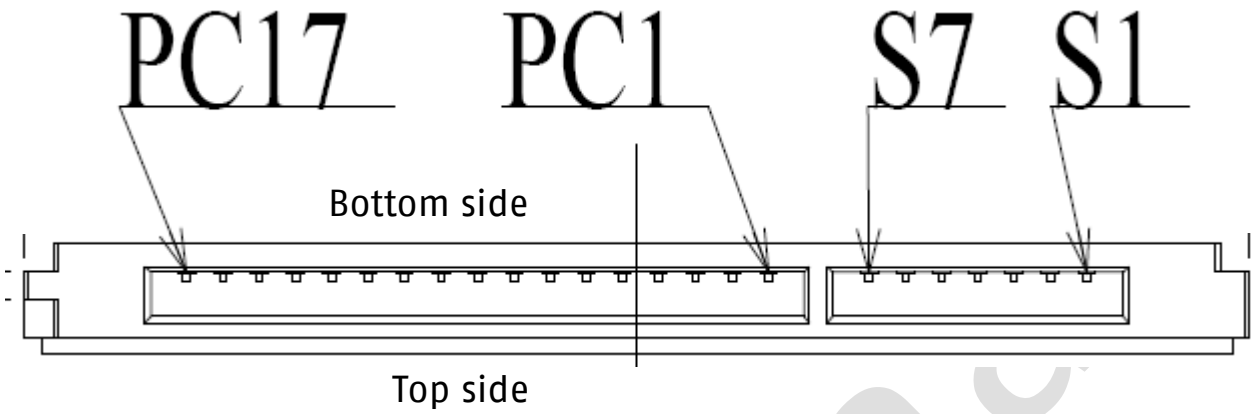


Table 10: Pin Assignment, name, and description

Pin	Signal Name	Description
S1	SGround	Signal Ground
S2	A+	+ Differential Device Receive signal
S3	A-	- Differential Device Receive signal
S4	SGround	Signal Ground
S5	B-	- Differential Device Transmit signal
S6	B+	+ Differential Device Transmit signal
S7	SGround	Signal Ground
PC1	CDI *)	Card detect in
PC2	Ground	Power Ground
PC3...PC6	TBD	not used
PC7	Ground	Power Ground
PC8	LED1	LED output for device activity (driven low)
PC9	LED2	LED output for SATA link indication (driven low)
PC10	IO1 WP	Write protect input (low active)
PC11...PC12	IO2...3	not used
PC13...PC14	3.3V	Device power 3.3V
PC15...PC16	Ground	Power Ground
PC17	CDO *)	Card detect out

*) CDI This pin is connected to CDO and to the card controller.
If CDI is not driven by the host, it should be connected to GND (see section 5.4)
It can be used for PHYSLP functionality (see section 5.4)

5.2 Electrical Specification

Table 11 and Table 12 define the DC Characteristics of the CFAST card. Unless otherwise stated, conditions are:

- Vcc = 3.3V ± 5%
- 0°C to +70°C

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 12.

Table 11: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 3.6V

Table 12: Input Power write and read

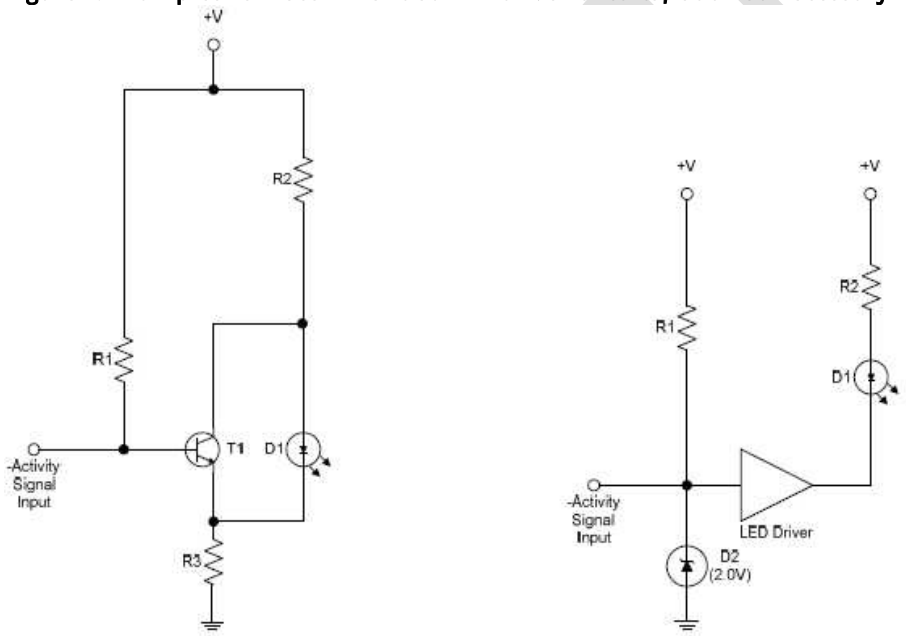
Mode	Maximum Average RMS Current	Conditions
SATA II	250mA	-40... +85 °C
SATA I	220mA	

5.3 LED and IO-pins

LED1 is the DASP signal and is held low for every command and is not driven in idle mode.
LED2 is the SATA link indicator and is driven low, if the SATA is connected and active.

LED1 and LED2 pin is driven low and only pulled up weakly. So this pin can be tied low by the host without accidental current through these pins. The LED pins can be used to display the function of the card.
The LED1 and LED2 pins could drive up to 10mA directly for an LED with serial resistance to 3.3V. It is recommended to use an LED driver circuit.

Figure 1: Examples for recommended LED driver circuits, but not necessary



IO1 pin is the write protect pin.
If this pin tied low, the card is write protected and rejects all write commands.

5.4 Card detection and PHYSLP functions with CDI and CDO pin

5.4.1 General

The CFast card connector contains two signals, CDI and CDO. These signals enable two functions:

a. Card Detect. This function enables the host to detect when the card is fully inserted. For example, the host may wish to power up the card only after it is inserted, or turn on an LED when the card is properly inserted.
b. PHYSLP. This function is a CFast power management protocol which may be invoked when the SATA connection is in Slumber mode. Please see the CFast specifications for a complete description. The purpose of this function is to enable the device to turn off the SATA PHY completely, saving power. The host may turn off its own PHY when invoking this function.

Swissbit F-2x0 support Card detect and PHYSLP functionality
This section explains recommended methods for the host to interface with the card so that the card will not be damaged, and to ensure compatibility between the card and the host regarding the above described functions.

5.4.2 Connection when the host uses the Card Detect functionality only

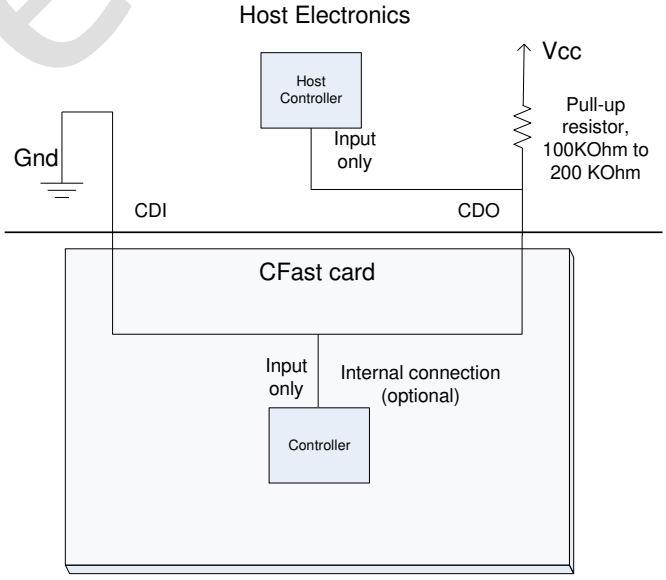
The host needs to take into account the following restrictions:

a. CDI and CDO are shorted together on the CFast card.
b. The card may not have Vcc connected directly to CDI or to CDO.
(The newest F-2x0 cards have a serial resistor between CDI and controller)
c. The CDI – CDO signal on the F-2x0 card is connected to a card controller input pin.
d. The card doesn't actively drive the CDI or CDO signals.

Based on the above, the following is recommended:

a. CDI will be connected to Gnd.
b. CDO will be connected to an input port on the host controller.
c. CDO will be connected to a pull-up resistor on the host. The value of the resistor is calculated so that the voltage drop across the resistor when the card CDO is connected and CDI is not connected will not exceed 0.4V. The leakage current of the card controller is up to 1µA. As an example, if the host controller leakage is also 1µA, the pull-up resistor may have a value of up to 200KΩ . It is recommended that the pull-up resistor value will be as high as possible in order to have no effect on the card controller and to conserve power.

See Figure 2
Figure 2: CFast connection for Card Detect functionality only



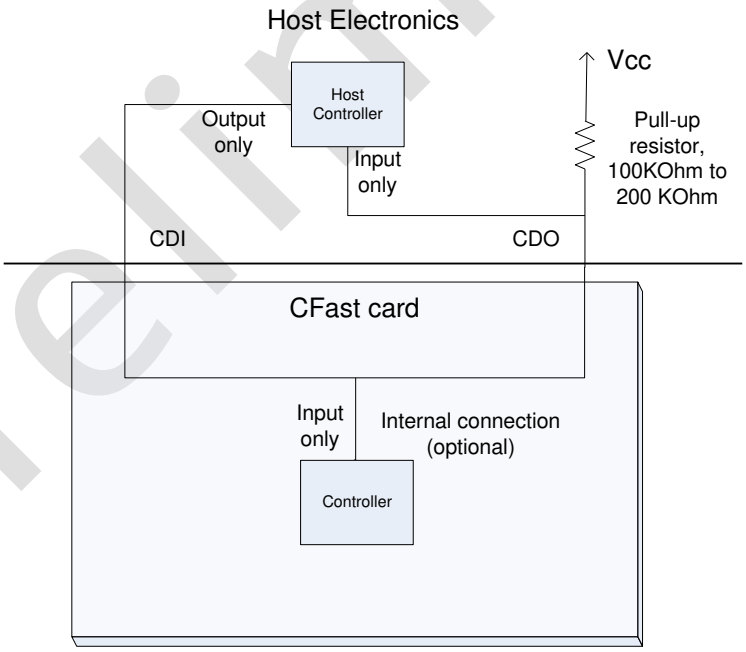
5.4.3 Connection when the card uses the Card Detect functionality and the PHYSLP functionality

The circuit is modified when PHYSLP is intended to be used. CDI is connected to an active LVCMOS level output port on the host controller.
The same restrictions as in the previous section apply.
Based on the above, the following is recommended:

a. CDI will be connected to a host controller output port.
b. CDO will be connected to an input port on the host controller.
c. CDO will be connected to a pull-up resistor on the host. The value of the resistor is calculated so that the voltage drop across the resistor when the card CDO is connected and CDI is not connected will not exceed 0.4V. The leakage current of the card controller is up to 1µA. As an example, if the host controller leakage is also 1µA, the pull-up resistor may have a value of up to 200KΩ . It is recommended that the pull-up resistor value will be as high as possible in order to have no effect on the card controller and to conserve power.
d. During normal operation CDI will, by default, be driven by the host controller to a logic LOW level. This enables Card Detect functionality, the same as in section 5.4.2 .
   When a card supports the PHYSLP functionality, SATA is in Slumber mode, and the host wants to put the card into PHYSLP mode, the host will
   1. Disregard the CDO input port.
   2. Drive CDI to a logic HIGH level
e. In case the Card Detect functionality is required while in the PHYSLP power mode, there is a mechanism described in the CFast specification. This mechanism consists of pulsing CDI to logic LOW for a period of less than 2 milliseconds, and sampling CDO while CDI is at logic LOW. The CFast specification specifies that a CDI pulse going to logic LOW of less than 2 milliseconds will not affect the device PHYSLP state.

See Figure 3.

Figure 3 – CFast connection for Card Detect and PHYSLP functionality



5.5 Power Management

See the SATA specification for more information on SATA PHY power modes.
SATA PHY power modes affect only the SATA PHY, not the device power status. PHYSLP mode can be used by the host to relatively quickly minimize (and restore) PHY power. It may also be used to further reduce CFast device power after the host has sent commands to put the CFast device in a low power device state.
A device's ability to support PHYSLP mode is indicated in Identify Drive Word 161 (CFast Specific Support).

5.5.1 PHYSLP protocol overview

If the host and device support PHYSLP mode the following protocols shall be used to enter and exit PHYSLP mode.

To enter PHYSLP mode the protocol is:

a) The host shall send a request for the card to enter the SATA PHY Slumber mode. See the SATA specification for more information.
b) After the CFast PHY has gone into Slumber power mode, the host shall deassert CDI.
c) The host and the device shall power down their respective PHYs retaining calibration information.
d) After deasserting CDI and entering PHYSLP mode, the host may assert CDI for a period of less than one millisecond to check for device presence.

To exit PHYSLP mode the protocol is:

a) The host shall assert CDI. The CFast card shall not respond to CDI assertions of less than two milliseconds.
b) The host and the device shall power up their respective PHYs into SATA PHY Slumber mode.

The device shall send a SATA COMWAKE signal to begin the SATA defined slumber to PHYRDY sequence (see section "Power-On Sequence State Machine" in the SATA specification).

Figure 4: PHYSLP entry timing diagram

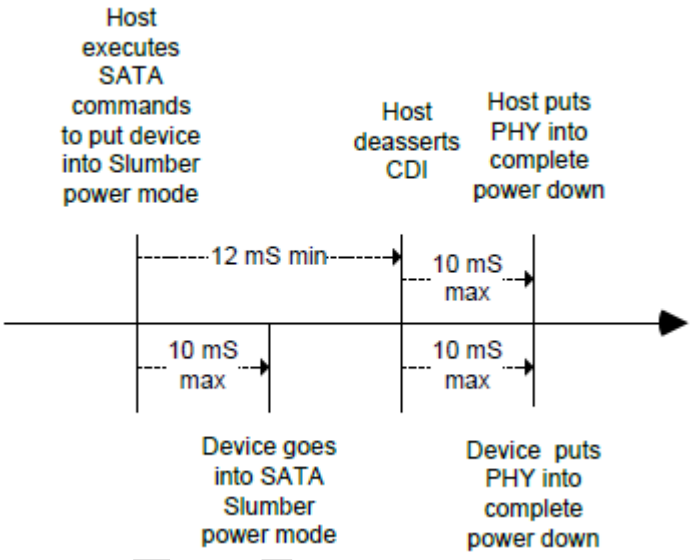
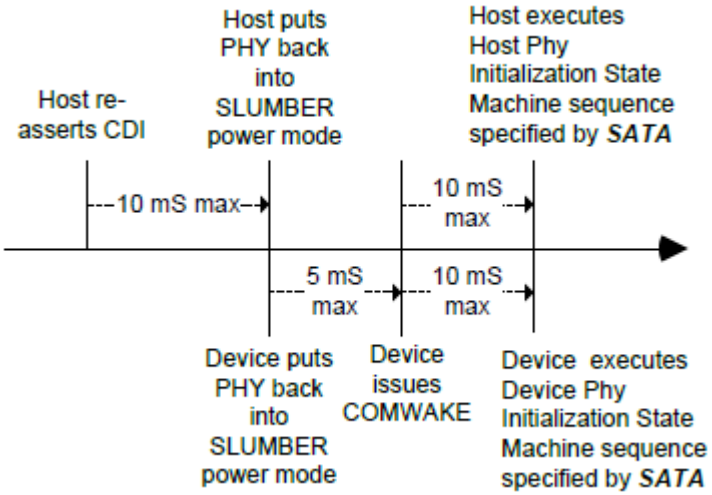


Figure 5: PHYSLP exit timing diagram



6 ATA command description

This section provides information on the ATA commands supported by the CFAST card. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register.

ATA Command Flow

DDMAI0: DMA_in State This state is activated when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command. When in this state, the device shall prepare the data for transfer of a data FIS to the host.

Transition DDMAI0:1 When the device has the data ready to transfer a data FIS, the device shall transition to the DDMAI1: Send_data state. Transition DDMAI0:2 When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.

DDMAI1: Send_data This state is activated when the device has the data ready to transfer a data FIS to the host. When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2,048 Dwords (8KB).

Transition DDMAI1:1 When the data FIS has been transferred, the device shall transition to the DMA0I0: DMA_in state.

DDMAI2: Send_status This state is activated when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data. When in this state, the device shall request that the Transport layer transmit a Register FIS with the register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DDMAI2:1 When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 13 summarizes the Drive command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 13: ATA Command Set (1)

Command	Code	FR(1)	SC(2)	SN(3)	CY(5:4)	DH(6)	LBA(5:3)
Check Power Mode	E5h or 98h					D	
Data Set Management	06h		YY			D	YY
Execute Drive Diagnostic	90h					D	
Flush cache	E7h					D	
Flush cache Ext	EAh					D	
Format track	50h		Y		Y	Y	Y
Identify Drive	ECh					D	
Idle	E3h or 97h		Y			D	
Idle Immediate	E1h or 95h					D	
Media Lock	DEh					D	
Media Unlock	DFh					D	
NOP	00h					D	
Read Buffer	E4h					D	
Read DMA	C8		Y	Y	Y	Y	Y
Read DMA Ext	25h		YY			D	YY
Read FPDMA Queued	60h	Y	Y	Y	Y	D	Y
Read Multiple	C4h		Y	Y	Y	Y	Y
Read Multiple Ext	29h		YY			D	YY
Read native max address	F8h					D	
Read native max address Ext	27h					D	
Read Sector(s)	20h		Y	Y	Y	Y	Y
Read Sector(s) Ext 2)	24h		YY	YY	YY	D	YY
Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h		YY	YY	YY	D	YY
Recalibrate	1Xh					D	
Security Disable Password	F6h					D	
Security Erase Prepare	F3h					D	
Security Erase Unit	F4h					D	
Security Freeze Lock	F5h					D	
Security Set Password	F1h					D	
Security Unlock	F2h					D	
Seek	7Xh			Y	Y	Y	Y
Set Features	EFh	Y				D	
Set max address	F9h		Y	Y	Y	Y	Y
Set max address Ext	37h		YY	YY	YY	D	YY
Set Multiple Mode	C6h		Y			D	
Set Sleep Mode	E6h or 99h					D	
S.M.A.R.T.	B0h	Y	Y		Y	D	
Stand By	E2h or 96h					D	
Stand By Immediate	E0h or 94h					D	
Write Buffer	E8h					D	
Write DMA	CAh or CBh		Y	Y	Y	Y	Y
Write DMA Ext	35h		YY	YY	YY	D	YY
Write FPDMA Queued	61h		Y	Y	Y	D	Y
Write Multiple	C5h		Y	Y	Y	Y	Y
Write Multiple Ext	39h		YY	YY	YY	D	YY
Write Sector(s)	30h		Y	Y	Y	Y	Y
Write Sector(s) Ext	34h		YY	YY	YY	D	YY
Write Verify	3Ch		Y	Y	Y	Y	Y

1. FR = Features Register (1), SC = Sector Count Register (2), SN = Sector Number Register (3), CY = Cylinder Registers (5:4),
   DH = Drive/Head Register (6), LBA = Logical Block Address Mode Supported (see command descriptions for use),
   Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Drive and head parameters are used.
   YY – registers must be written twice for 48bit LBA commands
   D – only the Drive parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).
2. To read out the higher and lower byte of the 16bit registers bit7 of the Device Control Register (write to Alternate status register) must be set to 1 or 0, respectively.

6.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Drive is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Drive is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 14 defines the Byte sequence of the Check Power Mode command.

Table 14: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.2 Data Set Management (06h) TRIM

This 48-bit command is optional for ATA devices. The DATA SETMANAGEMENT command is not part of any feature set.
The DATA SET MANAGEMENT command provides information for device optimization (e.g., file system information).
See Table 15 for the DATA SET MANAGEMENT command inputs.

Table 15: Data Set Management

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	nu	06h							
DRIVE/HEAD	nu	nu	L	nu	Transport dependent	Reserved			
LBA High	Reserved								
LBA Mid	Reserved								
LBA Low	Reserved								
SECTOR COUNT	15:8	7:0 Number of 512-byte blocks to be transferred; the value of zero is reserved.							
FEATURES	Reserved								TRIM

Currently this command is specified only for the TRIM command.
Currently only one 512-byte block can be transferred with one command (see Identify Device word 169).
Detailed information about the TRIM command is available in the ATA/ATAPI Command Set-2 (ACS-2) at www.t13.org

6.3 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Drive.
The Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 16 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 17 are returned in the Error Register at the end of the command.

Table 16: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 17: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error

6.4 Flush Cache (E7h)

This command causes the drive to complete writing data from its cache. The drive returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the drive does not support the Flush Cache command, the drive shall return command aborted.

Table 18: Flush Cache

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E7h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.5 Flush Cache Ext (EAh) 48bit LBA

This command causes the card to complete writing data from its volatile cache into non-volatile memory. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache Ext command, the Compact Flash Storage Card shall return command aborted. See Table 19 for the DATA SET MANAGEMENT command inputs.

Table 19: Flush cache Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	EAh							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	nu	nu							
LBA Mid	nu	nu							
LBA Low	nu	nu							
SECTOR COUNT	nu	nu							
FEATURES	nu	nu							

An unrecoverable error encountered while writing data results in aborting the command and the Command Block registers contain the 48 –bit sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE EXT commands continue the process of flushing the cache starting with the first sector after the sector in error.
This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

6.6 Format track (50h)

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash™ Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash™ Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Table 20: Format track

Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count (LBA only)							
FEATURES	nu							

6.7 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the Drive. This command has the same protocol as the Read Sector(s) command. Table 21 defines the Identify Device command Byte sequence. All reserved bits or Words are zero.
Table 22 shows the definition of each field in the Identify Drive Information.

Table 21: Identify Device

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 22: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	**045Ah***	2	Standard Configuration FIX (optional 848Ah for removable)
1	XXXXh	2	Default number of cylinders (obsolete)
2	0000h	2	Reserved
3	00XXh	2	Default number of heads (obsolete)
4	0000h	2	Obsolete
5	0200h	2	Obsolete
6	XXXXh	2	Default number of sectors per track (obsolete)
7-8	XXXXh	4	Number of sectors per Drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Buffer type (dual ported multi-sector) retired
21	0001h	2	Buffer Size in 512byte increment (obsolete)
22	0004h	2	Reserved
23-26	**YYYY***	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	**YYYY***	40	Model number in ASCII (right justified ("SFCAxxxxHxBVxxx-x-xx-xxx-xxx")
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double word not supported
49	**0Fooh***	2	Capabilities with DMA, LBA, IORDY supported
50	4001h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Obsolete
53	0007h	2	Field validity (Bytes 54-58, 64-70, 88)
54	XXXXh	2	Current numbers of cylinders (obsolete)
55	XXXXh	2	Current numbers of heads (obsolete)
56	XXXXh	2	Current sectors per track (obsolete)
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) (obsolete)
59	**010Xh***	2	Multiple sector setting (can be changed by host).
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Single Word DMA transfer not implemented

Word Address	Default Value	Total Bytes	Data Field Type Information
63	**0X07h*** **0000h***	2	Multi-Word DMA transfer support and selection (can changed by host). no multi-word DMA
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	0078h*	2	Minimum Multi-Word DMA transfer cycle time per Word.
66	0078h*	2	Recommended Multi-Word DMA transfer cycle time.
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69	8000h	2	CFast specification supported
70-74	0000h	10	Reserved
75	**001Fh***	2	Queue depth 32 for NCQ, if supported
76	**0306h*** **0206h***	2	SATA Capabilities (Bit 8 for NCQ)
77	0000h	2	Reserved
78	0000h*	2	SATA Feature support
79	0000h*		SATA Features enabled (can be changed by host)
80-81	01E0h FFFFh	4	ATA version 5 to ATA version 8
82-84	742Bh* 7401h* 4120h*	6	Features/command sets supported
85-87	**7409h*** **B401h*** **4020h***	6	Features/command sets enabled (can change in operation)
88	**XX7F***	2	UDMA Mode Supported 0 to 6 and Selected (changes in operation)
89	0000h*	2	Time for security erase unit completation
90	0000h*	2	Time for enhanced security erase unit completation
91	0000h	2	Reserved
92	**FFFE***	2	Master Password Revision Code
93-99	0000h*	14	Reserved
100-103	XXXXh*	8	Total number of sectors addressable in LBA48 mode
104	0000h	2	Reserved
105	0001h	2	Number of sectors per Data Set management command (TRIM)
106-107	0000h	4	Reserved
108-111	0000h*	8	World Wide Name
112-118	0000h	14	Reserved
119	4000h	2	Command set/feature set supported extension
120	4000h*	2	Command set/feature set enabled extension
121-127	0000h	14	Reserved
128	0009h*	2	Security Status (changes in operation)
129	XX00h*	2	Write Protect Status (Vendor specific)
130-159	XXXXh	60	Vendor specific
160	80FAh*	2	CFA Max. current (e.g. 250mA)
161	8001h*	2	CFast PHYSLP mode supported
162-168	0000h	14	Reserved
169	0001h	2	Trim bit in Data Set Management supported
170-216	0000h	94	Reserved
217	0001h	2	Nominal Media Rotation Rate: Solid State Device
218-221	0000h	8	Reserved
222	101fh	2	Transport major version: Serial transport, SATA rev 2.6
223	FFFFh	2	Transport minor version: not supported
224-254	0000h	62	Reserved
255	XXA5h	2	Integrity word

* Standard values, depending on configuration
XXXX Depending on drive capacity and drive geometry
YYYY Depending on drive configuration

6.7.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **045Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the drive as the root storage device.

6.7.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.7.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.7.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.7.5 Word 7-8: Number of Sectors per Drive

This field contains the number of sectors per Drive. This double Word value is also the first invalid address in LBA translation mode.

6.7.6 Word 10-19: Memory Drive Serial Number

The contents of this field are right justified and padded without spaces (20h).

6.7.7 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.7.8 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.7.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.7.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 11: IORDY Supported
  If bit 11 is set to 1 then this drive supports IORDY operation.
  If bit 11 is set to 0 then this drive may support IORDY operation.
- Bit 10: IORDY may be disabled
  If bit 10 is set to 1 then IODRDY may be disabled.
- Bit 9 LBA support: drive support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

6.7.11 Word 50: Capabilities

- Bit 0 shall be set to one to indicate a vendor specific Standby timer value minimum.

6.7.12 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15:8: are set to 02H.

6.7.13 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid

- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported UDMA

6.7.14 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.7.15 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

6.7.16 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7:0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

6.7.17 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Drive in LBA mode only.

6.7.18 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the drive to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
Selection of Multiword DMA modes 3 and above are specific to Drive are as described in Word 163.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the drive to indicate the Multiword DMA modes it is capable of supporting.
Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the drive supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the drive supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the Drive supports Multiword DMA modes 2, 1 and 0.
Support for Multiword DMA modes 3 and above are specific to Drive are reported in word 163 as described in Word 163.

6.7.19 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the drive to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the Drive supports PIO mode 4.
- Bit 0 is set to '1' to indicate that the Drive supports PIO mode 3.

Support for PIO modes 5 and above are specific to Drive are reported in word 163 as described in Word 163.

6.7.20 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.7.21 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the Drive will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.7.22 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer without utilization of flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.7.23 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the Drive supports while performing data transfers while utilizing IORDY flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the Drive.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.7.24 Word 69: CFast Specification

- Bit 15 is set to '1' to indicate that CFast specification is supported.

6.7.25 Word 75: Queue depth for NCQ

- Bit 15:5 Reserved
- Bit 4:0 Maximum queue depth -1

6.7.26 Word 76: Serial ATA Capabilities

- Bit 15:11 Reserved
- Bit 10 1 = Supports Phy Event Counters
- Bit 9 1 = Supports receipt of host initiated power management requests
- Bit 8 1 = Supports native Command Queuing
- Bit 7:3 Reserved for future SATA signaling speed grades
- Bit 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
- Bit 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
- Bit 0 Shall be cleared to zero

6.7.27 Word 78: SATA Feature support

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation
- Bit 5 1 = Supports asynchronous notification
- Bit 4 1 = Supports in-order data delivery
- Bit 3 1 = Device supports initiating interface power management
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization
- Bit 1 1 = Supports non-zero buffer offsets
- Bit 0 Shall be cleared to zero

6.7.28 Word 79: SATA Features enabled

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation enabled
- Bit 5 1 = Supports asynchronous notification enabled
- Bit 4 1 = Supports in-order data delivery enabled
- Bit 3 1 = Device supports initiating interface power management enabled
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization enabled

- Bit 1 1 = Supports non-zero buffer offsets enabled
- Bit 0 Shall be cleared to zero

6.7.29 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
- If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
- Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
- If bit 5 of word 82 is set to one, write cache is supported.
- If bit 6 of word 82 is set to one, look-ahead is supported.
- Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
- Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
- Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 82 is obsolete.
- Bit 12 of word 82 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 82 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 82 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 82 is obsolete.

- Bit 0 of word 83 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 83 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- Bit 2 of word 83 shall be set to zero; the Drive does not support the CFA feature set.
- If bit 3 of word 83 is set to one, the Drive supports the Advanced Power Management feature set.
- Bit 4 of word 83 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.7.30 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
- If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security
- Set Password command.
- Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
- If bit 5 of word 85 is set to one, write cache is enabled.
- If bit 6 of word 85 is set to one, look-ahead is enabled.
- Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
- Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
- Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 85 is obsolete.
- Bit 12 of word 85 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 85 shall be set to one; the Drive supports the Read Buffer command.

- Bit 14 of word 85 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 85 is obsolete.
- Bit 0 of word 86 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 86 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- If bit 2 of word 86 shall be set to zero, the Drive does not support the CFA feature set.
- If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
- Bit 4 of word 86 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.7.31 Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device does not support UDMA.

- Bit 15 Reserved
- Bit 14 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7 Reserved
- Bit 6 1 = Ultra DMA mode 6 and below are supported. Bits 5:0 shall be set to 1.
- Bit 5 1 = Ultra DMA mode 5 and below are supported. Bits 4:0 shall be set to 1.
- Bit 4 1 = Ultra DMA mode 4 and below are supported. Bits 3:0 shall be set to 1.
- Bit 3 1 = Ultra DMA mode 3 and below are supported, Bits 2:0 shall be set to 1.
- Bit 2 1 = Ultra DMA mode 2 and below are supported. Bits 1:0 shall be set to 1.
- Bit 1 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0 1 = Ultra DMA mode 0 is supported

6.7.32 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete. Support of this word is mandatory if the Security feature set is supported.
Required Time= (Value*2) minutes

6.7.33 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision is not supported. Support of this word is mandatory if the Security feature set is supported.

6.7.34 Word 128: Security status

Support of this word is mandatory if the Security feature set is supported.
Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.
Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.
Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hardware reset.
Bit 3 of word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.
Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.
Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.
Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

6.7.35 Word 129: Write protect Status (Vendor information)

Word 129 identifies the Vendor Specific Write Status.

- Bit 15 = permanent write protect, out of spare blocks
- Bit 14 = permanent write protect due to table corruption
- Bit 13 = read protection due to table corruption
- Bit 9 = permanent write protect from vendor command
- Bit 8 = temporary write protect from vendor command

6.8 Idle (97h or E3h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 23 defines the Byte sequence of the Idle command.

Table 23: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

6.9 Idle Immediate (95h or E1h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 24 defines the Idle Immediate command Byte sequence.

Table 24: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.10 Media Lock/Media Unlock (DEh/DFh)

This command is effective an NOP command and always fails with the Drive returning command aborted. Table 25 defines the Byte sequence of the commands.

Table 25: Media Lock/Media Unlock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	DEh/DFh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.11 NOP (00h)

This command always fails with the Drive returning command aborted. Table 26 defines the Byte sequence of the NOP command.