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swissbit®

Product data sheet

## Industrial CompactFlash™ Card

### C-300 Series

up to UDMA / MDMA4 / PIO6

Standard and industrial  
temperature grade

BU: Swissbit Group

Date: May 27, 2013

Revision: 1.70

File:

C-300\_data\_sheet\_CF-HxBK\_Rev170.doc





# C-300 Series – UDMA CompactFlash™ Card, 64MByte up to 4GByte, 3.3/5V Supply

## 1. Features

- highly-integrated memory controller
  - Fully compliant with CompactFlash™ specification 3.0, compatible with specification 4.1
  - Fully compatible with PCMCIA specification
  - PC Card ATA Interface supported
  - True IDE mode compatible
  - Up to PIO mode 6 supported
  - Up to MDMA4 supported
  - Up to UDMA4 supported
  - Hardware RS-code ECC (4 Bytes/528 Bytes correction)
  - Fix drive (IDE mode) & removable drive (PCMCIA mode) as default in the same card
- Small form factor
  - CFC Type I: 36.4mm x 42.8mm x 3.3mm
- Low-power CMOS technology
- 3.3V or 5.0V power supply
- Power saving mode (with automatic wake-up)
- S.M.A.R.T. support by \*-SMA product type
- Wear Leveling: equal wear leveling of static and dynamic data  
The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Data Retention: 10 year (JESD47)
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 16/32 sectors data loss (old data kept) for 2k/4k Page flash respectively
  - All data written to the flash if card status is ready after write command
- High reliability
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF: > 3,000,000 hours
  - Data reliability: < 1 non-recoverable error per 10<sup>14</sup> bits read
  - Number of insertions: > 10,000
- Hot swappable in PCMCIA modes
- High performance
  - Up to 66MB/s burst transfer rate in UDMA4
  - Sustained Write performance: up to 20MB/s (UDMA4)
  - Sustained Read Performance: up to 37MB/s (UDMA4)
- Available densities
  - up to 4GBytes
  - 1 or 2 channel cards are available depends at the application requirement
- Operating System support
  - Standard Software Drivers operation CompactFlash
- Controlled BOM



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### 3. Order Information

#### 3.1 Standard part numbers

IDE-FIX & PCMCIA-Removable / PIO, DMA & UDMA support

Density	Part Number	Comment
	<b>1 channel Toshiba</b>	
64MB	SFCF0064HxBK1TO-t-MS-5y3-SMA	
128MB	SFCF0128HxBK1TO-t-MS-5y3-SMA	
256MB	SFCF0256HxBK1TO-t-MS-5y3-SMA	
512MB	SFCF0512HxBK1TO-t-MS-5y3-SMA	2 channel variation recommended
1GB	SFCF1024HxBK1TO-t-MS-5y3-SMA	2 channel variation recommended
2GB	SFCF2048HxBK1TO-t-DT-5y3-SMA	C-320 or C-440 Series are recommended
4GB	SFCF4096HxBK1TO-t-QT-5y3-SMA	
	<b>2 channel Toshiba</b>	
512MB	SFCF0512HxBK2TO-t-MS-5y3-SMA	
1GB	SFCF1024HxBK2TO-t-MS-5y3-SMA	
2GB	see C-320/C-440 Series data sheet	

**Table 1: Standard and industrial product list**

x= depends on product generation

y= firmware generation

t= C commercial temperature; =I industrial temperature

#### 3.2 Offered OEM options

- Disabling MDMA and/or UDMA modes
- Customer specified card size and card geometry (C/H/S – cylinder/head/sector)
- Customer specified CIS and drive ID strings
- Preload service (also images with any file system)
- Customized front label
- ROM mode (write protected with preloaded software)
- Special Firmware solutions for additional customer requirements
- ...

## 4. Product Specification

The CompactFlash is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.

The Card operates in three basic modes:

- **PC card ATA I/O mode**
- **PC card ATA memory mode**
- **True IDE mode**

The CompactFlash also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.

**Standard** cards are shipped as max. **PIO6 and MDMA4 (80ns) and UDMA4 (30ns)**.

If the cards should be used in extended speed modes, they should be qualified on the target system and the system should **fulfill the requirements** listed below.

It conforms to the PCMCIA Card Specification 2.1 when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC), defect handling, diagnostics and clock control**.

The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.

Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.

The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.

The specification has been realized and approved by the CompactFlash Association (CFA).

This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design. The system highlights are shown in Table 2 ... Table 8.

### Related Documentation

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994
- CF+ and CompactFlash Specification Revision 3.0



## 4.1 System Performance

**Table 2: System Performance**

System Performance			Typ.	Max.	Unit
Sleep to write				5	ms
Sleep to read				5	
Power up to Ready			<500	1000	
Reset to Ready (PCMCIA/IDE Master )			200	500	
Data transfer Rate (UDMA4 burst)				66	MB/s
Sustained Read (measured)	SFCF*BK1T0* 2k <sup>(1)</sup>	1ch 64MB–512MB	19	24	MB/s
	SFCF*BK1T0* 4k <sup>(1)</sup>	1ch 1GB–2GB	22	25	
	SFCF*BK2T0* 2k <sup>(1)</sup>	2ch 512MB – 1GB	35	37	
Sustained Write (measured)	SFCF*BK1T0* 2k <sup>(1)</sup>	1ch 64MB–512MB	11–13	14	
	SFCF*BK1T0* 4k <sup>(1)</sup>	1ch 1GB–2GB	18	20	
	SFCF*BK2T0* 2k <sup>(1)</sup>	2ch 512MB – 1GB	18	20	
Command to DRQ	Read		100	2000	μs
	Write		30	1000	
Access Time			Read		ms

- All values refer to Toshiba Flash chips CompactFlash Card in UDMA mode 4, cycle time 30ns in True-IDE mode with Sequential write/read test with 128kB/command. The number of flash and flash manufacturer is decoded in the part number, also the flash page size is depicted in this table. The densities are the current standard products.  
Sustained Speed depends on flash type and number, file size, and burst speed

## Requirements for using extended speed (PIO 5, 6/ MDMA 3, 4) (CompactFlash Specification 3.0; section 4.3.7)

The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:

1. Only one CF device shall be attached to the CF Bus.
2. The host shall not present a load of more than 40pF to the device for all signals, including any cabling.
3. The maximum cable length is 0.05 m (2 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported.
4. The  $\overline{\text{WAIT}}$  and  $\text{IORDY}$  signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes.

## Ultra DMA Electrical Requirements

(CompactFlash Specification 3.0; section 4.3.8)

Operation in Ultra DMA mode requires careful attention to cabling, printed circuit board (PCB) trace routing and termination for reliable operation. These requirements are described in the following sections.

### Host and Card signal capacitance limits for Ultra DMA operation

The host interface signal capacitance at the host connector shall be a maximum of 25pF for each signal as measured at 1 MHz.

The card interface signal capacitance at the card connector shall be a maximum of 20pF for each signal as measured at 1 MHz.

### Series termination required for Ultra DMA operation

Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. The CF specification describes typical values for series termination at the host and the device.

## 4.2 Environmental Specifications

### 4.2.1 Recommended Operating Conditions

**Table 3: CF Card Recommended Operating Conditions**

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage (5V)	4.5V to 5.5V – 5.0V ±10%
Power Supply VCC Voltage (3.3V)	2.97V to 3.63V – 3.3V ±10%

**Table 4: Current consumption (1)**

Current Consumption (type)	3.3V	5V	Unit
Read (MDMA2/UDMA4/max) 1ch	50 / 70 / 90	65 / 85 / 100	mA
Write (MDMA2/UDMA4/max) 1ch	50 / 70 / 90	75 / 80 / 100	
Read (MDMA2/UDMA4/max) 2ch	60 / 80 / 130	85 / 120 / 140	mA
Write (MDMA2/UDMA4/max) 2ch	60 / 80 / 120	95 / 110 / 130	
Sleep/Idle Mode (typ/max)	0.5 / 1.5	3.5 / 5.0	

1. All values are typical at 25° C and nominal supply voltage and refer to 512MByte (1ch) or 1GByte (2ch) CompactFlash Card. Max values are for 256MB (1ch) and 4GB (2ch) cards in UDMA4 mode in IDE mode. The card goes to Sleep/Idle mode 20ms (default) after last host command.

### 4.2.2 Recommended Storage Conditions

**Table 5: CF Card Recommended Storage Conditions**

Parameter	Value
Storage Temperature	-50°C to 100°C

### 4.2.3 Shock, Vibration, and Humidity

**Table 6: Shock, Vibration, and Humidity**

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20 G peak, 20-2000Hz, 4 per direction (JEDEC JESD22, method B103) 5.35G RMS, 15 min per plane (IEC 68-2-6)
Shock	1.5k G peak, 0.5ms 5 times (JEDEC JESD22, method B110) 30 G, 11ms 1 time (IEC 68-2-27)

### 4.3 Physical Dimensions

**Table 7: Physical Dimensions**

Parameter	Value	Unit
Width	42.8	mm
Height	36.4	
Thickness	3.3	
Weight (typ.)	10	g

### 4.4 Reliability

**Table 8: System Reliability and Maintenance**

Parameter	Value
MTBF @ 25°C	> 3,000,000 hours (1)
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10 <sup>14</sup> bits Read (1)
Data Retention	10 years (JESD47)

(1) Dependent on final system qualification data.

### 4.5 Drive Geometry / CHS Parameter

**Table 9: CF capacity specification**

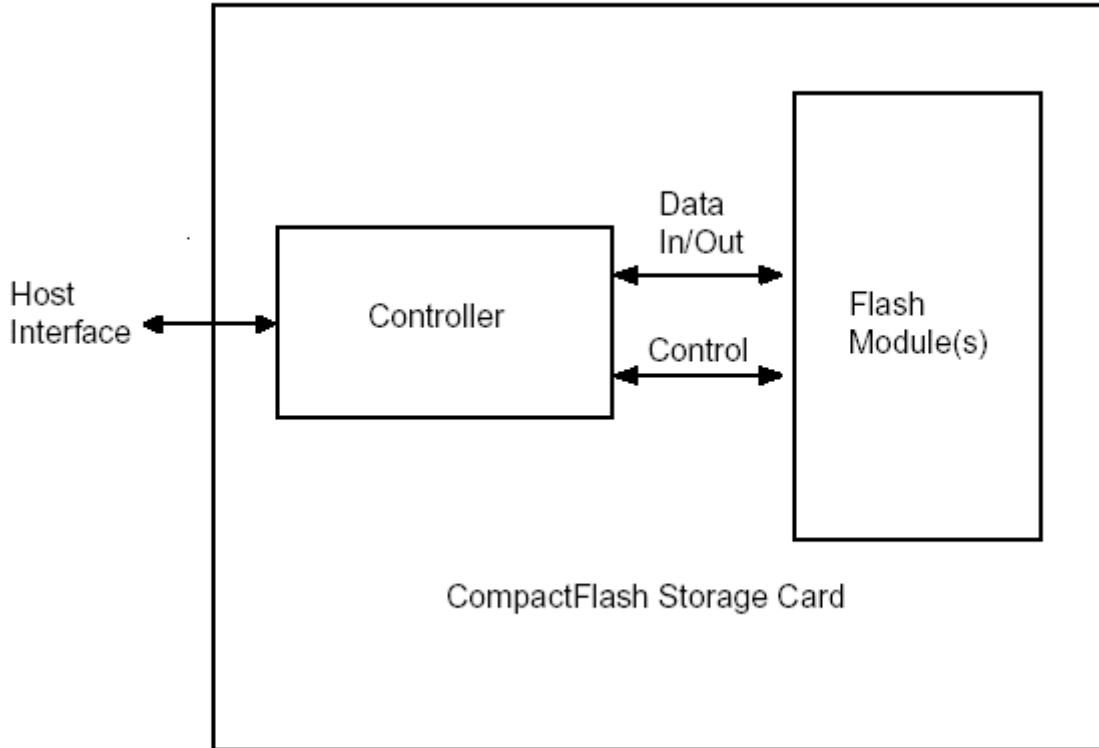
Capacity	Cylinders	Heads	Sectors / track	Sectors	Total addressable capacity (Byte)
64MB	490	8	32	125,440	64,225,280
128MB T0	937	8	32	239,872	122,814,464
256MB	980	16	32	501,760	256,901,120
512MB	993	16	63	1,000,944	512,483,328
1GB	1,986	16	63	2,001,888	1,024,966,656
2GB	3,970	16	63	4,001,760	2,048,901,120
4GB	7,964	16	63	8,027,712	4,110,188,544

### 4.6 Physical description

The CompactFlash Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 shows the Block Diagram of the CompactFlash Memory Card.

The Card is offered in a Type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27mm) centers. Figure 21 shows Type I Card Dimensions.

Figure 1: CompactFlash Memory Card Block Diagram



## 5. Electrical interface

### 5.1 Electrical description

The CompactFlash Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode with MWDMA and UDMA, which is compatible with most disk drives

The signal/pin assignments are listed in Table 10 Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output.

The configuration of the Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the memory card.



Table 11 describes the I/O signals. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.

All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

**Table 10: Pin Assignment and Pin Type**

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>(4)</sup>		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	Do3	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do3	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do3	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
3	Do4	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do4	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do4	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
4	Do5	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do5	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do5	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
5	Do6	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do6	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do6	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
6	Do7	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do7	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do7	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
7	-CE1	I	I <sub>3U</sub>	-CE1	I	I <sub>3U</sub>	-CS0	I	I <sub>3Z</sub>
8	A10	I	I <sub>1Z</sub>	A10	I	I <sub>1Z</sub>	A10 <sup>(2)</sup>	I	I <sub>1Z</sub>
9 <sup>(1)</sup>	-OE	I	I <sub>3U</sub>	-OE	I	I <sub>3U</sub>	-ATASEL	I	I <sub>3U</sub>
10	A09	I	I <sub>1Z</sub>	A09	I	I <sub>1Z</sub>	A09 <sup>(2)</sup>	I	I <sub>1Z</sub>
11	A08	I	I <sub>1Z</sub>	A08	I	I <sub>1Z</sub>	A08 <sup>(2)</sup>	I	I <sub>1Z</sub>
12	A07	I	I <sub>1Z</sub>	A07	I	I <sub>1Z</sub>	A07 <sup>(2)</sup>	I	I <sub>1Z</sub>
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A06	I	I <sub>1Z</sub>	A06	I	I <sub>1Z</sub>	A06 <sup>(2)</sup>	I	I <sub>1Z</sub>
15	A05	I	I <sub>1Z</sub>	A05	I	I <sub>1Z</sub>	A05 <sup>(2)</sup>	I	I <sub>1Z</sub>
16	A04	I	I <sub>1Z</sub>	A04	I	I <sub>1Z</sub>	A04 <sup>(2)</sup>	I	I <sub>1Z</sub>
17	A03	I	I <sub>1Z</sub>	A03	I	I <sub>1Z</sub>	A03 <sup>(2)</sup>	I	I <sub>1Z</sub>
18	A02	I	I <sub>1Z</sub>	A02	I	I <sub>1Z</sub>	A02	I	I <sub>1Z</sub>
19	A01	I	I <sub>1Z</sub>	A01	I	I <sub>1Z</sub>	A01	I	I <sub>1Z</sub>
20	A00	I	I <sub>1Z</sub>	A00	I	I <sub>1Z</sub>	A00	I	I <sub>1Z</sub>
21	Do0	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do0	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do0	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
22	Do1	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do1	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do1	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
23	Do2	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do2	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	Do2	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
24	WP	O	O <sub>1T</sub>	-IOIS16	O	O <sub>1T</sub>	-IOIS16	O	O <sub>1N</sub>
25	-CD2	O	Ground	-CD2	O	Ground	-CD2	O	Ground
26	-CD1	O	Ground	-CD1	O	Ground	-CD1	O	Ground
27	D11 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D11 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D11 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
28	D12 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D12 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D12 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
29	D13 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D13 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D13 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
30	D14 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D14 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D14 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
31	D15 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D15 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>	D15 <sup>(1)</sup>	I/O	I <sub>1Z</sub> ,O <sub>2Z</sub>
32	-CE2 <sup>(1)</sup>	I	I <sub>3U</sub>	-CE2 <sup>(1)</sup>	I	I <sub>3U</sub>	-CS1 <sup>(1)</sup>	I	I <sub>3Z</sub>
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I <sub>3U</sub>	-IORD	I	I <sub>3U</sub>	-IORD <sup>(7)</sup>	I	I <sub>3Z</sub>
							HSTROBE <sup>(8)</sup>		
							-HDMARDY <sup>(9)</sup>		
35	-IOWR	I	I <sub>3U</sub>	-IOWR	I	I <sub>3U</sub>	-IOWR <sup>(7)</sup>	I	I <sub>3Z</sub>
							STOP <sup>(8)(9)</sup>		
36	-WE	I	I <sub>3U</sub>	-WE	I	I <sub>3U</sub>	-WE <sup>(3)</sup>	I	I <sub>3U</sub>
37	READY	O	O <sub>1T</sub>	-IREQ	O	O <sub>1T</sub>	INTRQ	O	O <sub>2T</sub>
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL <sup>(5)</sup>	I	I <sub>2Z</sub>	-CSEL <sup>(5)</sup>	I	I <sub>2Z</sub>	-CSEL	I	I <sub>2U</sub>

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>(4)</sup>		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
40	-VS2	0	OPEN	-VS2	0	OPEN	-VS2	0	OPEN
41	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
42	-WAIT	0	OT1	-WAIT	0	OT1	IORDY <sup>(7)</sup>	0	ON1
							-DDMARDY <sup>(8)</sup>		
							DSTROBE <sup>(9)</sup>		
43	-INPACK	0	OT1	-INPACK	0	OT1	DMARQ	0	OZ1
44	-REG	I	I3U	-REG	I	I3U	-DMACK <sup>(6)</sup>	I	I3U
45	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
47	Do8 <sup>(1)</sup>	I/O	I1Z,OZ3	Do8 <sup>(1)</sup>	I/O	I1Z,OZ3	Do8 <sup>(1)</sup>	I/O	I1Z,OZ3
48	Do9 <sup>(1)</sup>	I/O	I1Z,OZ3	Do9 <sup>(1)</sup>	I/O	I1Z,OZ3	Do9 <sup>(1)</sup>	I/O	I1Z,OZ3
49	D10 <sup>(1)</sup>	I/O	I1Z,OZ3	D10 <sup>(1)</sup>	I/O	I1Z,OZ3	D10 <sup>(1)</sup>	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is required for CompactFlash Storage Cards.
5. The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6. **If DMA operations are not used, the signal must be held high or tied to VCC by the host, also for read registers.**
7. Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. The signal should be grounded by the host.

**Table 11: Signal Description**

Signal Name	Dir.	Pin	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 to A0 (True IDE Mode)			In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
–STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
–PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
–SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
–DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15–Doo (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. Doo is the LSB of the Even Byte of the Word. Do8 is the LSB of the Odd Byte of the Word.
D15–Doo (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15–Doo (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)		1, 50	Ground.
GND (PC Card I/O Mode)			Same for all modes.
GND (True IDE Mode)			Same for all modes.
–INPACK (PC Card Memory Mode)	0	43	This signal is not used in this mode.
–INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU.

Signal Name	Dir.	Pin	Description
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by $\text{-IORD}$ and $\text{-IOWR}$ . This signal is used in a handshake manner with $\text{-DMACK}$ , i.e., the device shall wait until the host asserts $\text{-DMACK}$ before negating $\text{DMARQ}$ , and reasserting $\text{DMARQ}$ if there is more data to transfer. $\text{DMARQ}$ shall not be driven when the device is not selected. While a DMA operation is in progress, $\text{-CS0}$ and $\text{-CS1}$ shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
$\text{-IORD}$ (PC Card Memory Mode)			This signal is not used in this mode.
$\text{-IORD}$ (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface.
$\text{-IORD}$ (True IDE Mode)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
$\text{-HDMARDY}$ (True IDE Mode – In Ultra DMA Protocol DMA Read)	I	34	In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate $\text{-HDMARDY}$ to pause an Ultra DMA transfer.
HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
$\text{-CD1}$ , $\text{-CD2}$ (PC Card Memory Mode)			These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card or is fully inserted into its socket.
$\text{-CD1}$ , $\text{-CD2}$ (PC Card I/O Mode)	0	26, 25	This signal is the same for all modes.
$\text{-CD1}$ , $\text{-CD2}$ (True IDE Mode)			This signal is the same for all modes.
$\text{-CE1}$ , $\text{-CE2}$ (PC Card Memory Mode)			These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. $\text{-CE2}$ always accesses the odd byte of the word. $\text{-CE1}$ accesses the even byte or the Odd byte of the word depending on $\text{A0}$ and $\text{-CE2}$ . A multiplexing scheme based on $\text{A0}$ , $\text{-CE1}$ , $\text{-CE2}$ allows 8 bit hosts to access all data on $\text{D0-D7}$ . See Table 31, Table 39, Table 40, Table 41, and Table 42.
$\text{-CE1}$ , $\text{-CE2}$ (PC Card I/O Mode)	I	7, 32	This signal is the same as the PC Card Memory Mode signal.
$\text{-CS0}$ , $\text{-CS1}$ (True IDE Mode)			In the True IDE Mode, $\text{-CS0}$ is the chip select for the task file registers while $\text{-CS1}$ is used to select the Alternate Status Register and the Device Control Register. While $\text{-DMACK}$ is asserted, $\text{-CS0}$ and $\text{-CS1}$ shall be held negated and the width of the transfers shall be 16 bits.
$\text{-CSEL}$ (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.

Signal Name	Dir.	Pin	Description
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
-IOWR (PC Card Memory Mode)			This signal is not used in this mode.
-IOWR (PC Card I/O Mode)	I	35	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATASEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	0	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode)			This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)	I	44	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.



Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
–RESET (True IDE Mode)			In the True IDE Mode, this input pin is the <b>active low</b> hardware reset from the host.
Vcc (PC Card Memory Mode)		13, 38	+5V, +3.3V power.
Vcc (PC Card I/O Mode)			Same for all modes.
Vcc (True IDE Mode)			Same for all modes.
–VS1, –VS2 (PC Card Memory Mode)	0	33, 40	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
–VS1, –VS2 (PC Card I/O Mode)			This signal is the same for all modes.
–VS1, –VS2 (True IDE Mode)			This signal is the same for all modes.
–WAIT (PC Card Memory Mode)	0	42	The –WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
–WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
–DDMARDY (True IDE Mode – Ultra DMA Write Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
DSTROBE (True IDE Mode – Ultra DMA Read Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
–WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
–WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
–WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	0	24	Memory Mode – The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (–IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
–IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

## 5.2 Electrical Specification

Table 12 defines the DC Characteristics for the CompactFlash Memory Card. Unless otherwise stated, conditions are:

- $V_{CC} = 5V \pm 10\%$
- $V_{CC} = 3.3V \pm 10\%$
- $0\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Table 12 shows that the Card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.

The current is measured by connecting an amp meter in series with the  $V_{CC}$  supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 12.

Table 13 shows the Input Leakage Current, Table 14 the Input Characteristics, Table 15 the Output Drive Type and Table 16 the Output Drive Characteristics.

**Table 12: Absolute Maximum Conditions**

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V
Voltage on any pin except VCC with respect to GND	V	-0.5V to VCC +0.5V

**Table 13: Input Leakage current(1)**

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	$V_{IH} = V_{CC}$ $V_{IL} = \text{GND}$	-1		1	$\mu\text{A}$
IxU	Pull Up Resistor	RPU1	$V_{CC} = 5.0\text{V}$	50		500	kOhm
IxD	Pull Down Resistor	RPD1	$V_{CC} = 5.0\text{V}$	50		500	kOhm

1. x refers to the characteristics described in Table 14. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

**Table 14: Input characteristics**

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			$V_{CC} = 3.3\text{V}$			$V_{CC} = 5.0\text{V}$			
1	Input Voltage CMOS	$V_{IH}$	2.0		3.6	2.0		5.3	V
		$V_{IL}$	-0.3		0.6	-0.3		0.8	
2	Input Voltage CMOS	$V_{IH}$	2.0		3.6	2.0		5.3	V
		$V_{IL}$	-0.3		0.6	-0.3		0.8	
3	Input Voltage CMOS Schmitt Trigger	$V_{TH}$	2.0		3.6	2.0		5.3	V
		$V_{TL}$	-0.3		0.6	-0.3		0.8	

**Table 15: Output Drive Type(1)**

Type	Output Type	Valid Conditions
Otx	Totem pole	$I_{OH}$ & $I_{OL}$
Ozx	Tri-State N-P Channel	$I_{OH}$ & $I_{OL}$
Opx	P-Channel Only	$I_{OH}$ only
Onx	N-Channel Only	$I_{OL}$ only

1. x refers to the characteristics described in Table 14. For example, O13 refers to totem pole output with a type 3 output drive characteristic.

**Table 16: Output Drive Characteristics**

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1	Output Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4			V
		$V_{OL}$	$I_{OL} = 4\text{mA}$			0.45	
2	Output Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4			V
		$V_{OL}$	$I_{OL} = 4\text{mA}$			0.45	
3	Output Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4			V
		$V_{OL}$	$I_{OL} = 4\text{mA}$			0.45	
X	Leakage Current	$I_{OZ}$	$V_{OL} = \text{Gnd}$	-10		10	$\mu\text{A}$
			$V_{OH} = V_{CC}$				

### 5.3 Additional requirements for CompactFlash Advanced Timing mode

When operating in a CompactFlash Advanced timing mode, the following conditions must be respected:

- **Only one CompactFlash Card must be connected to the CompactFlash bus.**
- The load capacitance (cable included) for all signals must be lower than 40pF.
- The cable length must be **lower than 0.15m (6 inches)**. The cable length is measured from the Card connector to the host controller. **0.46m (18 inches) cables are not supported.**

## 6. Command Interface

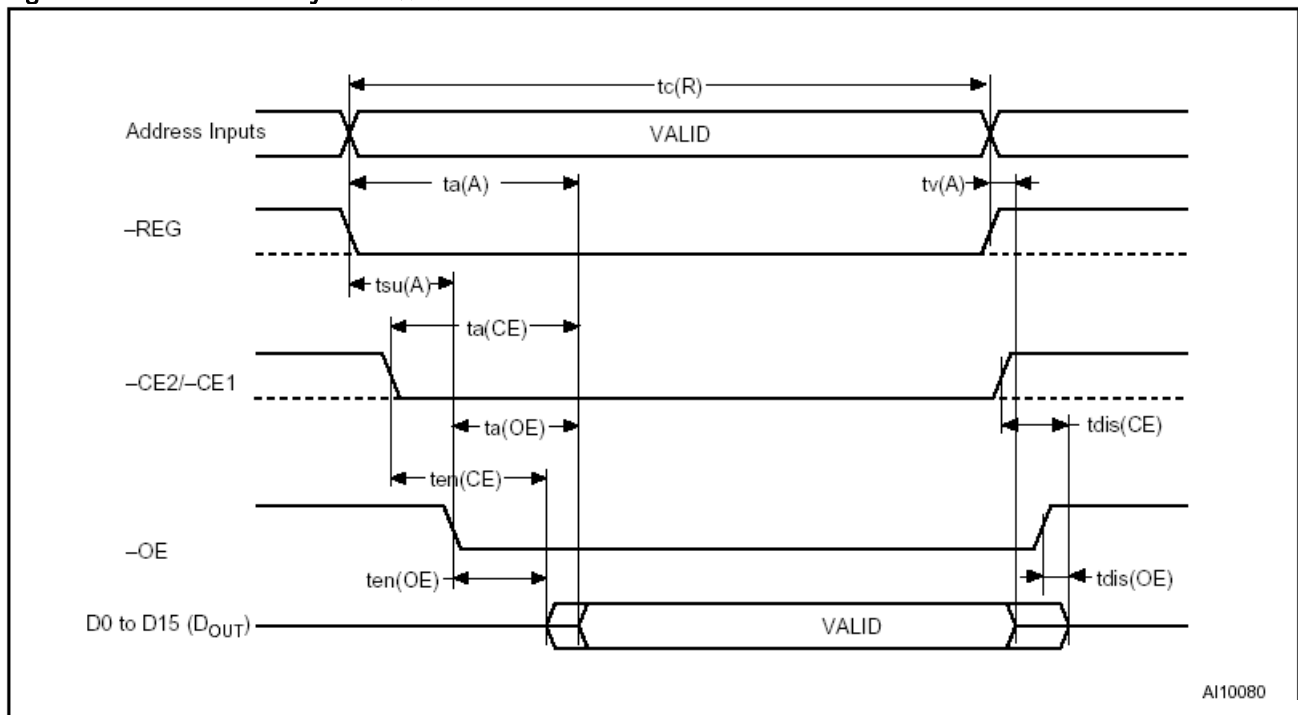
There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. Two types of bus cycles are also available in True IDE interface type: PIO transfer and Multi-Word DMA transfer.

Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, and Table 24 show the read and write timing parameters. Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 and Figure 9 show the read and write timing diagrams.

In order to set the card mode, the  $\text{-OE}$  ( $\text{-ATASEL}$ ) signal must be set and kept stable before applying VCC until the reset phase is completed. To place the card in Memory mode or I/O mode,  $\text{-OE}$  ( $\text{-ATASEL}$ ) must be driven High, while it must be driven Low to place the card in True IDE mode.

### 6.1 Attribute Memory Read and Write

Figure 2: Attribute Memory Read waveforms

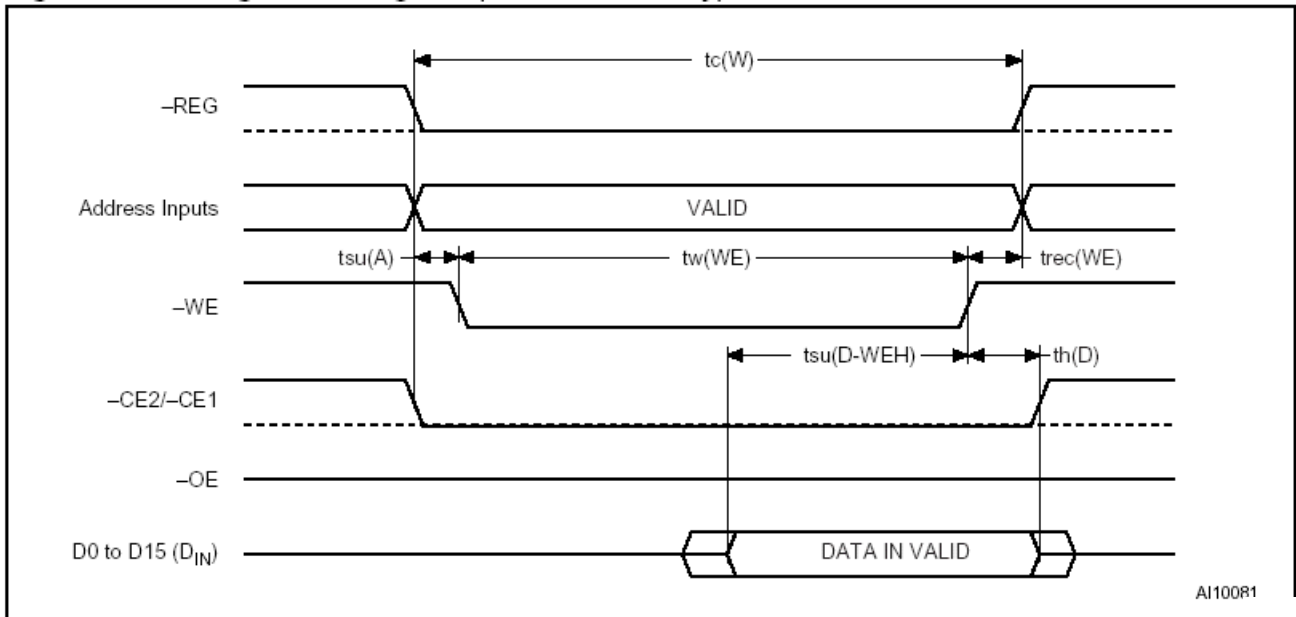


AI10080

Table 17: Attribute Memory Read timing

Item	Speed version		300ns	
	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Read Cycle Time	$t_{cl}$	$t_{AVAV}$	300	
Address Access Time	$t_{a(A)}$	$t_{AVQV}$		300
Card Enable Access Time	$t_{a(CE)}$	$t_{ELQV}$		300
Output Enable Access Time	$t_{a(OE)}$	$t_{GLQV}$		150
Output Disable Time from CE	$t_{dis(CE)}$	$t_{EHQZ}$		100
Output Disable Time from OE	$t_{dis(OE)}$	$t_{GHQZ}$		100
Output Enable Time from CE	$t_{en(CE)}$	$t_{ELQNZ}$	5	
Output Enable Time from OE	$t_{en(OE)}$	$t_{GLQNZ}$	5	
Data Valid from Address Change	$t_{v(A)}$	$t_{AXQX}$	0	
Address Setup Time	$t_{su(A)}$	$t_{AVWL}$	30	

Figure 3: Configuration Register (Attribute Memory) Write waveforms



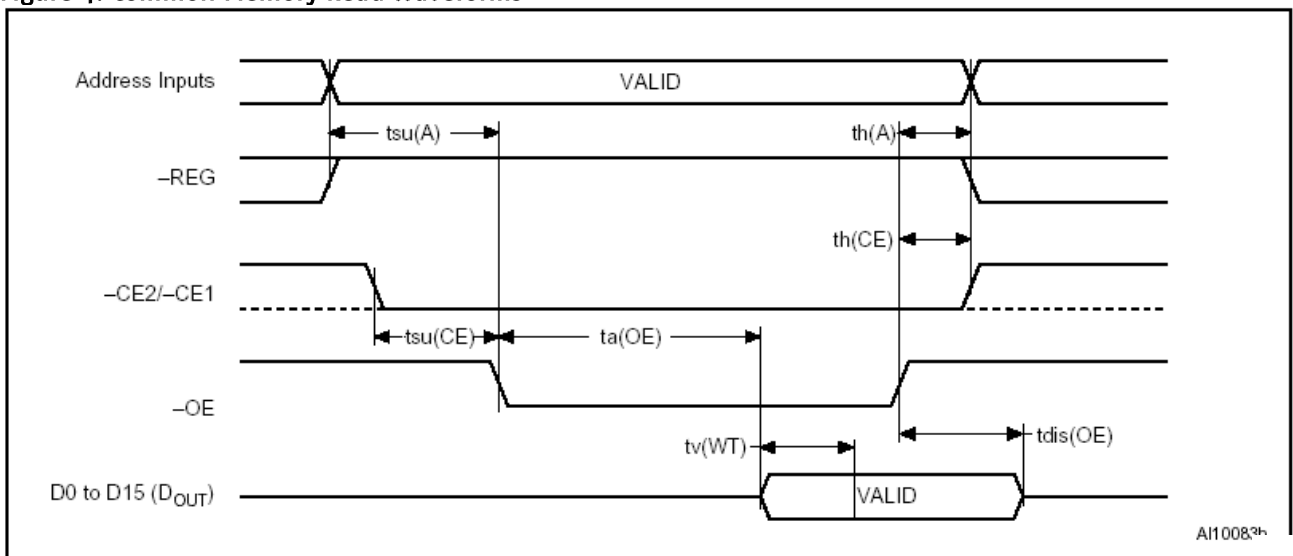
16  $D_{IN}$  signifies data provided by the system to the CompactFlash Card.

Table 18: Configuration Register (Attribute Memory) Write timing

Item	Speed Version		250ns	
	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	$t_c(W)$	tAVAV	250	
Write Pulse Width	$t_w(WE)$	tWLWH	150	
Address Setup Time	$t_{su}(A)$	tAVWL	30	
Data Setup Time for WE	$t_{su}(D-WEH)$	tDVWH	80	
Data Hold Time	$t_h(D)$	tWMDX	30	
Write Recovery Time	$t_{rec}(WE)$	tWMAX	30	

## 6.2 Common Memory Read and Write

Figure 4: Common Memory Read waveforms



17  $D_{OUT}$  means data provided by the CompactFlash Memory Card to the system.



Table 19: Common Memory Read timing (1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	

18 Swissbit CF does not assert the WAIT signal.

Figure 5: Common Memory Write Waveforms

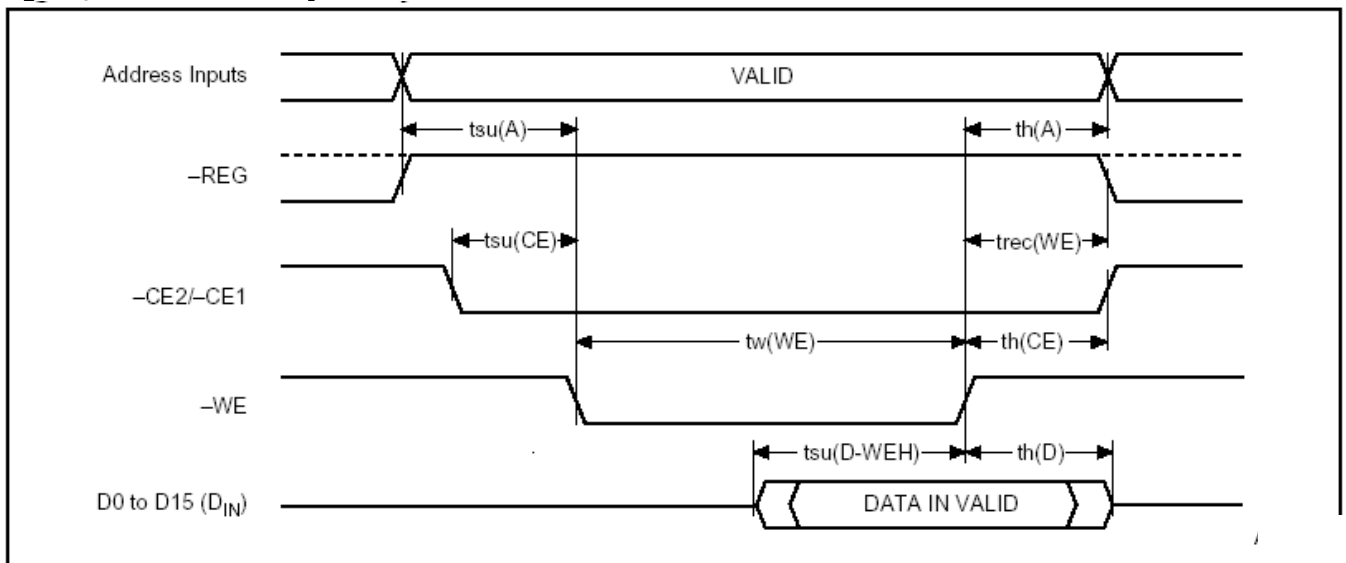


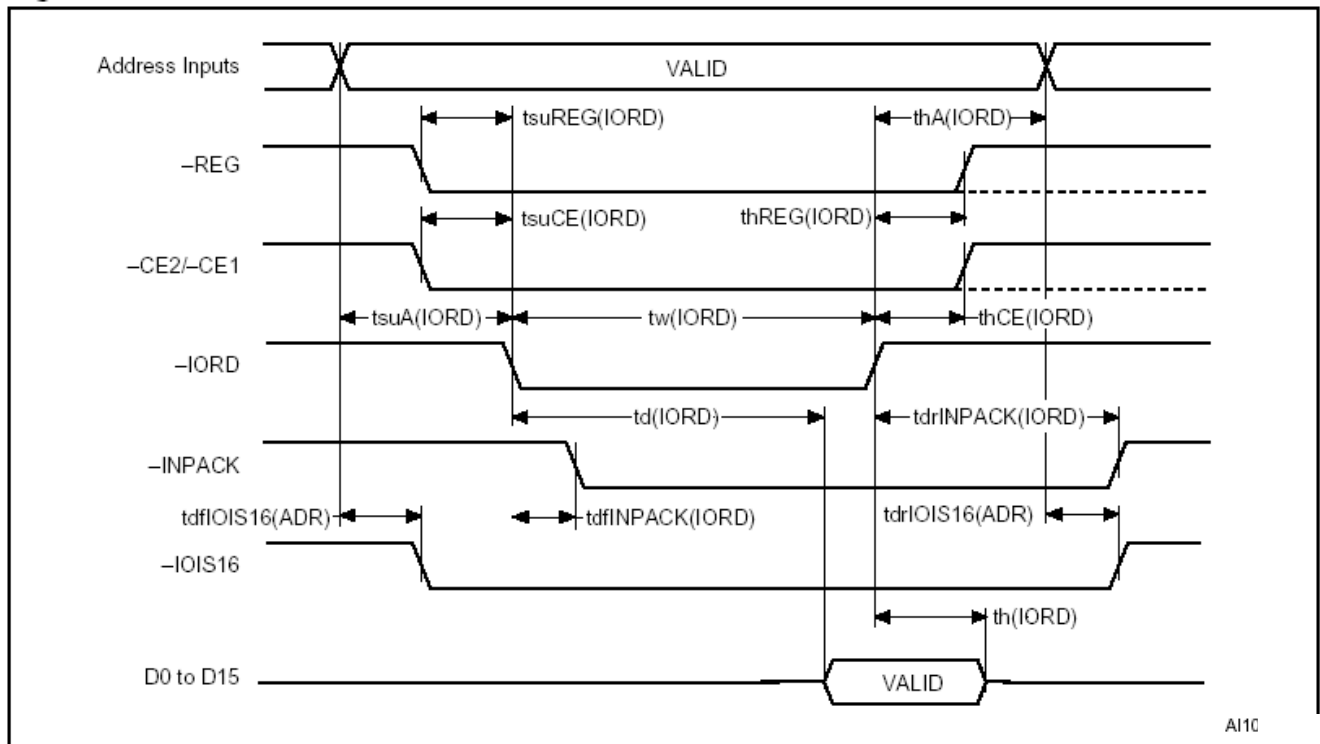
Table 20: Common Memory Write Timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tIWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	

19 Swissbit CF does not assert the WAIT signal.

### 6.3 I/O Read and Write

Figure 6: I/O Read waveforms



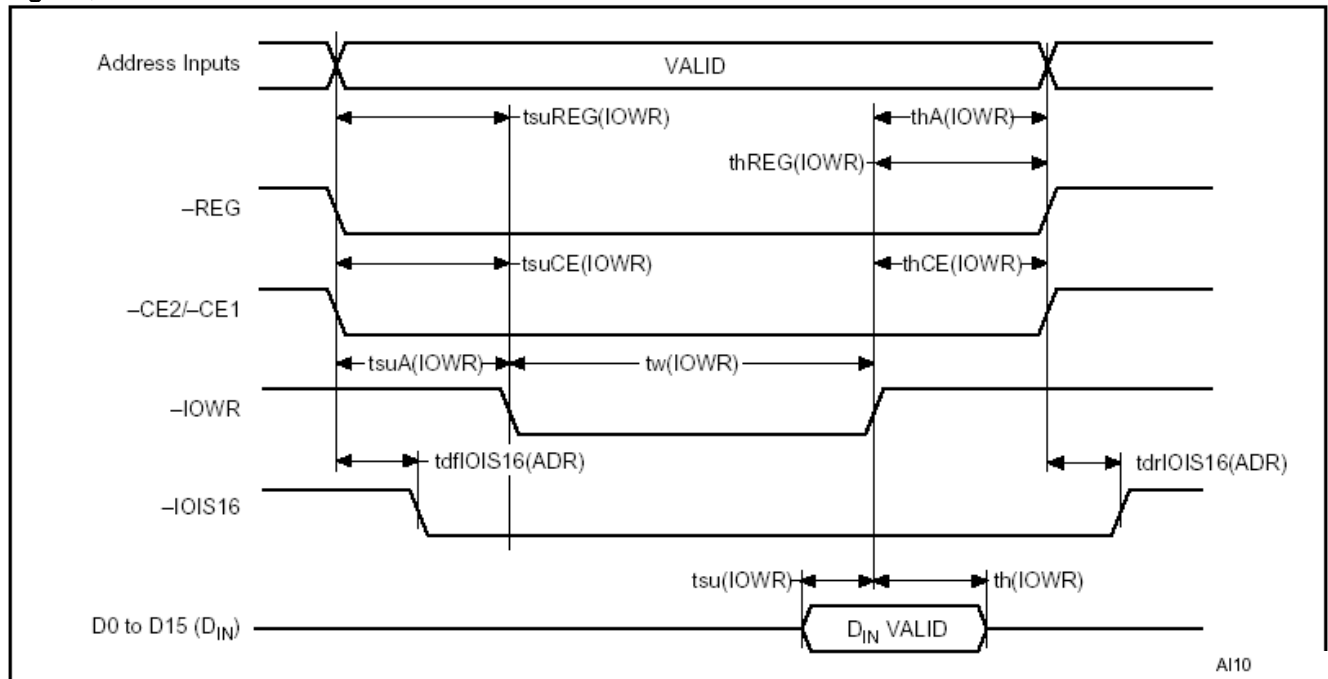
20 DOUT signifies data provided by the CompactFlash Memory Card or to the system.

Table 21: I/O Read timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	0	NA <sup>(2)</sup>	0	NA <sup>(2)</sup>	0	NA <sup>(2)</sup>
NPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45		NA <sup>(2)</sup>		NA <sup>(2)</sup>		NA <sup>(2)</sup>
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35						
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35						

- Swissbit CF does not assert the WAIT signal.
- IOIS16 is not supported in this mode.

Figure 7: I/O Write waveforms



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Table 22: I/O write timing

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Addr.	tdfIOIS16(ADR)	tAVISL		35		NA <sup>(2)</sup>		NA <sup>(2)</sup>		NA <sup>(2)</sup>
IOIS16 Delay Rising from Addr.	tdrIOIS16(ADR)	tAVISH		35		NA <sup>(2)</sup>		NA <sup>(2)</sup>		NA <sup>(2)</sup>

1.  $D_{IN}$  signifies data provided by the system to the CompactFlash Memory Card.
2. -IOIS16 and -INPACK are not supported in this mode.

## 6.4 True IDE Mode

The timing waveforms for True IDE mode and True IDE DMA mode of operation in this section are drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the waveforms inverted from their electrical states on the bus.