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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Product data sheet

Industrial CompactFlash™ Card

C-440 Series

up to UDMA6 / MDMA4 / PIO6

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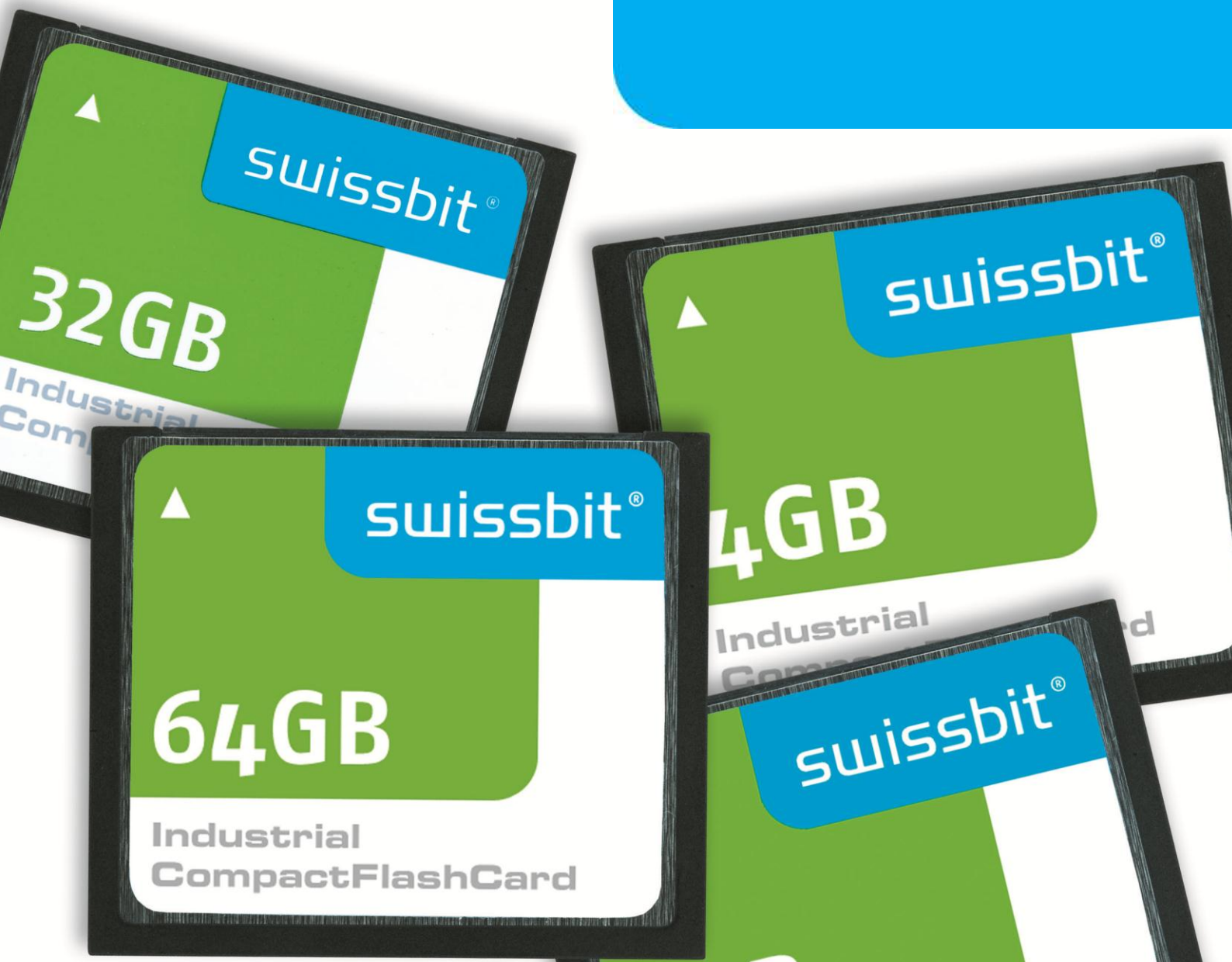


C-440 Series – Industrial UDMA CompactFlash™ Card, 2GByte up to 64GByte, 3.3/5V Supply

1 Main Features

- Highly-integrated memory controller
  - CompactFlash™ specification 4.1, compatible with specification 5.0
  - PCMCIA specification 2.1 (chapter CF-ATA Registers) & PC Card ATA Interface Specification 8, 7, 6, and 5
  - True IDE mode compatible, up to UDMA6 / MDMA4 / PIO6 supported
  - Fix drive (IDE mode) & removable drive (PC card mode) as default in the same card
  - Hot swappable in PC card modes
  - Signal termination resistors to improve signal quality
  - LBA48 address support (LBA28 limitation on request)
  - Fix drive (IDE mode) & removable drive (PC card mode) as default configuration
- Small form factor
  - CFC Type I: 36.4mm x 42.8mm x 3.3mm
- Low-power CMOS technology
- 3.3V or 5.0V power supply, card drives bus with 3.3V, inputs 5V compatible
- Power saving mode (with automatic wake-up)
- S.M.A.R.T. support and extended vendor information
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Data Retention: 10 year (JESD47)
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 32 sectors data loss (old data kept)
- High reliability
  - MTBF >3,000,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of connector insertions/removals: >10,000
  - 24bit per double sector ECC capability
  - Near Miss ECC handling at read (refresh and correct data, if multiple correctable errors detected)
  - Read Disturb Management (RDM, refresh and correct data after a certain number of read commands per block)
- High performance
  - Up to 133MB/s burst transfer rate in UDMA6
  - Sustained Write performance: up to 40MB/s (UDMA6 untrimmed)
  - Sustained Read Performance: up to 65MB/s (UDMA6)
  - Trim command supported to increase random write performance
  - Up to 300 IOPS with Trim Support (4k random write) and up to 32 IOPS untrimmed
- Available densities
  - up to 64GBytes (SLC NAND Flash)
- Operating System support
  - Standard Software Drivers operation CompactFlash™
- 2 Temperature ranges
  - Commercial Temperature range 0 ... +70°C
  - Industrial Temperature range -40 ... +85°C
- Life Cycle Management
- Controlled BOM
- RoHS compatible

2 Table of Contents

3 Order Information

3.1 Standard part numbers

IDE-FIX & PC card-Removable / PIO, DMA & UDMA support

Density	Part Number
2GB	SFCF2048HxBU2TO-t-MS-5y7-STD
4GB	SFCF4096HxBU4TO-t-MS-5y7-STD
8GB	SFCF8192HxBU2TO-t-QT-5y7-STD
16GB	SFCF16GBHxBU4TO-t-QT-5y7-STD
32GB	SFCF32GBHxBU4TO-t-QT-5y7-STD
64GB	SFCF64GBHxBU4TO-t-NU-5y7-STD

Table 1: Product list for standard product variations

X = depends on product generation;
y = depends on latest FW revision
t = C: commercial temperature; I: industrial temperature

3.2 Supported Features

- **MDMA/UDMA also in PC card mode**
- **SMART Feature Set with additional life time information**
- **TRIM command**
- **48bit Address Feature Set**
- Security Mode Feature Set
- Power Management Feature Set
- Write Cache
- Write_Buffer Command
- Read_Buffer Command
- NOP_Command
- Flush_Cache_EXT

3.3 Offered OEM options on request

- Write Protect switch
- Disabling MDMA and/or UDMA modes
- Customer specified card size and card geometry (C/H/S – cylinder/head/sector)
- Customer specified CIS and drive ATA-ID strings
- Preload service (also images with any file system)
- Customized label
- ROM mode (write protected with preloaded software)
- Special Firmware solutions for additional customer requirements
- ...

3.4 Offered LBA28 options on request

To be compatible to dedicated host systems, cards with the part number suffix "-L28" only support LBA28 commands but don't support LBA48 commands (extended) including the TRIM command are available on request.

3.4.1 Commands not supported in LBA28 cards

The following commands are not supported in "-L28" cards:

Table 2: CF-ATA Command Set (1)

Class	Command	Code	FR(1)	SC(2)	SN(3)	CY(5:4)	DH(6)	LBA(5:3)
2	Data Set Management	06h		YY			D	YY
1	Flush cache Ext	EAh					D	
1	Read DMA Ext	25h		YY	YY	YY	D	YY
1	Read Multiple Ext	29h		YY	YY	YY	D	YY
1	Read Sector(s) Ext	24h		YY	YY	YY	D	YY
1	Read Verify Sector(s) Ext	42h		YY	YY	YY	D	YY
2	Write DMA Ext	35h		YY	YY	YY	D	YY
3	Write Multiple Ext	39h		YY	YY	YY	D	YY
2	Write Sector(s) Ext	34h		YY	YY	YY	D	YY

1. FR = Features Register (1), SC = Sector Count Register (2), SN = Sector Number Register (3), CY = Cylinder Registers (5:4), DH = Card/Drive/Head Register (6), LBA = Logical Block Address Mode Supported (see command descriptions for use),
Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash™ Memory Card and head parameters are used.
YY – registers must be written twice for 48bit LBA commands
D – only the Compact Flash Memory Card parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

Data Set Management is used for the TRIM command.

3.4.2 Differences in the ATAID

Following Information are different in the ATAID compared with standard cards:

Table 3: Identify Device Information

Word Address	STD Value	L28 Value	Total Bytes	Data Field Type Information
27-46	**aaaa* -STD**	**aaaa* -L28**	40	Model number in ASCII (right justified) Big Endian Byte Order in Word ("SFCFxxxxHxBUxT0-x-xx-xxx-**xxx**")
83	**7405h***	**5005h***	2	Features/command sets supported Bit10 48bit address feature set supported Bit13 48bit address feature set incl Flush Cache EXT supported
86	**3405h***	**1005h***	2	Features/command sets enabled Bit10 48bit address feature set enabled Bit13 48bit address feature set incl Flush Cache EXT enabled
105	0001h	0000h	2	Number of sectors per Data Set Management command
169	0001h	0000h	2	Trim bit in Data Set Management not supported

* Standard values for full functionality, depending on configuration

XXXX Depending on card capacity and drive geometry

4 Product Specification

The CompactFlash™ is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in three basic modes:

- **PC card ATA I/O mode**
- **PC card ATA memory mode**
- **True IDE mode**

The CompactFlash™ also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.
Standard cards are shipped as max. **UDMA6 (30ns) and PIO6/MDMA4 (80ns).**
If the cards should be used in extended speed modes, they should be qualified on the target system and the system should **fulfill the requirements** listed below.
It conforms to the PCMCIA Card Specification 2.1 when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash™ Cards can be used with passive adapters in a PC-Card Type I, II, or Type III socket.
The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware BCH-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware ECC mechanism allows to detect and correct **6 bit per sector or 24 bit per double sector, depending on the flash**.
The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The specification has been realized and approved by the CompactFlash™ Association (CFA).
This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design. The system highlights are shown in Table 4 ... Table 10.

Related Documentation

- CF+ and CompactFlash™ Specification Revision 4.1, 5.0
- AT Attachment Interface Document, American National Standards Institute, ATA-7, 2005
- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification 7
- ATA Command Set 2 (ACS-2) for TRIM command

4.1 System Performance

Table 4: System Performance

System Performance			Typ.	Max.	Unit
Sleep to write				5	ms
Sleep to read				5	
Power up to Ready			<500	1000	
Reset to Ready (PC card/IDE Master)			200	500	
Data transfer Rate (UDMA6 burst)				133	MB/s
Sustained Read (measured)	2 channel 4k[1, 3]	2GB-16GB	59	65	MB/s
Sustained Write (measured)	2 channel 4k[1, 3]	2GB-16GB	31	35	
Sustained Read (measured)	2 channel 8k[1, 3]	32GB-64GB	58	65	MB/s
Sustained Write (measured)	2 channel 8k[1, 3]	32GB-64GB	31	35	
Random Write 4k(measured)	2 channel 4k[1, 2]	2GB-16GB	32	170 (300)	IOPS (input/output per second)
Random Write 4k(measured)	2 channel 8k[1, 2]	32GB-64GB	27	160 (300)	
Command to DRQ	Read		100	250000	µs
	Write		30	500	
Access Time	Read		0.22		ms

1. All values refer to Toshiba Flash chips with firmware revision 1
2. The number of IOPS was measured with a fully used and a trimmed card with IOMETER
3. CompactFlash™ Card in UDMA mode 6, cycle time 30ns in True-IDE mode with Sequential write/read test.
   The number of flash is decoded in the part number; also the flash page size is depicted in this table.
   Sustained Speed depends on flash type and number, file size, and burst speed.

Requirements for using extended speed (PIO 5, 6/ MDMA 3, 4)
(CompactFlash™ Specification 5.0; section 4.3.7)

The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5, 6 and Multiword DMA Modes 3, 4.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:
1. Only one CF device shall be attached to the CF Bus.
2. The host shall not present a load of more than 40pF to the device for all signals, including any cabling.
3. The maximum cable length is 0.05 m (2 in). The cable length is measured from the card connector to the host controller. **0.46 m (18 in) cables are not supported**.
4. The –WAIT and IORDY signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes.

Ultra DMA Electrical Requirements
(CompactFlash™ Specification 5.0; section 4.3.8)

Operation in Ultra DMA mode requires careful attention to cabling, printed circuit board (PCB) trace routing and termination for reliable operation. These requirements are described in the following sections.

Host and Card signal capacitance limits for Ultra DMA operation
The host interface signal capacitance at the host connector shall be a maximum of 25pF for each signal as measured at 1 MHz.
The card interface signal capacitance at the card connector shall be a maximum of 20pF for each signal as measured at 1 MHz.

Series termination required for Ultra DMA operation
Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. The CF specification describes typical values for series termination at the host and the device.
C-400 cards have the specified serial resistances in IDE bus.

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

Table 5: CF Card Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage (5V)	5.0V ±10% (4.5V to 5.5V) *)
Power Supply VCC Voltage (3.3V)	3.3V ±10% (2.97V to 3.63V) *)

*) Voltage could be between 2.95V and 5.5V

Table 6: Current consumption (1)

Current Consumption (typ)	3.3V	5V	Unit
Read (UDMA6/max)	110 / 140	110 / 140	mA
Write (UDMA6/max)	90 / 110	85 / 110	
Sleep/Idle Mode (typ/max)	3 / 5	3 / 5	

1. All values are typical at 25° C and nominal supply voltage and refer to 8Gbyte CompactFlash™ Card.
   Max values are for 32GB cards in UDMA6 mode in IDE mode.
   The card goes to Sleep/idle mode 20ms (default) after last host command.
   The sleep current at 5V depends on the signal level at the CF-Bus

4.2.2 Recommended Storage Conditions

Table 7: CF Card Recommended Storage Conditions

Parameter	Value
Storage Temperature	-50°C to 100°C

High temperature storage decreases the data retention.

4.2.3 Shock, Vibration, and Humidity

Table 8: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20 G peak, 20-2000Hz, 4 per direction (JEDEC JESD22, method B103) 5.35G RMS, 15 min per plane (IEC 68-2-6)
Shock	1.5k G peak, 0.5ms 5 times (JEDEC JESD22, method B110) 30 G, 11ms 1 time (IEC 68-2-27)

4.3 Physical Dimensions

Table 9: Physical Dimensions

Parameter	Value	Unit
Width	42.8	mm
Height	36.4	
Thickness	3.3	
Weight (typ.)	10	g

4.4 Reliability

Table 10: System Reliability and Maintenance

Parameter	Value
MTBF (at 40°C)	> 3,000,000 hours (1)
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read (1)
Data Retention	10 years (JESD47)

(1) Dependent on final system qualification data.

4.5 Drive Geometry / CHS Parameter

Table 11: CF capacity specification

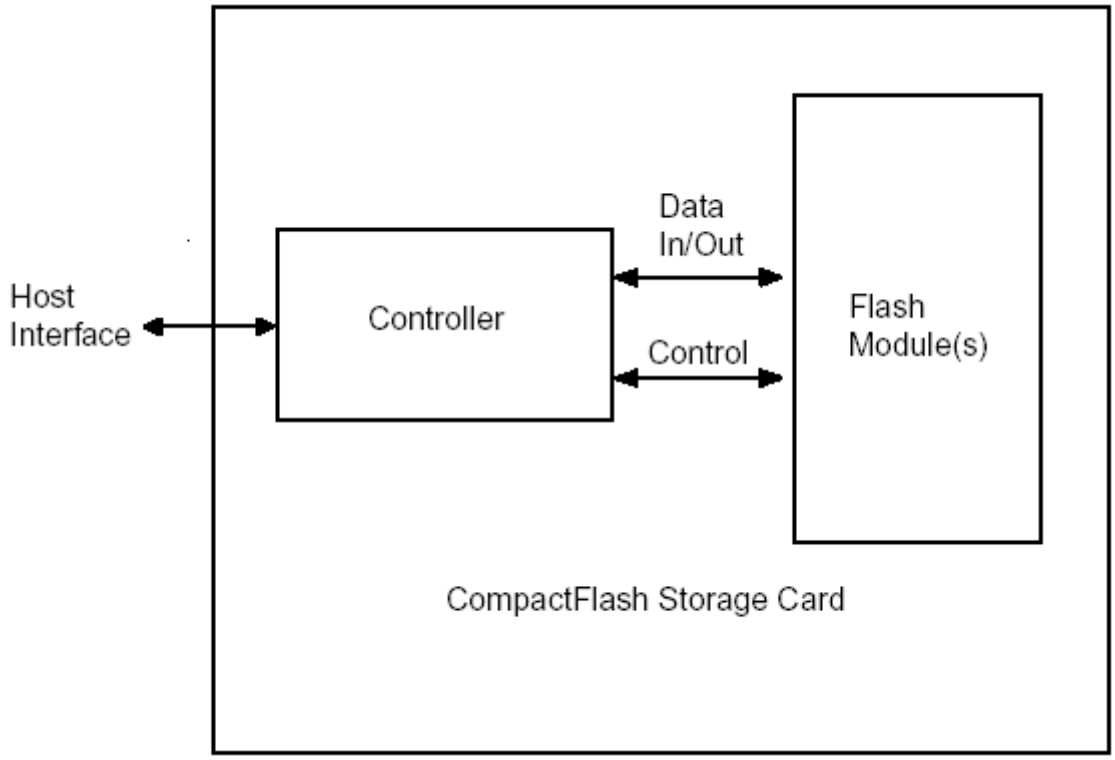
Capacity	Cylinders	Heads	Sectors / track	Sectors	Total addressable capacity (Byte)
2GB	3,970	16	63	4,001,760	2,048,901,120
4GB	7,964	16	63	8,027,712	4,110,188,544
8GB	15,880	16	63	16,007,040	8,195,604,480
16GB	16,383 (1)	16	63	31,717,728	16,239,476,736
32GB	16,383 (1)	16	63	64,028,160	32,782,417,920
64GB	16,383 (1)	16	63	125,313,024	64,160,268,288

(1) The CHS addressing is limited to about 8GB. Larger drives should be used in LBA mode.

4.6 Physical description

The CompactFlash™ Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 shows the Block Diagram of the CompactFlash™ Memory Card.
The Card is offered in a Type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27mm) centers. Figure 21 shows Type I Card Dimensions.

Figure 1: CompactFlash™ Memory Card Block Diagram



5 Electrical interface

5.1 Electrical description

The CompactFlash™ Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode with MWDMA and UDMA, which is compatible with most disk drives

The signal/pin assignments are listed in Table 12 Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output.
The configuration of the Card is controlled using the standard PC card configuration registers starting at address 200h in the Attribute Memory space of the memory card. Table 13 describes the I/O signals. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.
All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

Table 12: Pin Assignment and Pin Type

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	D3	I/O	I1Z,OZ3	D3	I/O	I1Z,OZ3	D3	I/O	I1Z,OZ3
3	D4	I/O	I1Z,OZ3	D4	I/O	I1Z,OZ3	D4	I/O	I1Z,OZ3
4	D5	I/O	I1Z,OZ3	D5	I/O	I1Z,OZ3	D5	I/O	I1Z,OZ3
5	D6	I/O	I1Z,OZ3	D6	I/O	I1Z,OZ3	D6	I/O	I1Z,OZ3
6	D7	I/O	I1Z,OZ3	D7	I/O	I1Z,OZ3	D7	I/O	I1Z,OZ3
7	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10[2]	I	I1Z
9[1]	-OE	I	I3U	-OE	I	I3U	-ATASEL	I	I3U
10	A9	I	I1Z	A9	I	I1Z	A9[2]	I	I1Z
11	A8	I	I1Z	A8	I	I1Z	A8[2]	I	I1Z
12	A7	I	I1Z	A7	I	I1Z	A7[2]	I	I1Z
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A6	I	I1Z	A6	I	I1Z	A6[2]	I	I1Z
15	A5	I	I1Z	A5	I	I1Z	A5[2]	I	I1Z
16	A4	I	I1Z	A4	I	I1Z	A4[2]	I	I1Z
17	A3	I	I1Z	A3	I	I1Z	A3[2]	I	I1Z
18	A2	I	I1Z	A2	I	I1Z	A2	I	I1Z
19	A1	I	I1Z	A1	I	I1Z	A1	I	I1Z
20	A0[11]	I	I1Z	A0[11]	I	I1Z	A0	I	I1Z
21	D0	I/O	I1Z,OZ3	D0	I/O	I1Z,OZ3	D0	I/O	I1Z,OZ3
22	D1	I/O	I1Z,OZ3	D1	I/O	I1Z,OZ3	D1	I/O	I1Z,OZ3
23	D2	I/O	I1Z,OZ3	D2	I/O	I1Z,OZ3	D2	I/O	I1Z,OZ3
24	WP	O	OT3	-IOIS16[10]	O	OT3	-IOIS16	O	ON3
25	-CD2	O	Ground	-CD2	O	Ground	-CD2	O	Ground
26	-CD1	O	Ground	-CD1	O	Ground	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	D11[1]	I/O	I1Z,OZ3	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	D12[1]	I/O	I1Z,OZ3	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	D13[1]	I/O	I1Z,OZ3	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
31	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	-CE2[1]	I	I3U	-CS1[1]	I	I3Z
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I3U	-IORD	I	I3U	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z
35	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR[7] STOP[8][9]	I	I3Z
36	-WE	I	I3U	-WE	I	I3U	-WE[3]	I	I3U
37	READY	O	OT1	-IREQ	O	OT1	INTRQ	O	OZ1
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL[5]	I	I2Z	-CSEL[5]	I	I2Z	-CSEL	I	I2U
40	-VS2	O	OPEN	-VS2	O	OPEN	-VS2	O	OPEN
41	RESET	I	I2U	RESET	I	I2U	-RESET	I	I2U
42	-WAIT	O	OT1	-WAIT	O	OT1	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1
43	-INPACK	O	OT1	-INPACK	O	OT1	DMARQ	O	OZ1
44	-REG	I	I3U	-REG	I	I3U	-DMACK[6]	I	I3U
45	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
47	D8[1]	I/O	I1Z,OZ3	D8[1]	I/O	I1Z,OZ3	D8[1]	I/O	I1Z,OZ3
48	D9[1]	I/O	I1Z,OZ3	D9[1]	I/O	I1Z,OZ3	D9[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is required for CompactFlash™ Storage Cards.
5. The –CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6. **If DMA operations are not used, the signal must be held high or tied to VCC by the host, also for read registers.**
7. Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. The signal should be grounded by the host.
10. **In PC-Card mode, the IOIS16 signal does not work as fully specified. If a host uses this signal, this may result in 16 bit accesses being changed to two 8 bit accesses. Depending on the address, this may result in an incompatibility with the host controller.**
11. **In PC-Card mode (memory and I/O), 16 bit ATA register file accesses (i.e. both -CE1 and -CE2 asserted) do not work as fully specified if A0 is high.**

If you have host-card incompatibilities please contact Swissbit.

Table 13: Signal Description

Signal Name	Dir.	Pin	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash™ Storage Card, the memory mapped port address registers within the CompactFlash™ Storage Card, a byte in the card's information structure and its configuration control and status registers. **In PC-Card mode, 16 bit ATA register file accesses (i.e. both -CE1 and -CE2 low) do not work if A0 is high. A simple test will show the C-400 compatibility to a certain host. If the C-400 cards can be recognized (Identify Device and MBR data is read out successfully), then this PC card issue will likely not affect the operation in this host. (1)**
A10 to A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 to A0 (True IDE Mode)			In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
–STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
–PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
–SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
–DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15-D0 (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D0 is the LSB of the Even Byte of the Word. D8 is the LSB of the Odd Byte of the Word.
D15-D0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15-D0 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)		1, 50	Ground.
GND (PC Card I/O Mode)			Same for all modes.
GND (True IDE Mode)			Same for all modes.
–INPACK (PC Card Memory Mode)	0	43	This signal is not used in this mode.
–INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash™ Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash™ Storage Card and the CPU.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PC card and True-IDE modes of operation need not alter the PC card mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.

Signal Name	Dir.	Pin	Description
–IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
–IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash™ Storage Card when the card is configured to use the I/O interface.
–IORD (True IDE Mode)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.
HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
–CD1, –CD2 (PC Card Memory Mode)	0	26, 25	These Card Detect pins are connected to ground on the CompactFlash™ Storage Card. They are used by the host to determine that the CompactFlash™ Storage Card or is fully inserted into its socket.
–CD1, –CD2 (PC Card I/O Mode)			This signal is the same for all modes.
–CD1, –CD2 (True IDE Mode)			This signal is the same for all modes.
–CE1, –CE2 (PC Card Memory Mode)	I	7, 32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 33, Table 40, Table 41, Table 42, and Table 43.
–CE1, –CE2 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
–CS0, –CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
–CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
–CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
–CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
–IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
–IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash™ Storage Card controller registers when the CompactFlash™ Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
–OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash™ Storage in Memory Mode and to read the CIS and configuration registers.
–OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
–ATASEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash™ Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash™ Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash™ Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
–IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash™ Storage Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
–REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
–REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
–DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. **The –DMACK signal must be high except during the execution of DMA commands. (1)** If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC card and True-IDE modes of operation need not alter the PC card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	The CompactFlash™ Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash™ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
–RESET (True IDE Mode)			In the True IDE Mode, this input pin is the **active low** hardware reset from the host.
Vcc (PC Card Memory Mode)		13, 38	+5V, +3.3V power.
Vcc (PC Card I/O Mode)			Same for all modes.
Vcc (True IDE Mode)			Same for all modes.
–VS1, –VS2 (PC Card Memory Mode)	O	33, 40	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the CompactFlash™ Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
–VS1, –VS2 (PC Card I/O Mode)			This signal is the same for all modes.
–VS1, –VS2 (True IDE Mode)			This signal is the same for all modes.
–WAIT (PC Card Memory Mode)	O	42	The –WAIT signal is driven low by the CompactFlash™ Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
–WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.

Signal Name	Dir.	Pin	Description
-DDMARDY (True IDE Mode – Ultra DMA Write Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
DSTROBE (True IDE Mode – Ultra DMA Read Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
–WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash™ Storage when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
–WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
–WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode – The CompactFlash™ Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash™ Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. **In PC-Card mode, the IOIS16 signal does not work correctly. If a host uses this signal, this may result in 16 bit accesses being changed to two 8 bit accesses. Depending on the address, this may fail. A simple test will show the C-400 compatibility to a certain host. If the C-400 cards can be recognized (Identify Device and MBR data is read out successfully), then this PC card issue will likely not affect the operation in this host. (1)**
–IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

1) If you have host-card incompatibilities please contact Swissbit.

5.2 Electrical Specification

Table 14 defines the DC Characteristics for the CompactFlash™ Memory Card. Unless otherwise stated, conditions are:

- Vcc = 5V ± 10%
- Vcc = 3.3V ± 10%
- 0 °C to +85 °C

The card interface is driven with 3.3V. The input pins are 5V tolerant.
The High-Speed IDE lines are terminated with serial resistors as specified in the ATA specification to improve the signal quality.
Table 14 shows that the Card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.
The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 14.

Table 15 shows the Input Leakage Current, Table 16 the Input Characteristics, Table 17 the Output Drive Type and Table 18 the Output Drive Characteristics.

Table 14: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V
Voltage on any pin except VCC with respect to GND	V	-0.5V to 6.5V

Table 15: Input Leakage current (1)

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current (if not pulled up or down)	IL	V_{IH} =Vcc V_{IL} = GND	-10		10	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50		500	kOhm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50		500	kOhm

1. x refers to the characteristics described in Table 16 For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 16: Input characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			Vcc = 3.3V			Vcc = 5.0V			
1	Input Voltage CMOS	V_{IH}	2.0		5.5	2.0		5.5	V
		V_{IL}	-0.3		0.8	-0.3		0.8	
2	Input Voltage CMOS	V_{IH}	2.0		5.5	2.0		5.5	V
		V_{IL}	-0.3		0.8	-0.3		0.8	
3	Input Voltage CMOS Schmitt Trigger	V_{TH}	2.0		5.5	2.0		5.5	V
		V_{TL}	-0.3		0.8	-0.3		0.8	

Table 17: Output Drive Type (1)

Type	Output Type	Valid Conditions
0tx	Totempole	I_{OH} & I_{OL}
0zx	Tri-State N-P Channel	I_{OH} & I_{OL}
0px	P-Channel Only	I_{OH} only
0nx	N-Channel Only	I_{OL} only

1. x refers to the characteristics described in Table 16 For example, 0T3 refers to totem pole output with a type 3 output drive characteristic.

Table 18: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min.	Max.	Units
1	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4		V
		V_{OL}	I_{OL} = 4mA		0.45	
2	Output Voltage	V_{OH}	I_{OH} = -1mA	2.4		V
		V_{OL}	I_{OL} = 4mA		0.45	
3	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4		V
		V_{OL}	I_{OL} = 4mA		0.45	
	Tri-State	I_{OZ}	V_{OL}= GND	-10	10	µA
X	Leakage Current		V_{OH} = Vcc			

5.3 Additional requirements for CompactFlash™ Advanced Timing mode

When operating in a CompactFlash™ Advanced timing mode (PIO5, 6 or MDMA 3, 4), the following conditions must be respected:

- **Only one CompactFlash™ Card must be connected to the CompactFlash™ bus.**
- The load capacitance (cable included) for all signals must be lower than 40pF.
- The cable length must be **lower than 0.15m** (6 inches). The cable length is measured from the Card connector to the host controller. **0.46m (18 inches) cables are not supported**.

6 Command Interface

There are two types of bus cycles and timing sequences that occur in the PC card type interface, direct mapped I/O transfer and memory access. Two types of bus cycles are also available in True IDE interface type: PIO transfer and Multi-Word DMA transfer.

Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, and Table 26 show the read and write timing parameters. Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 and Figure 9 show the read and write timing diagrams.

In order to set the card mode, the –OE (-ATASEL) signal must be set and kept stable before applying VCC until the reset phase is completed. To place the card in Memory mode or I/O mode, -OE (-ATASEL) must be driven High, while it must be driven Low to place the card in True IDE mode.

6.1 Attribute Memory Read and Write

Figure 2: Attribute Memory Read waveforms

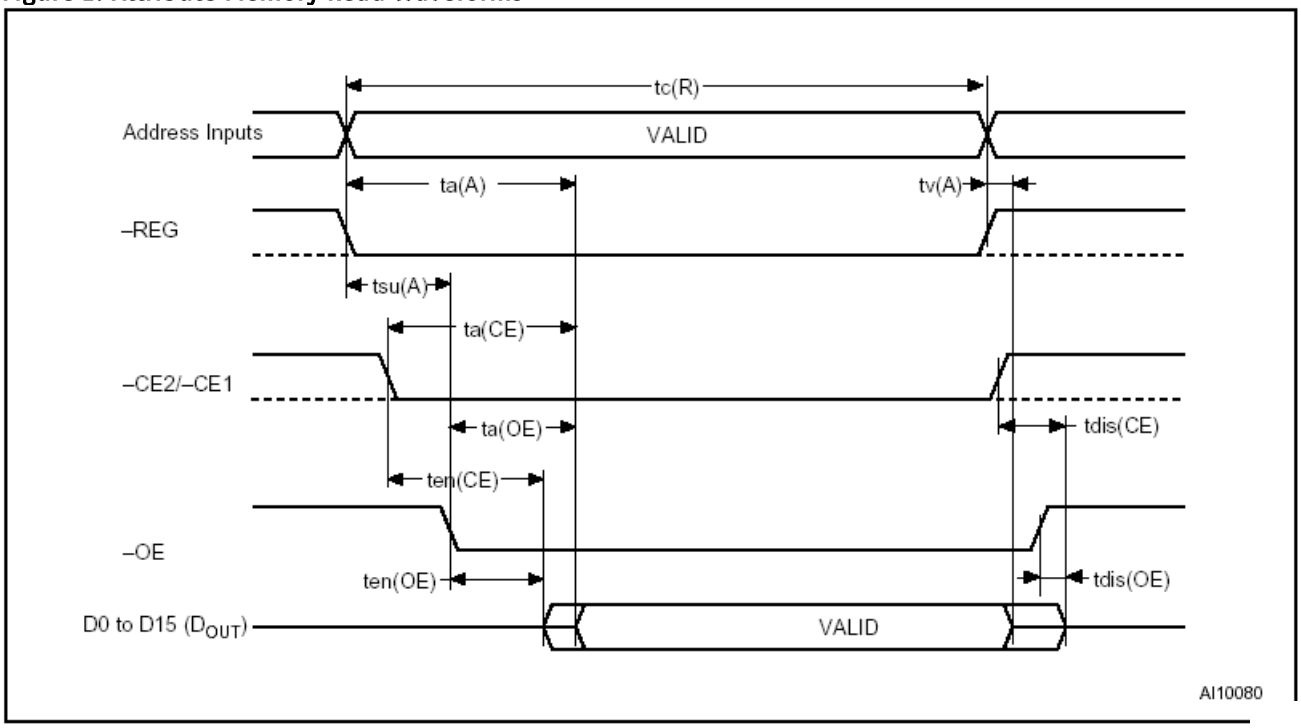
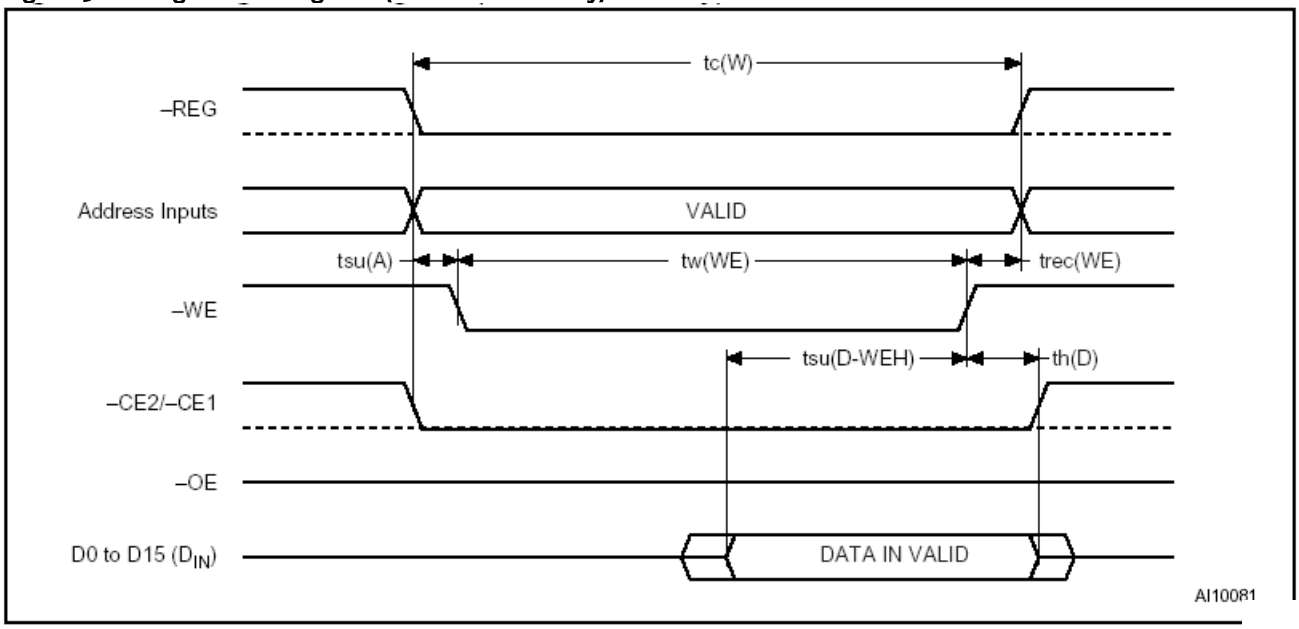


Table 19: Attribute Memory Read timing

Speed version			300ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Read Cycle Time	tcl	tAVAV	250	
Address Access Time	ta(A)	tAVQV		250
Card Enable Access Time	ta(CE)	tELQV		250
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Setup Time	tsu(A)	tAVWL	30	

Figure 3: Configuration Register (Attribute Memory) Write waveforms



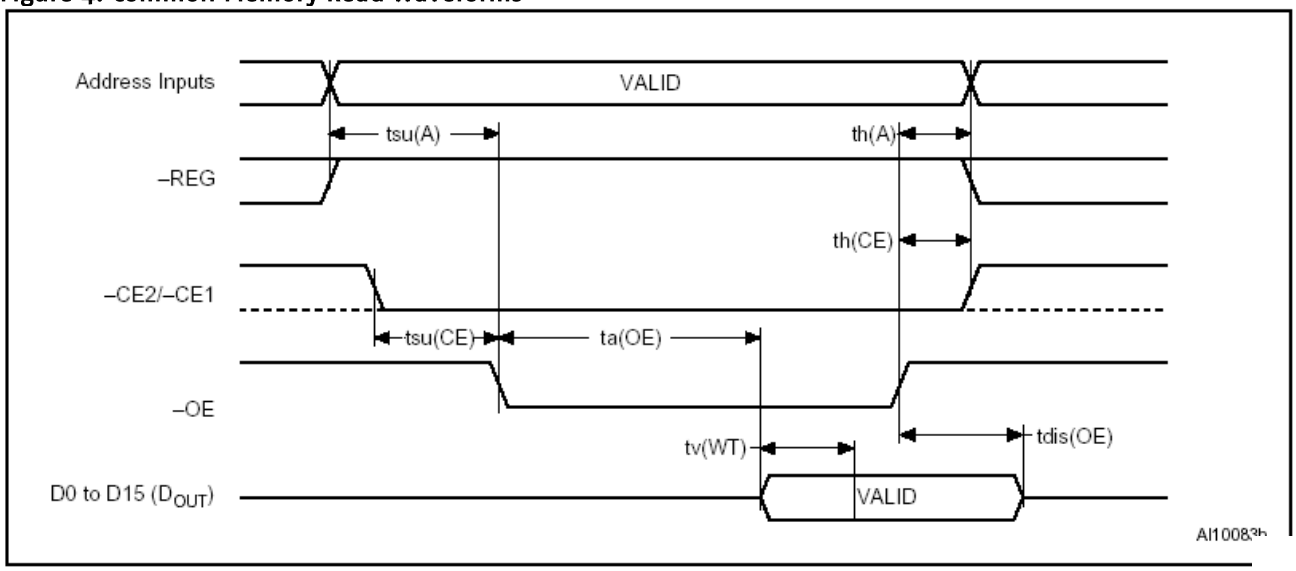
1 D_{IN} signifies data provided by the system to the CompactFlash™ Card.

Table 20: Configuration Register (Attribute Memory) Write timing

Speed Version			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	

6.2 Common Memory Read and Write

Figure 4: Common Memory Read waveforms



1 D_{OUT} means data provided by the CompactFlash™ Memory Card to the system.

Table 21: Common Memory Read timing (1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	

1 Swissbit CF does not assert the WAIT signal.

Figure 5: Common Memory Write Waveforms

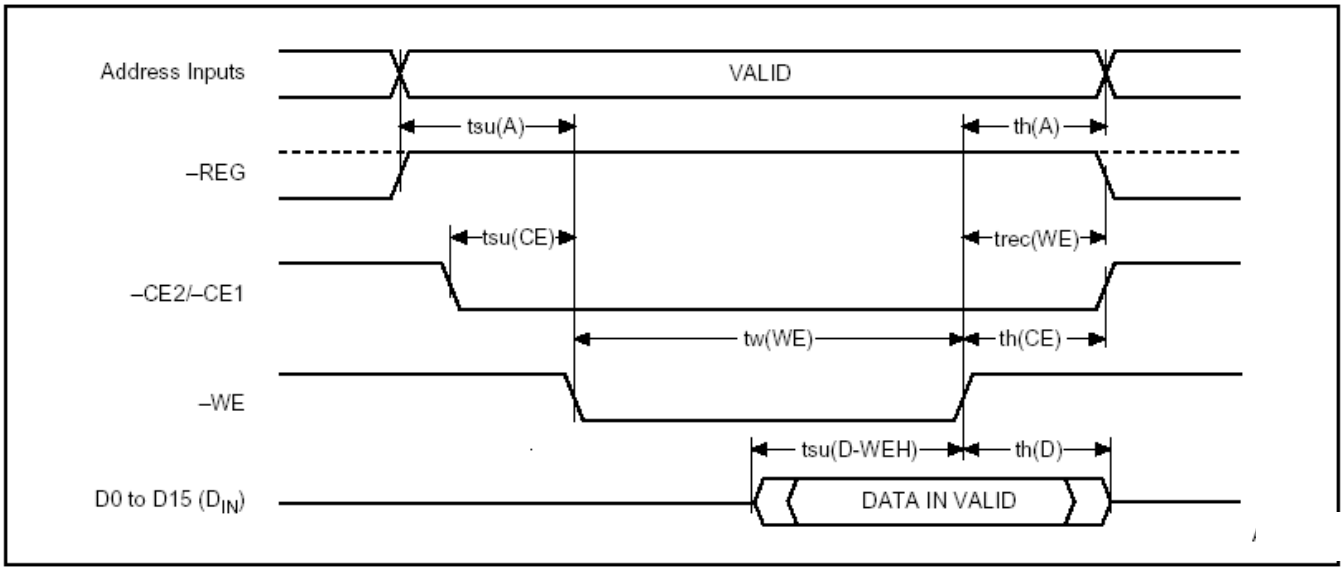


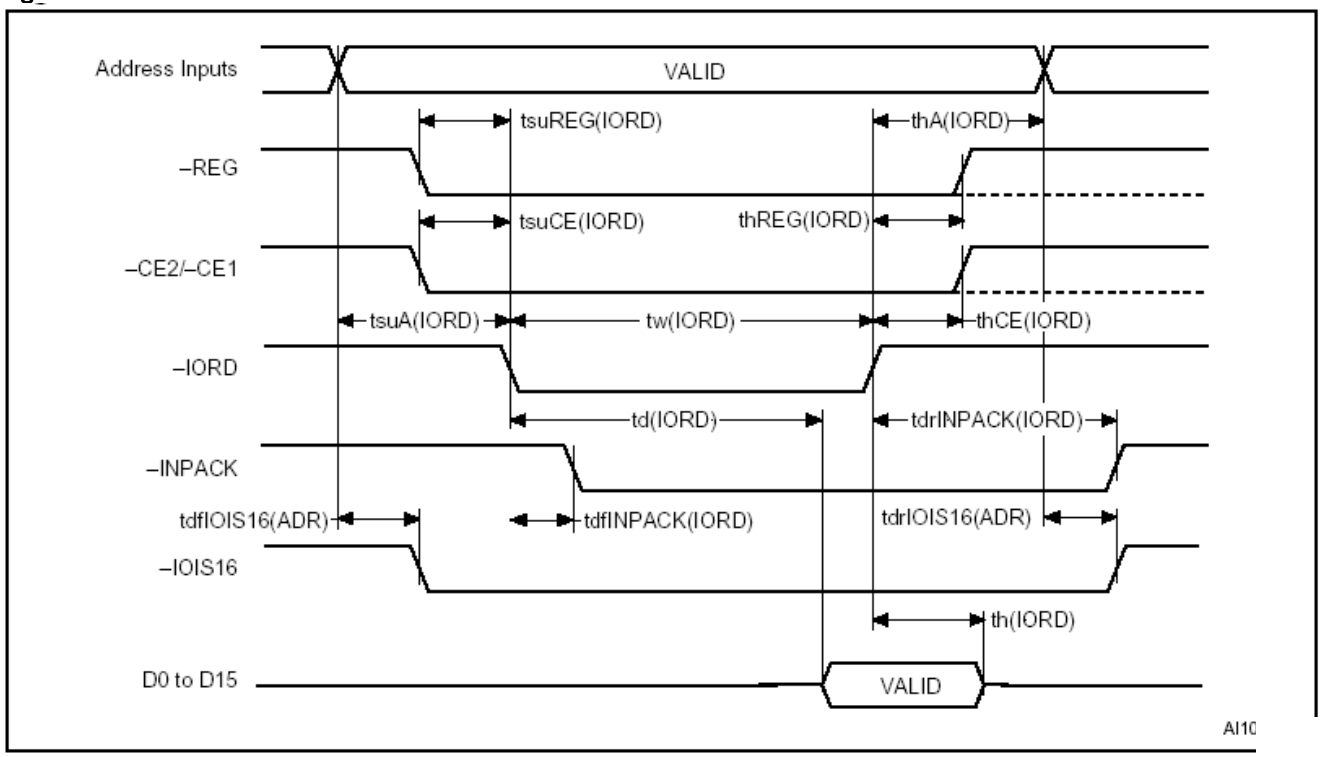
Table 22: Common Memory Write Timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tIWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	

1 Swissbit CF does not assert the WAIT signal.

6.3 I/O Read and Write

Figure 6: I/O Read waveforms



1 DOUT signifies data provided by the CompactFlash™ Memory Card or to the system.

Table 23: I/O Read timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	0	NA(2)	0	NA(2)	0	NA(2)
NPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45		NA(2)		NA(2)		NA(2)
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35						
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35						

1. This Swissbit CF card does not assert the WAIT signal.
2. –IOIS16 is not supported in this mode.

Figure 7: I/O Write waveforms

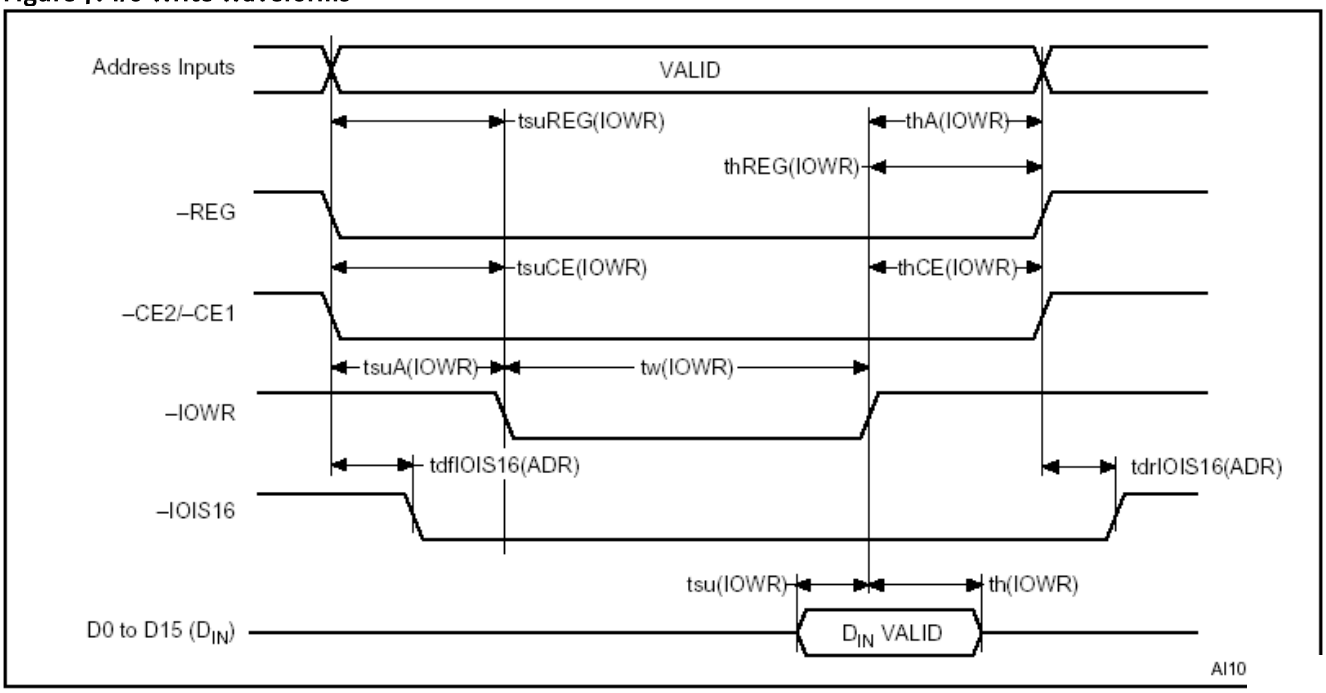


Table 24: I/O write timing

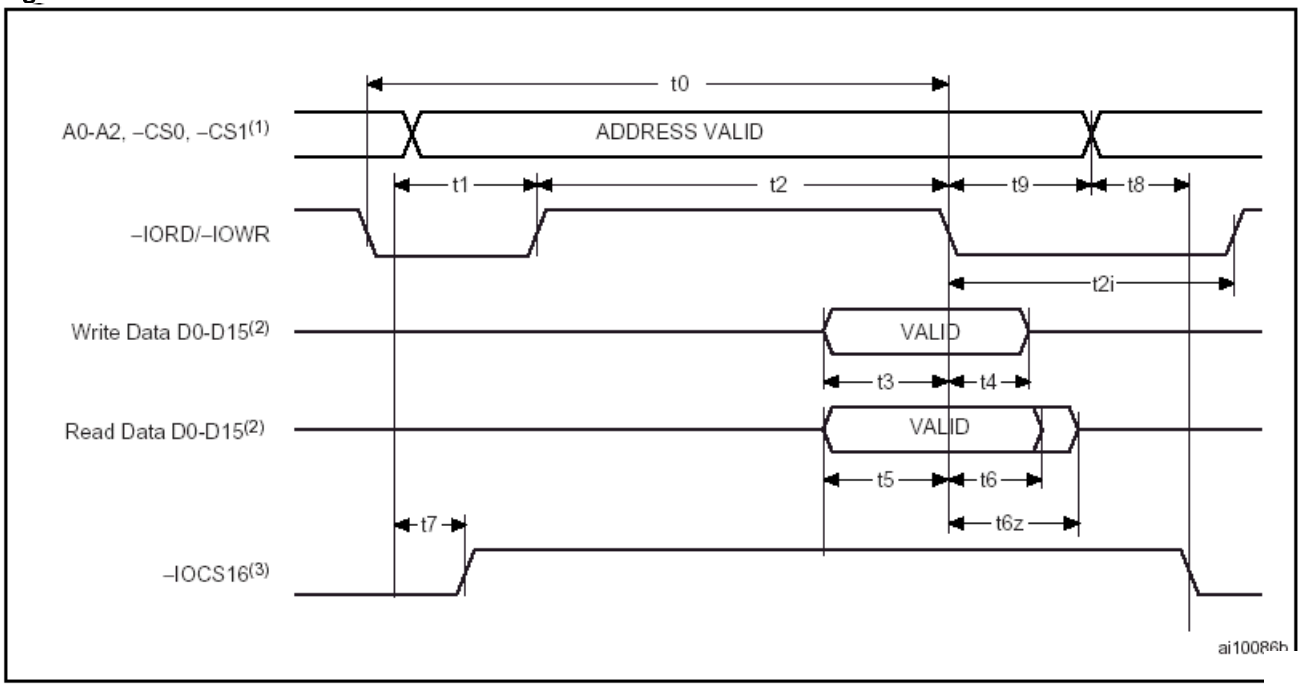
Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Addr.	tdfIOIS16(ADR)	tAVISL		35		NA(2)		NA(2)		NA(2)
IOIS16 Delay Rising from Addr.	tdrIOIS16(ADR)	tAVISH		35		NA(2)		NA(2)		NA(2)

1. D_{IN} signifies data provided by the system to the CompactFlash™ Memory Card.
2. –IOIS16 and –INPACK are not supported in this mode.

6.4 True IDE Mode

The timing waveforms for True IDE mode and True IDE DMA mode of operation in this section are drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the waveforms inverted from their electrical states on the bus.

Figure 8: True IDE PIO mode Read/Write waveforms



1. The device addresses consists of –CS0, –CS1, and A2–A0.
2. The Data I/O consist of D15–D0 (16–bit) or D7–D0 (8 bit).
3. –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

Table 25: True IDE PIO mode Read/Write timing (1)

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)	5(5) (ns)	6(5) (ns)
Cycle time (min)	t_0(2)	600	383	240	180	120	100	80
Address Valid to –IORD/–IOWR setup (min)	t_1	70	50	30	30	25	15	10
–IORD/–IOWR (min)	t_2(2)	165	125	100	80	70	65	55
–IORD/–IOWR (min) Register (8 bit)	t_2(2)	290	290	290	80	70	65	55
–IORD/–IOWR recovery time (min)	t_{2i}(2)	–	–	–	70	25	25	20
–IOWR data setup (min)	t_3	60	45	30	30	20	20	15
–IOWR data hold (min)	t_4	30	20	15	10	10	5	5
–IORD data setup (min)	t_5	50	35	20	20	20	15	10
–IORD data hold (min)	t_{6z}(3)	5	5	5	5	5	5	5
–IORD data tri–state (max)	t_7(4)	30	30	30	30	30	20	20
Address valid to –IOCS16 assertion (max)	t_8(4)	90	50	40	NA	NA	NA	NA
Address valid to –IOCS16 released (max)	t_7	60	45	30	NA	NA	NA	NA
–IORD/–IOWR to address valid hold	t_9	20	15	10	10	10	10	10

1. The maximum load on –IOCS16 is 1 LSTTL with a 50pF total load.
2. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements of to, t_2, and t_{2i} have to be met. The requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can ensure that to is equal to or greater than the value reported in the devices identify drive Card implementation should support any legal host implementation.
3. This parameter specifies the time from the falling edge of –IORD to the moment when the CompactFlash™ Memory Card (tri–state).
4. t_7 and t_8 apply only to modes 0, 1 and 2. The –IOCS16 signal is not valid for other modes.

Figure 9: True IDE Multi-Word DMA Mode Read/Write waveforms

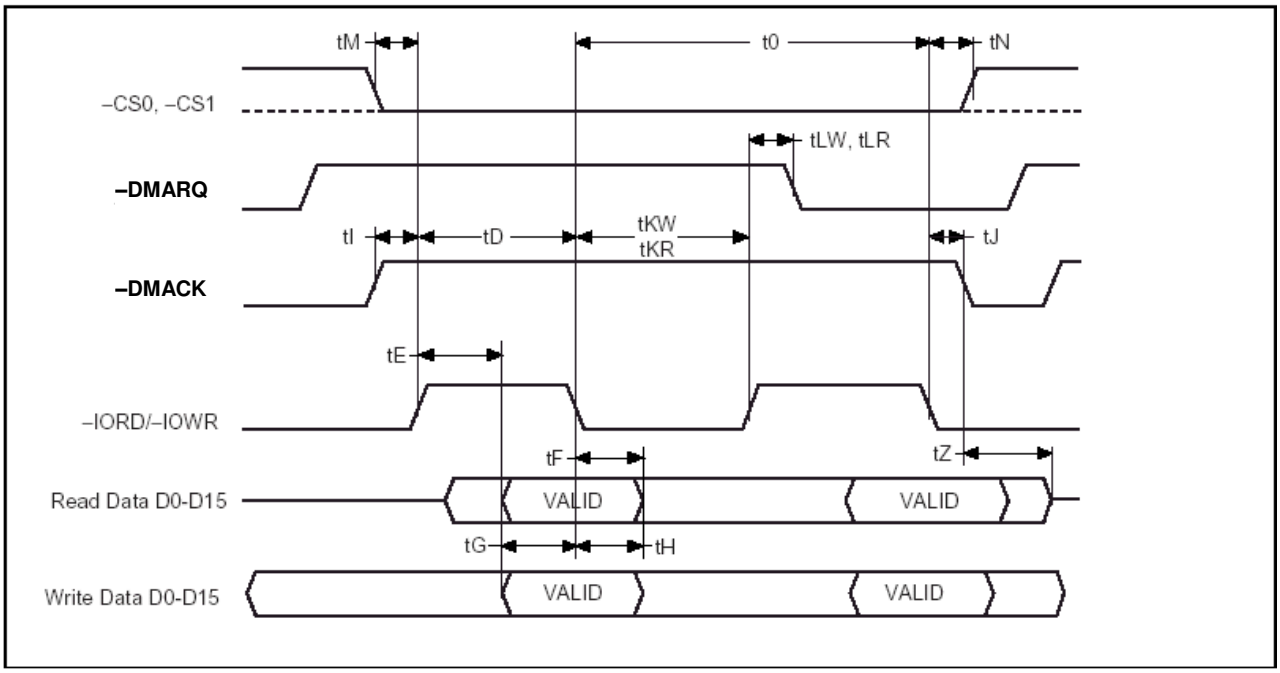


Table 26: True IDE Multi-Word DMA Mode Read/Write timing

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)
Cycle time (min)	t_0 (1)	480	150	120	100	80
-IORD / -IOWR asserted width (min)	t_D (1)	215	80	70	65	55
-IORD data access (max)	t_E	150	60	50	50	45
-IORD data hold (min)	t_F	5	5	5	5	5
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10
-IOWR data hold (min)	t_H	20	15	10	5	5
DMACK to –IORD/-IOWR setup (min)	t_I	0	0	0	0	0
-IORD / -IOWR to –DMACK hold (min)	t_J	20	5	5	5	5
-IORD Low width (min)	t_{KR} (1)	50	50	25	25	20
-IOWR Low width (min)	t_{KW} (1)	215	50	25	25	20
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35
CS(1:0) valid to –IORD / -IOWR (min)	t_M	50	30	25	10	5
CS(1:0) hold (min)	t_N	15	10	10	10	10
-DMACK (max)	t_Z	20	25	25	25	25

1. t_0 is the minimum total cycle time. T_D is the minimum command active time. T_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles, respectively. The actual cycle time is the sum of the actual command active time and the actual command inactive time. The timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be respected. T_0 is higher than t_D + t_{KR} or t_D + t_{KW}, for input and output cycles respectively. This means the host can lengthen either t_D or t_{KR}/t_{KW}, or both, to ensure that t_0 is equal to or higher than the value reported in the devices identify device data. A CompactFlash™ Storage Card implementation shall support any legal host implementation.

6.5 Ultra DMA Mode

6.5.1 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).
Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 27.