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Product data sheet

Industrial SATA SSD 2.5"

X-200 Series

SATA II - 3.0Gb/s
up to UDMA6 / MDMA2 / PIO4

Standard and industrial temperature grade

BU: Swissbit Group
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X-200 Series – Industrial SATA Solid State Drive 2.5" 4GByte to 64GByte

1 Feature summary

- Form factor:
  - 2.5-inch SATA Solid State Drive (SSD)
  - 100.2mm x 70.0mm x 9.0mm
  - Replacement of a standard SATA-compliant Hard Disk Drive
  - 7+15 pin (SATA+power) SATA connector
- Interface:
  - SATA Rev 2.6 – 3Gbit/s (1.5Gbit/s compatible)
- Highly-integrated memory controller
  - max. UDMA6 supported
  - max. PIO mode 4, MDMA2 supported
  - SLC NAND Flash
  - Hardware BCH-code ECC (8 Bit correction per sector for SLC)
  - fix drive configuration
- Low-power CMOS technology
- 5.0V ± 10% power supply (3.3V optional)
- Low Power, less than 500mA
- No mechanical noise
- Wear Leveling: active wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- High reliability
  - Best available SLC NAND Flash technology
  - MTBF > 2,500,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of connector insertions/removals: >1,000
- High performance
  - Up to 300MB/s burst transfer rate in SATA II – 3.0Gb/sec
  - Sustained Write performance: up to 95MB/s
  - Sustained Read Performance: up to 120MB/s
- Available densities
  - 4GByte up to 64GByte (SLC NAND Flash)
- S.M.A.R.T., HPA, Security and 48bit feature set
- 2 Temperature ranges
  - Commercial Temperature range 0 ... +70°C
  - Industrial Temperature range -40 ... +85°C
- Life Cycle Management
- Controlled BOM
- RoHS compatible

2 Contents

3 Order Information

3.1 Available Standard part numbers

FIX / SATA II/ PIO4, MDMA2, UDMA6 / 0°C to 70°C

Density	Part Number
4GB	SFSA4096QxBR4TO-C-MS-2y6-STD
8GB	SFSA8192QxBR4TO-C-DT-2y6-STD
16GB	SFSA16GBQxBR8TO-C-DT-2y6-STD
32GB	SFSA32GBQxBR8TO-C-QT-2y6-STD
64GB	SFSA64GBQxBR8TO-C-NC-2y6-STD

Table 1: Commercial temperature product list

x= depends on product generation, y= depends on firmware generation

FIX / SATA II/ PIO4, MDMA2, UDMA6 / -40°C to +85°C

Density	Part Number
4GB	SFSA4096QxBR4TO-I-MS-2y6-STD
8GB	SFSA8192QxBR4TO-I-DT-2y6-STD
16GB	SFSA16GBQxBR8TO-I-DT-2y6-STD
32GB	SFSA32GBQxBR8TO-I-QT-2y6-STD
64GB	SFSA64GBQxBR8TO-I-NC-2y6-STD

Table 2: Industrial temperature product list

x= depends on product generation, y= depends on firmware generation

3.2 Offered OEM options

- Customer specified drive size and drive geometry (C/H/S – cylinder/head/sector)
- Customer specified drive ID (Strings)
- Preload service (also drive images with any file system)
- ...

4 Product Specification

The Solid State Drive (SSD) is a small form factor (2.5'') non-volatile memory drive which provides high capacity data storage. It has a standard combined connector with SATA and power/control part. The card works at a supply voltage of 5V.
The drive with the SATA interface operates in Mode 2.0 (1.5 or 3.0 Gb/s burst).
The drive has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware BCH-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to detect and correct **8 random bits per 528 Bytes**.
The drive has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The specification has been realized and approved by the ATA/ATAPI-7 specification.
The system highlights are shown in Table 3 ...Table 10.

Related Documentation

- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-7)
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994

4.1 Physical description

The SSD contains a flash controller and Flash memory modules. The controller interfaces with a host system allowing data to be written to and read from the Flash memory modules.
The SSD is offered in a 2.5'' size package with a standard SATA connector. Figure 1 and Figure 2 (page 39) show SSD dimensions and connector location.

4.2 System Performance

Table 3: System Performance (measured) UDMA5

System Performance		Typ.	Max.	Unit
Data transfer Rate (SATA burst (1.5 or 3.0Gb/s))		150 or 300	300	MB/s
Sustained Sequential Read 128kB Block size	4GB	100(1)	110	
	8...16GB	110(1)	120	
	32GB	93(1)	100	
	64GB	87(1)	95	
Sustained Sequential Write 128kB Block size	4GB	46(1)	47	
	8...16GB	87(1)	95	
	32GB	76(1)	90	
	64GB	72(1)	85	
Sustained Sequential Read 4kB Block size	4GB	27(1)	28	MB/s
	8...16GB	28(1)	30	
	32GB	25(1)	28	
	64GB	23(1)	26	
Sustained Sequential Write 4kB Block size	4GB	20(1)	22	
	8...16GB	21(1)	23	
	32GB	19(1)	21	
	64GB	17(1)	19	
Sustained Random Read 4kB Block size	4...8GB	11(1)	12	MB/s
	16GB	9(1)	11	
	32GB	5.5(1)	7	
	64GB	5.0(1)	7	
Sustained Random Write 4kB Block size	4GB	0.06(1)(2)	0.09	
	8...16GB	0.05(1)(2)	0.08	
	32GB	0.05(1)(2)	0.08	
	64GB	0.05(1)(2)	0.08	

1. All values refer to Toshiba Flash chips (see part number) in UDMA5 mode (SATA 3.0Gbit/s) with Sequential write/read test (256 sectors multiple commands) and sequential and random write/read test (8 sectors multiple commands).Sustained Speed depends on flash type and number, file/cluster size, and burst speed.
2. The typical random write speed values are really random access across the whole drive. Random write values in file systems are much larger.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage	4.5V to 5.5V

Table 5: Current consumption (1)

Current Consumption (type)	5.0V	Unit
Read (typ/max)	260/320	mA
Write (typ/max)	260/310	
Sleep/Idle Mode (typ/max)	120/140	

1. All values are typical at 25° C and nominal supply voltage and refer to SATAII performance test random pattern for a 64GByte SSD.

4.3.2 Recommended Storage Conditions

Table 6: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-50°C to 100°C
Industrial Storage Temperature	-50°C to 100°C

4.3.3 Shock, Vibration, and Humidity

Table 7: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20G Peak, 10...2000Hz
Shock	1500G, 0.5ms duration, half sine wave

4.4 Physical Dimensions

Table 8: Physical Dimensions

Physical Dimensions		Unit
Length	100.20±0.2	mm
Width	69.85±0.2	
Thickness	9.00±0.1	
Weight (typ.)	90	g

4.5 Reliability

Table 9: System Reliability and Maintenance (1)

Parameter	Value
MTBF (at 25°C)	> 2,500,000 hours
Insertions/Removals	> 1,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read
Data Retention	10 years (JESD47)

1. Dependent on final system qualification data.

4.6 Drive geometry / CHS parameter

Table 10: SSD density specification

Density	Default cylinders	Default heads	Default sectors	Sectors drive	Total addressable Bytes	Remark
4GB	7,732	16	63	7,793,856	3,990,454,272	
8GB	15,498	16	63	15,621,984	7,998,455,808	
16GB	16,383*)	16	63	31,277,056	16,013,852,672	
32GB	16,383*)	16	63	62,586,880	32,044,482,560	
64GB	16,383*)	16	63	125'304'832 125'313'024	64'156'073'984 64'160'268'288	Firmware "1" Firmware "2"

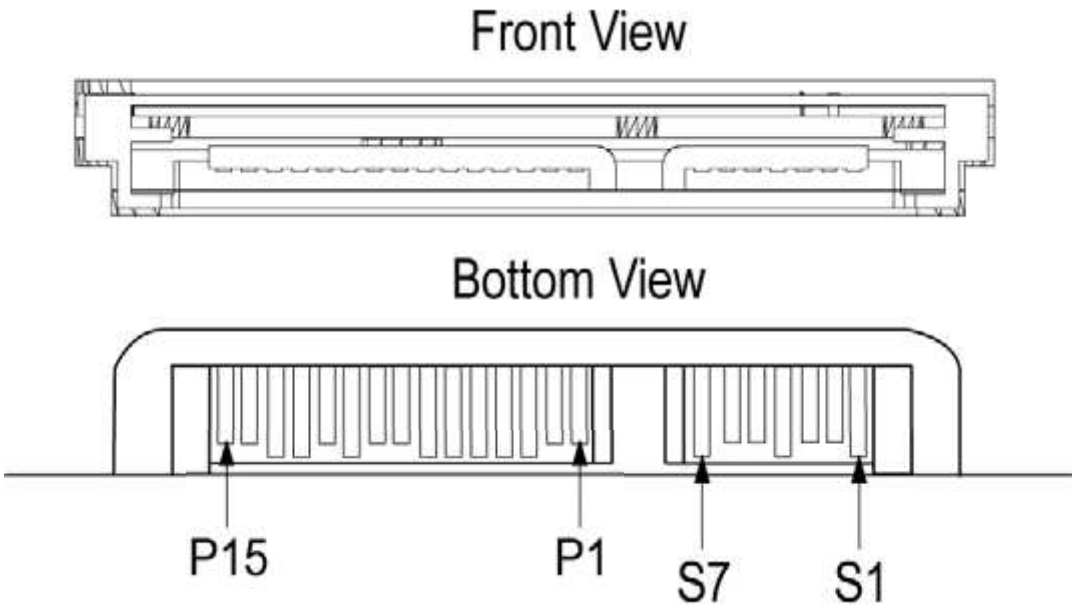
*) The CHS access is limited to about 8GB. Above 8GB the drive must be addressed in LBA mode.

5 Electrical interface

5.1 Electrical description

The SSD is connected with a standard 7 pin SATA connector and a standard 15 pin SATA power connector.

The signal/pin assignments and descriptions are listed in Table 11



The signal/pin assignments and descriptions are listed in Table 11.

Table 11: Pin Assignment, name, and description

Pin	Signal Name	Description
S1	Ground	Signal Ground
S2	A+	+ Differential Receive signal
S3	A-	- Differential Receive signal
S4	Ground	Signal Ground
S5	B-	- Differential Transmit signal
S6	B+	+ Differential Transmit signal
S7	Ground	Signal Ground
P1...P3	3.3V	3.3V power (optional on request)
P4...P6	Ground	Power Ground
P7	5V	5V precharge
P8...P9	5V	5V power
P10	Ground	Power Ground
P11	Reserved	(not used)
P12	Ground	Power Ground
P13...P15	12V	12V power(not used)

5.2 Electrical Specification

Table 12 and Table 13 define the DC Characteristics of the SSD. Unless otherwise stated, conditions are:

- Vcc = 5.0V ± 10%
- 0°C to +70°C

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 13.

Table 12: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V

Table 13: Input Power write and read

Mode	Maximum Average RMS Current	Conditions
SATA II (3.0Gb/s)	310mA	5V
SATA I (1.5Gb/s)	240mA	
Idle	120mA	

6 ATA command description

This section provides information on the ATA commands supported by the SSD. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register.

ATA Command Flow

DDMAI0: DMA_in State This state is activated when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command. When in this state, the device shall prepare the data for transfer of a data FIS to the host.

Transition DDMAI0:1 When the device has the data ready to transfer a data FIS, the device shalltransition to the DDMAI1: Send_data state. Transition DDMAI0:2 When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.

DDMAI1: Send_data This state is activated when the device has the data ready to transfer a data FIS to the host. When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2,048 Dwords (8KB).

Transition DDMAI1:1 When the data FIS has been transferred, the device shall transition to the DMA0I0: DMA_in state.

DDMAI2: Send_status This state is activated when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data. When in this state, the device shall request that the Transport layer transmit a Register FIS with the register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DDMAI2:1 When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 14 summarizes the Drive command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 14: ATA Command Set[1]

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5h or 98h					D	
Erase Sector(s) (CFA)	C0h		Y	Y	Y	Y	Y
Execute Drive Diagnostic	90h					D	
Flush cache	E7h					D	
Identify Drive	ECh					D	
Idle	E3h or 97h		Y			D	
Idle Immediate	E1h or 95h					D	
NOP	00h					D	
Read Buffer	E4h					D	
Read DMA	C8		Y	Y	Y	Y	Y
Read Multiple	C4h		Y	Y	Y	Y	Y
Read native max address	F8h					D	
Read Sector(s)	20h		Y	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
Request Sense (CFA)	03h					D	
Security Disable Password	F6h					D	
Security Erase Prepare	F3h					D	
Security Erase Unit	F4h					D	
Security Freeze Lock	F5h					D	
Security Set Password	F1h					D	
Security Unlock	F2h					D	
Set Features	EFh	Y				D	
Set max address (with set password)	F9h		Y	Y	Y	Y	Y
Set Multiple Mode	C6h		Y			D	
Sleep	E6h or 99h					D	
S.M.A.R.T.	B0h	Y	Y		Y	D	
Standby	E2h or 96h					D	
Standby Immediate	E0h or 94h					D	
Translate Sector (CFA)	87h		Y	Y	Y	Y	Y
Write Buffer	E8h					D	
Write DMA	CA		Y	Y	Y	Y	Y
Write Multiple	C5h		Y	Y	Y	Y	Y
Write Multiple w/o Erase (CFA)	CDh		Y	Y	Y	Y	Y
Write Sector(s)	30h		Y	Y	Y	Y	Y
Write Sector(s) w/o Erase (CFA)	38h		Y	Y	Y	Y	Y

1. FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers,
DH = Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use),
Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Drive and head parameters are used.
D – only the Drive parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

6.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Drive is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Drive is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 15 defines the Byte sequence of the Check Power Mode command.

Table 15: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.2 Erase Sector(s) (C0h)

This command is used to pre-erase and condition data sectors prior to a Write Sector without Erase command or a Write Multiple Without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur. Table 16 defines the Byte sequence of the Erase Sector command.

Table 16: Erase Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to erase							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to erase							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

6.3 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Drive.
The Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 17 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 18 are returned in the Error Register at the end of the command.

Table 17: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 18: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error

6.4 Flush Cache (E7h)

This command causes the drive to complete writing data from its cache. The drive returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the drive does not support the Flush Cache command, the drive shall return command aborted.

Table 19: Flush Cache

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E7h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.5 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the Drive. This command has the same protocol as the Read Sector(s) command. Table 20 defines the Identify Device command Byte sequence. All reserved bits or Words are zero. shows the definition of each field in the Identify Drive Information.

Table 20: Identify Device

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 21: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	**044Ah***	2	Standard Configuration FIX (optional 848Ah for removable)
1	XXXXh	2	Default number of cylinders (obsolete)
2	0000h	2	Reserved
3	00XXh	2	Default number of heads (obsolete)
4	0000h	2	Obsolete
5	XXXXh	2	Obsolete
6	XXXXh	2	Default number of sectors per track (obsolete)
7-8	XXXXh	4	Number of sectors per Drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Buffer type (dual ported multi-sector) retired
21	0002h*	2	Buffer Size in 512byte increment (obsolete)
22	000Xh	2	Reserved
23-26	**YYYY***	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	**YYYY***	40	Model number in ASCII (right justified ("SFSAxxxxQxBRxxx-x-xx-xxx-xxx")
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double word not supported
49	**0F00h*** **0E00h***	2	Capabilities with DMA, LBA, IORDY supported without DMA LBA, IORDY supported
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Obsolete
53	**0007h***	2	Field validity (Bytes 54-58, 64-70, 88)
54	XXXXh	2	Current numbers of cylinders (obsolete)
55	XXXXh	2	Current numbers of heads (obsolete)
56	XXXXh	2	Current sectors per track (obsolete)
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) (obsolete)
59	010Xh*	2	Multiple sector setting (can be changed by host).
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Obsolete
63	**0007h*** **0000h***	2	Multi-Word DMA transfer support and selection (can be changed by host). no multi-word DMA
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	0078h*	2	Minimum Multi-Word DMA transfer cycle time per Word.
66	0078h*	2	Recommended Multi-Word DMA transfer cycle time.
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69-75	0000h	14	Reserved
76	0006h	2	SATA Capabilities
77	0000h	2	Reserved
78	0008h	2	SATA Feature support
79	0000h*	2	SATA Features enabled (can be changed by host)
80-81	0080h 0000h	4	ATA/ATAPI version 7
82 -84	742Bh* 5500h* 4002h*	6	Features/command sets supported
85-87	7429h* 1400h* 4002h*	6	Features/command sets enabled (can change in operation)
88	**207F***	2	UDMA Mode Supported 0,1,2,3,4,5,6 and Selected 5 (changes in operation)
89	0003*	2	Time for security erase unit completion (e.g. 6 minutes)
90-91	0000h*	4	Reserved
92	**FFFE***	2	Master Password Revision Code
93-127	0000h*	70	Reserved
128	0001h*	2	Security Status (changes in operation)
129-159	XXXXh	62	Vendor specific (e.g."Swissbit SSD")
160	0000h*	2	Max. current
161-216	0000h	112	Reserved
217	0001h*	2	Nominal Media Rotation Rate: Solid State Device
218-255	0000h	76	Reserved

* Standard values for full functionality, depending on configuration
XXXX Depending on drive capacity and drive geometry
YYYY Depending on drive configuration

6.5.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **045Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the drive as the root storage device.

6.5.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.5.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.5.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.5.5 Word 7-8: Number of Sectors per Drive

This field contains the number of sectors per Drive. This double Word value is also the first invalid address in LBA translation mode.

6.5.6 Word 10-19: Memory Drive Serial Number

The contents of this field are right justified and padded without spaces (20h).

6.5.7 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.5.8 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.5.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.5.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 11: IORDY Supported
  If bit 11 is set to 1 then this drive supports IORDY operation.
  If bit 11 is set to 0 then this drive may support IORDY operation.
- Bit 10: IORDY may be disabled
  If bit 10 is set to 1 then IODRDY may be disabled.
- Bit 9 LBA support: drive support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

6.5.11 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15-8: are set to 02H.

6.5.12 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported UDMA

6.5.13 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.5.14 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

6.5.15 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

6.5.16 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Drive in LBA mode only.

6.5.17 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the drive to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
Selection of Multiword DMA modes 3 and above are specific to Drive are as described in Word 163.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the drive to indicate the Multiword DMA modes it is capable of supporting.
Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the drive supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the drive supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the Drive supports Multiword DMA modes 2, 1 and 0.
Support for Multiword DMA modes 3 and above are specific to Drive are reported in word 163 as described in Word 163.

6.5.18 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the drive to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the Drive supports PIO mode 4.
- Bit 0 is set to '1' to indicate that the Drive supports PIO mode 3.

Support for PIO modes 5 and above are specific to Drive are reported in word 163 as described in Word 163.

6.5.19 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.5.20 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the Drive will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.5.21 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer without utilization of flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.5.22 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the Drive supports while performing data transfers while utilizing IORDY flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the Drive.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.5.23 Word 76: Serial ATA Capabilities

- Bit 15:11 Reserved
- Bit 10 1 = Supports Phy Event Counters
- Bit 9 1 = Supports receipt of host initiated power management requests
- Bit 8 1 = Supports native Command Queuing
- Bit 7:3 Reserved for future SATA signaling speed grades
- Bit 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
- Bit 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
- Bit 0 Shall be cleared to zero

6.5.24 Word 78: SATA Feature support

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation
- Bit 5 1 = Supports asynchronous notification
- Bit 4 1 = Supports in-order data delivery
- Bit 3 1 = Device supports initiating interface power managment
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization
- Bit 1 1 = Supports non-zero buffer offsets
- Bit 0 Shall be cleared to zero

6.5.25 Word 79: SATA Features enabled

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation enabled
- Bit 5 1 = Supports asynchronous notification enabled
- Bit 4 1 = Supports in-order data delivery enabled
- Bit 3 1 = Device supports initiating interface power managment enabled
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization enabled
- Bit 1 1 = Supports non-zero buffer offsets enabled
- Bit 0 Shall be cleared to zero

6.5.26 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
- If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
- Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
- If bit 5 of word 82 is set to one, write cache is supported.
- If bit 6 of word 82 is set to one, look-ahead is supported.
- Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
- Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
- Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 82 is obsolete.
- Bit 12 of word 82 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 82 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 82 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 82 is obsolete.

- Bit 0 of word 83 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 83 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- Bit 2 of word 83 shall be set to zero; the Drive does not support the CFA feature set.
- If bit 3 of word 83 is set to one, the Drive supports the Advanced Power Management feature set.
- Bit 4 of word 83 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.5.27 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
- If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security
- Set Password command.
- Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
- If bit 5 of word 85 is set to one, write cache is enabled.
- If bit 6 of word 85 is set to one, look-ahead is enabled.
- Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
- Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
- Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 85 is obsolete.
- Bit 12 of word 85 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 85 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 85 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 85 is obsolete.
- Bit 0 of word 86 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 86 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.

- If bit 2 of word 86 shall be set to zero, the Drive does not support the CFA feature set.
- If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
- Bit 4 of word 86 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.5.28 Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device does not support UDMA.

- Bit 15: Reserved
- Bit 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7: Reserved
- Bit 6: 1 = Ultra DMA mode 6 and below are supported. Bits 0-5 shall be set to 1.
- Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 shall be set to 1.
- Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
- Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
- Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
- Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0: 1 = Ultra DMA mode 0 is supported

6.5.29 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete. Support of this word is mandatory if the Security feature set is supported.
Required Time=(Value*2) minutes

6.5.30 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision is not supported. Support of this word is mandatory if the Security feature set is supported.

6.5.31 Word 128: Security status

Support of this word is mandatory if the Security feature set is supported.
Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.
Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.
Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hardware reset.
Bit 3 of word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.
Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.
Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.
Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

6.6 Idle (97h or E3h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 22 defines the Byte sequence of the Idle command.

Table 22: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

6.7 Idle Immediate (95h or E1h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 23 defines the Idle Immediate command Byte sequence.

Table 23: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.8 NOP (00h)

This command always fails with the Drive returning command aborted. Table 24 defines the Byte sequence of the NOP command.

Table 24: NOP

Task File Register	7	6	5	4	3	2	1	0
COMMAND	00h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.9 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Drive's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 25 defines the Read Buffer command Byte sequence.

Table 25: Read buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.10 Read DMA (C8h)

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The Drive asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and
asserts -IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

Table 26: Read DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.11 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error.

Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.
Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 27 defines the Read Multiple command Byte sequence.

Table 27: Read Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.12 Read Native max address (F8h)

The Read Native max address command reads the max native address of the drive. It is related to the Host protected Area feature set. Table 28 defines the Read max native address command Byte sequence.

Table 28: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.
The native drive size is given in Drive/Head, Cyl Hi, Cyl Low and Sector num register as LBA value.

6.13 Read Sector(s) (20h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Drive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 29 defines the Read Sector command Byte sequence.

Table 29: Read sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.14 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Drive sets BSY. When the requested sectors have been verified, the Drive clears BSY and generates an interrupt.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 30 defines the Read Verify Sector command Byte sequence.

Table 30: Read Verify Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h or 41h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.15 Request Sense (03h)

This command requests extended error information for the previous command. Table 31 defines the Request Sense command Byte sequence.
Table 32 defines the valid extended error codes. The extended error code is returned to the host in the Error Register.

Table 31: Request sense

Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 32: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

6.16 Security Disable Password (F6h)

This command requests a transfer of a single sector of data from the host. Table 33 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 33: Security Disable Password

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F6h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 34: Security Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

6.17 Security Erase Prepare (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable device erasing and unlocking. This command prevents accidental erase of the SSD.

Table 35: Security Erase Prepare

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F3h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.18 Security Erase Unit (F4h)

This command requests transfer of a single sector of data from the host. Table 34 defines the content of this sector of information. If the password does not match the password previously saved by the SSD, the SSD rejects the command with command aborted. The Security Erase Prepare command shall be completed immediately prior to the Security Erase Unit command. If the SSD receives a Security Erase Unit command without an immediately prior Security Erase Prepare command, the SSD aborts the Security Erase Unit command.

Table 36: Security Erase Unit

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F4h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.19 Security Freeze Lock (F5h)

The Security Freeze Lock command sets the SSD to Frozen mode. After command completion, any other commands that update the SSD Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security Freeze Lock is issued when the SSD is in Frozen mode, the command executes and the SSD remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0.
Commands disabled by Security Freeze Lock are:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

If security mode feature set is not supported, this command shall be handled as Wear Level command.

Table 37: Security Freeze Lock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							