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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SI-7321M Motor Driver IC

Introduction

This document describes the function and features of SI-7321M, a unipolar 2-phase stepping motor driver IC. This device uses PWM constant current-control, and provides user-configurable sequencer parameters. The clock-in type input interface allows simplified control logic, and options for built-in sense current detection and load circuit short or open protection (patent pending) provide lower loss. Lower thermal resistance results from the innovative multi-chip internal structure, which separates the main control IC (MIC) from the four heat-generating MOSFETs, and places wide output terminals at package corners to enhance thermal dissipation. The built-in excitation distribution circuit (sequencer) allows motor control using only the Clock signal for simple operations (forward, reverse, brake, coast, hold), with motor speed control by frequency input into Clock pin, and rotation direction control by a dedicated logic input. This eliminates logic signal lines required for conventional phase-input methods, and reduces demand on heavily-used CPUs.

Features and benefits include the following:

- Power supply voltage, V_{BB}, 46 V maximum, 10 to 44 V normal operating range
- Logic supply voltage, V_{DD}, 3.3 to 5.5 V
- Maximum output current: 1.5 A
- Four NMOS output MOSFETs, $R_{DS(on)}$ = 0.25 Ω typical
- Built-in sequencer
- Simplified clock-in stepping control
- Full- and half-stepping and $^1/_4$, $^1/_8$, and $^1/_{16}$ microstepping
- Surface mount type 44-pin molded package for automatic assembly and low profile
- Self-excitation PWM current control with fixed off-time
- Microstepping off-time adjusted automatically by step reference current ratio
- Built-in synchronous rectifying circuit reduces losses at PWM switch-off
- Synchronous PWM chopping function prevents motor noise in Hold mode

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

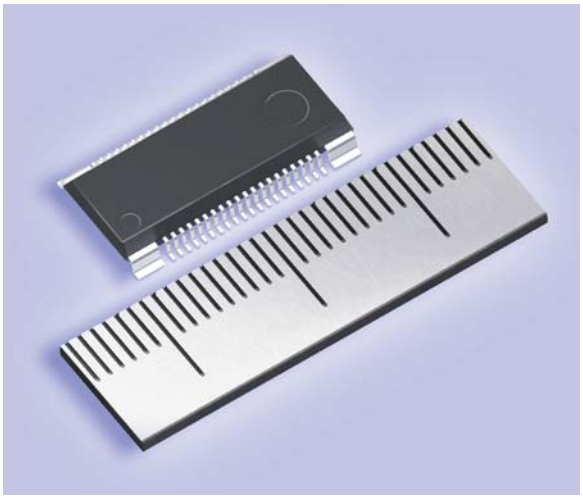

Figure 1. The HSOP is a fully molded, low-profile (2.3 mm overall height), 44-pin HSOP surface-mount package with four enlarged pins for enhanced thermal dissipation. Configuration is suitable for automated placement on application PCBs.

- Built-in current sensing for each phase, set externally
- Dual sleep modes reduce IC input current in stand-by state
- Built-in protection against motor coil opens and shorts
- User-configurable operation options, set by external logic input:
  - Blanking time: 1.8 µs or 3.6 µs
  - Sequencer timing on Clock input rising (POS) edge or both rising and falling (POS/NEG) edges
  - Protection features enable or disable

Applications include printers, copiers, ticket-vending machines, ATMs, and industrial robots.

Contents

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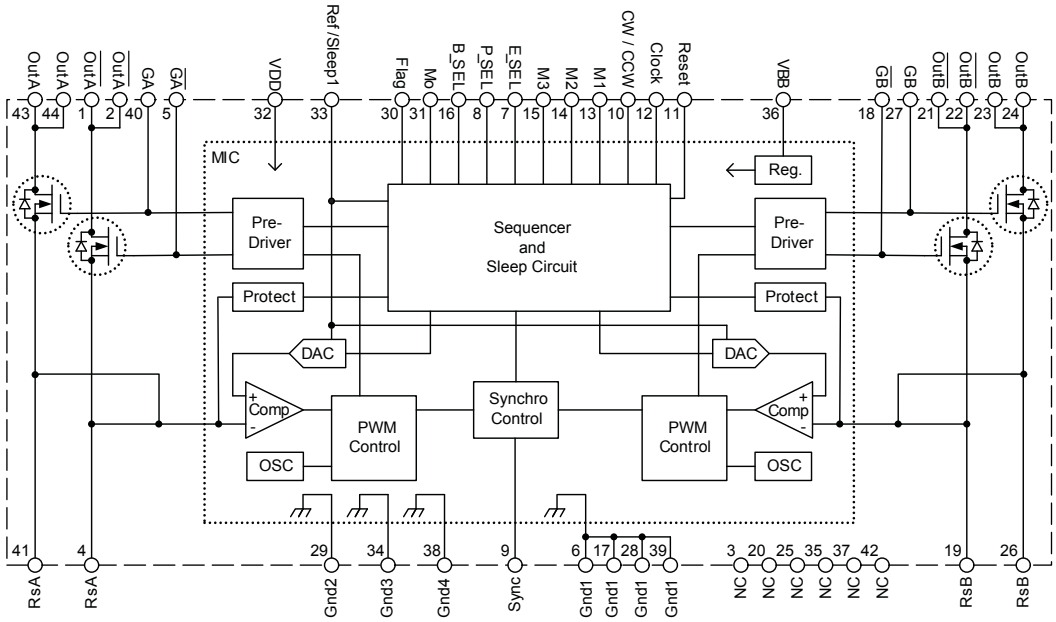
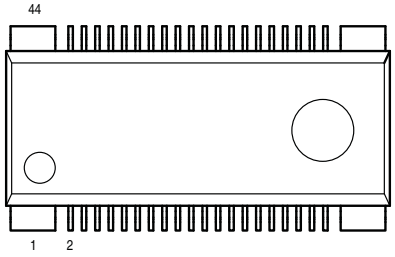
Functional Block Diagram



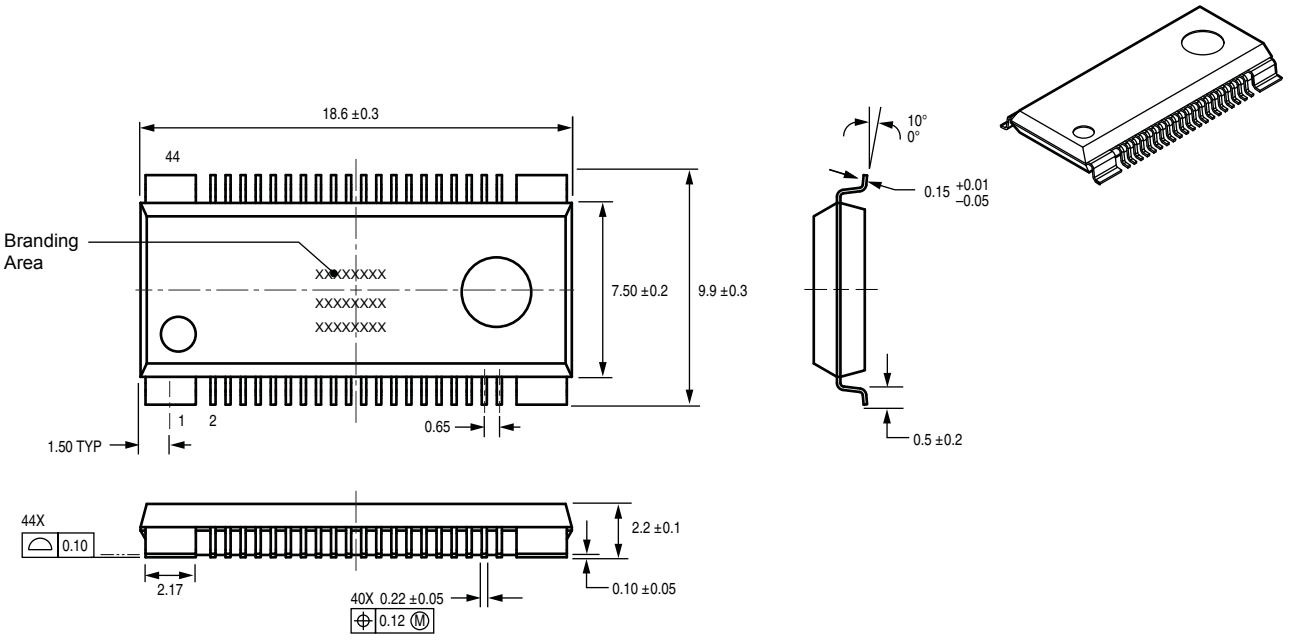
Pin-out Diagram



Terminal List Table

Number	Name	Function	Number	Name	Function
1	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$	23	OutB	Output of phase B
2	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$	24	OutB	Output of phase B
3	NC	Non connected pin	25	NC	Non connected pin
4	RsA	Phase A sense resistor connection	26	RsB	Phase B sense resistor connection
5	$\overline{\text{GA}}$	Phase $\overline{\text{A}}$ MOSFET Gate	27	GB	Phase B MOSFET gate
6	Gnd1	Gnd1	28	Gnd1	Gnd1
7	E_SEL	Edge select input	29	Gnd2	Gnd2
8	P_SEL	Protection enable/disable input	30	Flag	Output of protection circuit monitor
9	Sync	PWM control switch input	31	Mo	Output from monitor of 2-phase excitation status
10	CW/CCW	Sequence rotation switch	32	VDD	Power supply to logic
11	Reset	Reset for internal logic	33	Ref/Sleep1	V_{REF} PWM control input / Sleep1 enable input
12	Clock	Stepping clock input	34	Gnd3	Gnd3
13	M1	Commutation and Sleep2 setting	35	NC	Non connected pin
14	M2		36	VBB	Main power supply (for motor)
15	M3		37	NC	Non connected pin
16	B_SEL	Blanking time select input	38	Gnd4	Gnd4
17	Gnd1	Gnd1	39	Gnd1	Gnd1
18	$\overline{\text{GB}}$	Phase $\overline{\text{A}}$ MOSFET Gate	40	GA	Phase A MOSFET gate
19	RsB	Phase $\overline{\text{B}}$ sense resistor connection	41	RsA	Phase A sense resistor connection
20	NC	Non connected pin	42	NC	Non connected pin
21	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$	43	OutA	Output of phase A
22	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$	44	OutA	Output of phase A

Package Outline Drawing



Terminal core material: Cu
Terminal treatment: Ni plating and Pb-free solder dip
Package: HSOP-44

Dimensions in millimeters

Branding codes (exact appearance at manufacturer discretion):
1st line, type: SI7321M
2nd line, lot: *YMW*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
W is the week
3rd line, tracking code: *NNNN*

Device composition 100% lead (Pb) free

Functional Description

This section provides a description of the main features of the SI-7321M.

Control Logic Overview

The control logic is integrated in a single IC, the main IC (MIC) for high reliability and stability. The MIC also drives the four DMOS output MOSFETS, which control the current flow into the motor in accordance with signals from the MIC.

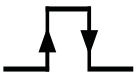
There are two drive phases, each with a pair of outputs. The drive structure is identical to that of the SLA7070M family. It provides operation in the following modes:

- PWM mode current level-controlled stepping and microstepping
- Commutation mode for continuous high-speed operation
- Hold mode for stopping motor rotation while continuing to supplying current into a motor, with the SI-7321M powered
- Two sleep modes: Sleep1 in which logic circuits respond to inputs, and Sleep2 in which the logic interface also shuts down

Sequencer Logic The single Clock input is used for step timing. Motor rotation direction is controlled by the CW/CCW input. In PWM stepping modes, each pair of outputs is controlled by a fixed off-time PWM current-control circuit. The internal oscillators (OSC in the Functional Block diagram) set the PWM fixed off-time. In high-speed rotation Commutation mode, current ratios are controlled by the combination of the M1, M2, and M3 input logic levels. For details, refer to tables 1 and 2 and figure1.

The low pass filter incorporated with the logic input pins (Reset, Clock, CW/CCW, M1, M2, M3, and Sync) improves noise rejection. The logic inputs are CMOS input compatible, and therefore they are in high impedance state. Use the IC at fixed input low and high logic levels.

Table 1. Truth Table for Common Input Pins

Pin Name	Logic Level	
	Low	High
Reset	Normal operation	Logic reset
CW/CCW	Forward	Reverse
M1	Commutation / Sleep2 function (see table 2)	
M2		
M3		
Ref/Sleep1	Normal operation / Sleep1 function (see Reference Voltage Ranges section)	
Sync	Asynchronous PWM control	Synchronous PWM control
B_SEL	Short Blanking Time (1.8 µs)	Long Blanking Time (3.6 µs)
E_SEL	Clock input: POS/NEG edge 	Clock input: POS edge 
P_SEL	Protection circuits enabled	Protection circuits disabled

Input Logic Timing

This device includes clock-in type of control that simplifies the interface.

Clock Input There are two options for applying Clock inputs: POS edge and POS/NEG edge, as shown in table 1 and figure 1. Setting the E_SEL pin high selects POS edge clocking, and E_SEL low selects POS/NEG clocking. In POS clocking, a low-to-high transition on the Clock input indexes the translator/sequencer. In POS/NEG clocking, low-to-high and high-to-low transitions index the translator/sequencer.

Clock pulse width should be set to more than 2 µs in both positive and negative polarities. Therefore, Clock response frequency is 250 kHz.

Reset Input The RESET input sets the translator/sequencer logic to a predefined home state and turns off all of the MOSFET outputs. The Reset function is asynchronous (see Synchronous Operation section).

If the input on the Reset pin is high, the internal logic circuit is reset. At this point, if the Ref/Sleep1 pin stays low, then the MOSFET outputs turn on at the starting point of excitation. Note that by default the protection circuits are enabled by a reset.

Table 2. Truth Table for Commutation/Sleep2 Function

Input Pins			Operation Mode		Current Ratio Mode
M1	M2	M3	Phases*	Stepping	
L	L	L	2	Full	8 only
H	L	L	2	Full	F only
L	H	L	1-2	Half	8, F
H	H	L	1-2	Half	F
L	L	H	W1-2	Quarter	4, 8, C, F
H	L	H	2W1-2	Eighth	2, 4, 6, 8, A, C, E, F
L	H	H	4W1-2	Sixteenth	1 through F
H	H	H	Sleep2 Mode Enable		–

*W = double

The Reset pulse width (the high pulse level hold time) should be greater than the 2 µs Clock input pulse width. A low pass filter is incorporated into the Reset circuit; therefore, a greater than 5 µs delay is required between the falling edge of the Reset input and the rising edge of the next Clock input.

CW / CCW, M1, M2, and M3 Inputs Logic inputs CW / CCW, M1, M2, and M3 set the translator step direction (CW / CCW) and step mode (M1, M2, and M3), as shown in tables 1 and 2. Changes to these inputs do not take effect until the next Clock edge (rising if POS option selected, either rising or falling if POS/NEG selected).

Logic changes are allowed either before or after Clock edges, but provide a 1 µs minimum delay both before and after adjacent Clock edges, as setup and hold times (refer to figure 1). The sequencer logic circuitry might malfunction if the logic polarity is changed during these setup and hold times. Note that, depending on the type and state of a motor, there may be anomalies in motor operation. A thorough evaluation on the sequence timing should be carried out with the application.

Synchronous Operation This function prevents occasional motor noise during Hold mode, which normally results from asynchronous PWM operation of both motor phases. A logic high at the Sync input selects synchronous operation. A logic low selects asynchronous operation.

The use of synchronous operation during rotation in Commutation mode is not recommended because it produces less motor torque and can cause motor vibration due to staircase current. The use of synchronous operation when the motor is not in continuous rotation is allowed only in full- and half-step sequence timing, due to the difference in the current controlled and PWM off-time at other stepping rates.

The Sync function is active only during 2-Phase Excitation timing. (2-Phase Excitation timing is enabled when the step reference current ratios of both phase A and phase B are in Mode 8.) If this function were available in any other timing, the overall balance might collapse because PWM off-time and the set current are different in each phase A and phase B control scenario.

DACs (D-to-A Converter) Operation During microstepping, the current level for each step is set by the value of the external sense resistor for that phase (R_{SExtx}), a reference voltage (V_{REF}, on the Ref/Sleep1 pin), and the output voltage of the internal DACs, controlled by the output of the translator / sequencer. Refer to the Step Sequencing Charts section for more information.

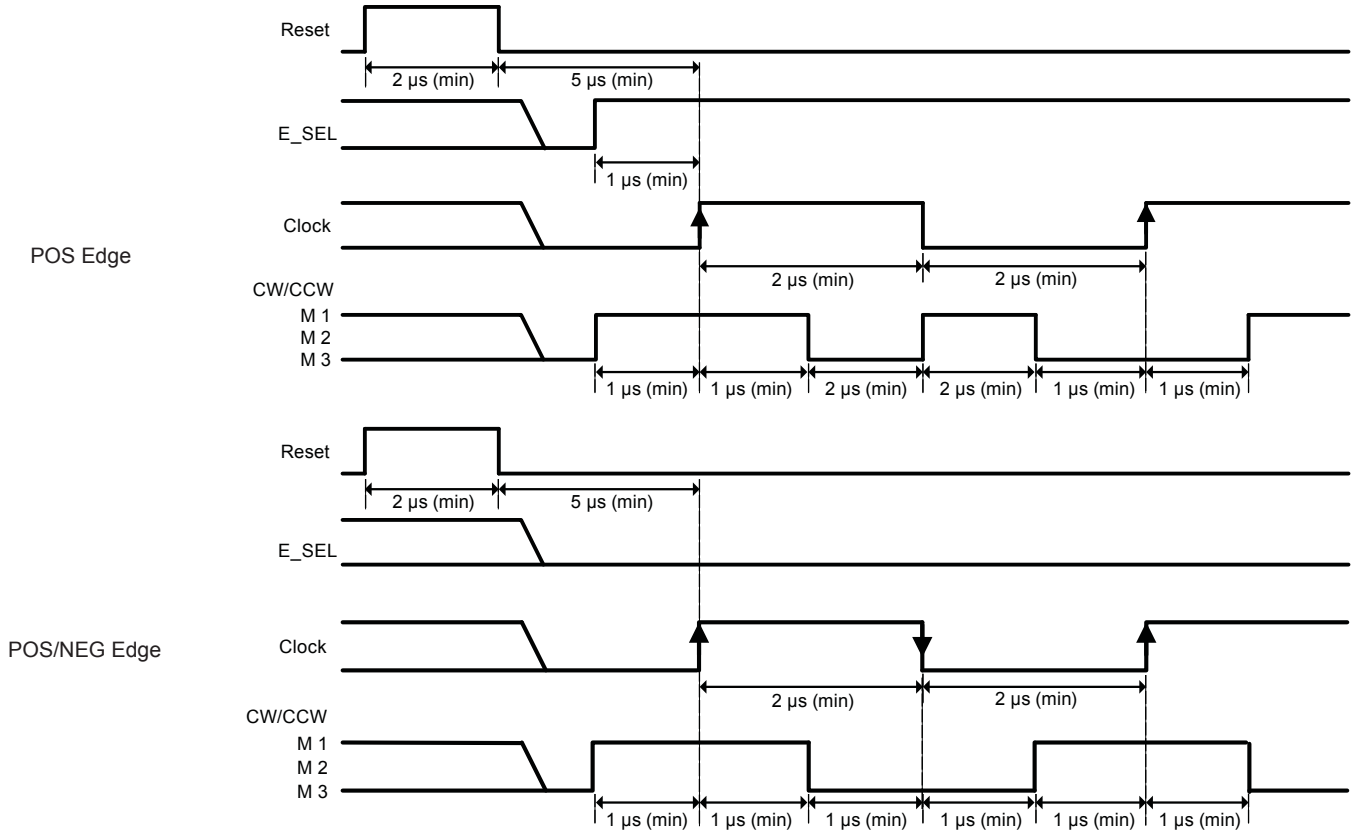


Figure 1. Step timing options. POS/NEG timing allows Clock edge to indexing logic pin settings twice in each Clock period

Regulator Circuit An integrated regulator circuit is used in driving the output MOSFET gates and powering other internal linear circuits.

Sleep Functions There are two low-power sleep modes available in the SI-7321M. These set load supply current, I_{BB}, to 100 µA (max), and disable the MOSFET outputs.

- Sleep1 mode is used to minimize power consumption when the SI-7321M is not in use. Although it disables much of the internal circuitry, including the output MOSFETs and regulator, the translator/sequencer circuit is active and logic circuits operate according to input signals. Therefore, during the Sleep1 function, a signal from an external microcontroller can set the step starting point for the next operation. Sleep1 is enabled during normal operation by a logic high at the Ref/Sleep1 pin (V_{REF}). Normal operation is restored by setting V_{REF} low. A delay of 100 µs is required before sending the initial Clock pulse after emerging from Sleep1.
- Sleep2 mode is used to further reduce power consumption by also deactivating the translator/sequencer, in addition to the the output MOSFETs and regulator. This puts the SI-7321M into a stand-by state during which logic inputs are ignored and the internal logic states remain in the same state as when Sleep2 began. Sleep2 is enabled from normal operation by setting the three Mx pins high, and then setting V_{REF} low. Normal operation is restored by setting V_{REF} high. A delay of 100 µs is required before sending the initial Clock pulse after emerging from Sleep2.

Reference Voltage Ranges The reference voltage, V_{REF} (applied on the Ref/Sleep1 pin), is used for setting the motor drive current level and for Sleep mode settings (see the Sleep Functions section). When in normal operating mode, applying V_{REF} > 2.0 V (logic high) activates Sleep1 mode. If the IC is in normal operation mode and the three Mx pins have been set high, applying a logic low enables Sleep2 mode. If the SI-7321M is already in Sleep2 mode, applying logic high restores the IC to normal operation.

V_{REF} should be less than 1.5 V for setting motor current in normal operation. As shown in figure 2, to prevent inadvertently causing a Sleep logic event, a guard band should be maintained between logic high and logic low ranges. If the protection functions are enabled (via the P_SEL pin), it is necessary to take into consideration the voltage threshold for overcurrent protection (OCP), 0.7 V. The V_{REF} guard band should be extended to provide a margin below V_{OVP}, such as restricting motor current setting voltages to less than 0.5 V.

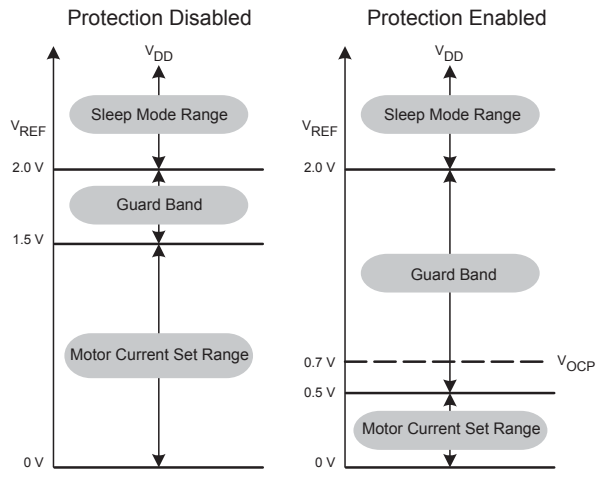


Figure 2. Reference voltage, V_{REF}, ranges

Monitor Outputs The Mo pin and the Flag pin are used to indicate the operating status of the SI-7321M, as shown in table 3.

Protection Functions

The SI-7321M includes motor coil short-circuit and motor coil open protection circuits. Protection functions are enabled by setting the P_SEL pin to logic low, and disabled by setting the P_SEL pin high.

When enabled, protection is activated by sensing voltage on the Rsx inputs, with the threshold level determined by external sense resistors, R_{SExtx}. Therefore, an overcurrent condition cannot be detected which results from the OUTx pins or Rsx pins, or both, shorting to Gnd.

Protection against motor coil opens is available only during PWM operation. Therefore, it does not work in Commutation mode constant voltage driving, when the motor is rotating at high speed.

Operation of the protection circuit disables all of the MOSFET outputs. The Flag pin is set to logic high. To come out of protection mode, cycle the logic supply, V_{DD}.

The protection functions are described as follows:

- Motor Coil (Load) Short-Circuit. This overcurrent protection (OCP) circuit begins to operate when the SI-7321M detects an

Table 3. Truth Table for Monitor Outputs

Pin Name	Low Level	High Level
Mo	Not operating in 2-Phase Excitation	Operating in 2-Phase Excitation
Flag	Normal operation	Protection circuit operating

increase in the Rsx input voltage level. The voltage at which motor coil short-circuit protection starts its operation, V_{OCP}, is set at approximately 0.7 V. In order for the motor coil short-circuit protection circuit to operate, V_{RSx} must be greater than V_{OCP}. Excessive current that flows without passing the external sense resistors (R_{SEextx}) is undetectable. The function is shown in figure 3.

- Motor Coil (Load) Open. Details of this function is not disclosed yet due to our patent policy (patent pending).

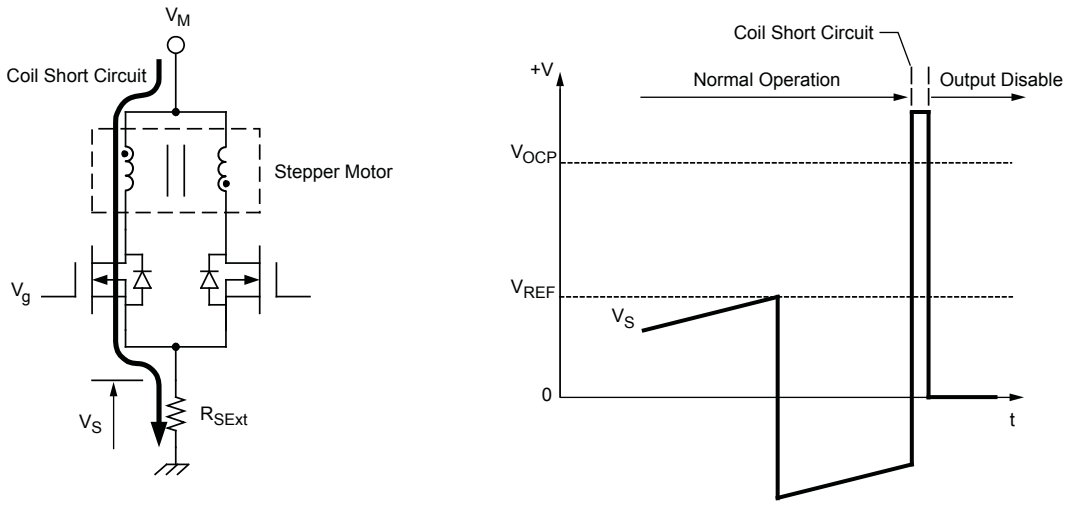


Figure 3. Motor coil short circuit protection circuit operation. Overcurrent that flows without passing the sense resistor is undetectable. To recover the circuit after protection operates, VDD must be cycled and started up again.

PWM Current Control

Blanking Time The actual operating waveforms on the Rs*x* pins when driving a motor are shown in figure 1. Immediately after PWM turns off, ringing (or spike) noise on the Rs*x* pins is observed for a few microseconds. Ringing noise can be generated by various causes, such as capacitance between motor coils and inappropriate motor wiring.

Each pair of outputs is controlled by a fixed off-time (7.5 to 13 µs, depending on stepping mode) PWM current-control circuit that limits the load current to a target value, I_{TRIP}. Initially, an output is enabled and current flows through the motor winding and the current-sense resistors. When the voltage across the current-sense resistor equals the DAC output voltage, V_{TRIP}, the current-sense comparator resets the PWM latch. This turns off the driver for the fixed off-time, during which the load inductance causes the current to recirculate for the off-time period. Therefore, if the ringing noise on the sense resistor equals and surpasses V_{TRIP}, PWM turns off.

To prevent this phenomenon, the blanking time is set to override signals from the current-sense comparator for a certain period right after PWM turns on (figure 2).

Blanking Time and Seeking Phenomenon By shortening blanking time, current control can be improved, but the ability to prevent ringing noise will be reduced, and a seeking phenomenon might occur, shown in figure 3. As a countermeasure against the seeking phenomenon, the SI-7321M offers two blanking times, selectable via the B_SEL pin, 1.8 µs and 3.6 µs. Torque reduction or motor noise issues caused by the phenomenon may be improved by using the longer time.

Comparison of Blanking Times The following table shows the comparison data of characteristics based on the difference of blanking time setting. The operating conditions and circuit factors such as the motor, motor voltage, and Ref/Sleep1 input voltage are the same.

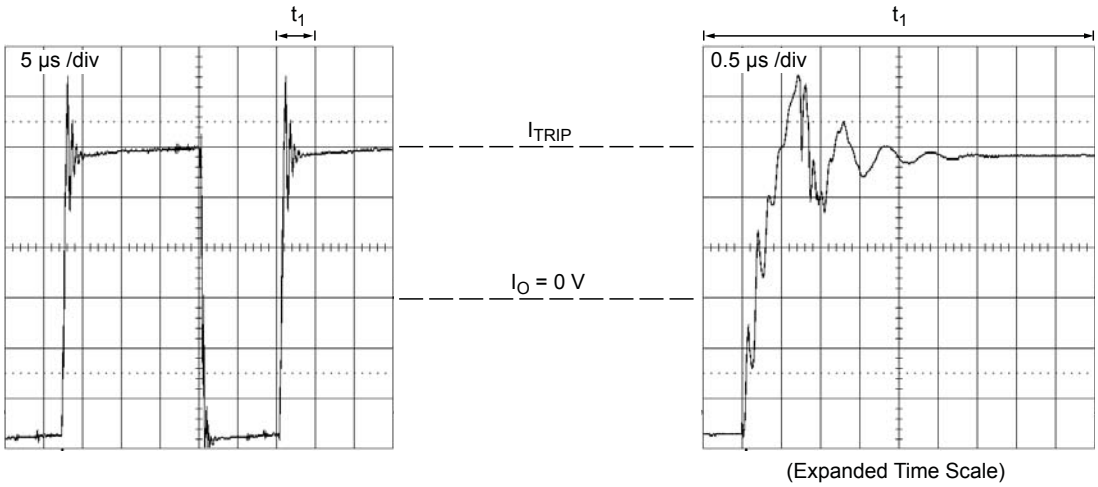


Figure 1. Operating waveforms on the Rs***x*** pins during PWM chopping

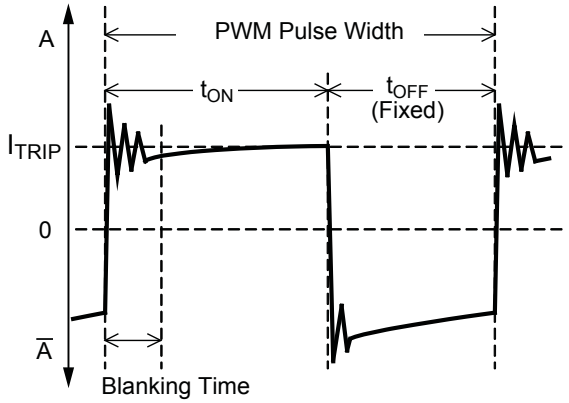


Figure 2. Rs***x*** pins pattern during PWM control

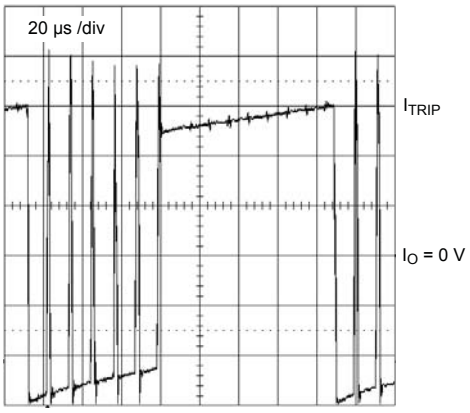


Figure 3. Rs***x*** pins pattern during seeking behavior

Minimum On-Time During PWM The SI-7231M features a fixed blanking time, with the device kept in active status (on) throughout this period, even if the on-time, t_{on}, is shortened to reduce the current level. PWM minimum on-time, $t_{on(min)}$, is defined as the actual on-time of the output MOSFET when the output status is On during this blanking period. Thus, the shorter blanking time means smaller $t_{on(min)}$.

Minimum Coil Current Minimum coil current represents reducing the coil current when the SI-7231M is operating with PWM control at minimum on time, $t_{on(min)}$. The result is that, with reduced coil current as the device powers down, current value decreases to a greater extent in the shorter blanking time.

Coil Current Waveform Distortion at High Speed Rotation The I_{TRIP} value varies according to the values specified by input on the Clock pin during microstepping. The I_{TRIP} value (internal standard voltage split ratio) is set up so that it becomes a sine wave. Because the motor coil current is PWM-controlled, referenced to I_{TRIP} value, coil current can be controlled so that it becomes a sine wave. In practice, there is some delay before the coil current reaches the target value of the inductance component of the coil.

In general, if the relationship between the convergence time, t_{conv}, (given $t_{conv} \leq I_{TRIP}$), and the input clock cycle (t_{clk}) is $t_{conv} < t_{clk}$ in all modes, then the envelope of the coil current follows I_{TRIP}. The threshold limit of t_{conv} is determined by power supply voltage and the coil time constant as current increases. As current decreases, it is determined by power supply voltage, coil time constant, and minimum on-time.

With increasing frequency of the Clock input signal, t_{clk} gets smaller normally, so that there are cases in which the coil current cannot converge to the I_{TRIP} value during one clock period. In these situations, the envelope of the coil current varies from a true sine wave.

Sanken calls this status *waveform distortion*. Figure 4 shows the comparison of waveform distortion with the two different blanking time options. The same power supply voltage, current setting value, and motors were used.

As shown the areas circled in figure 4, the envelope on the Rs*x* terminal waveform (same as the current waveform) with 1.8 µs blanking time forms a sine wave, but the waveform with 3.6 µs blanking time varies from a true sine wave.

Table 1. Blanking Times

Parameter	Relative Blanking Time	
	Short	Long
Minimum on-time during PWM	Smaller ←	
Anti-ringing noise tolerance		→ Bigger
Minimum coil current	Smaller ←	
Coil current at high speed rotation, with waveform distortion (microstep)		→ Bigger

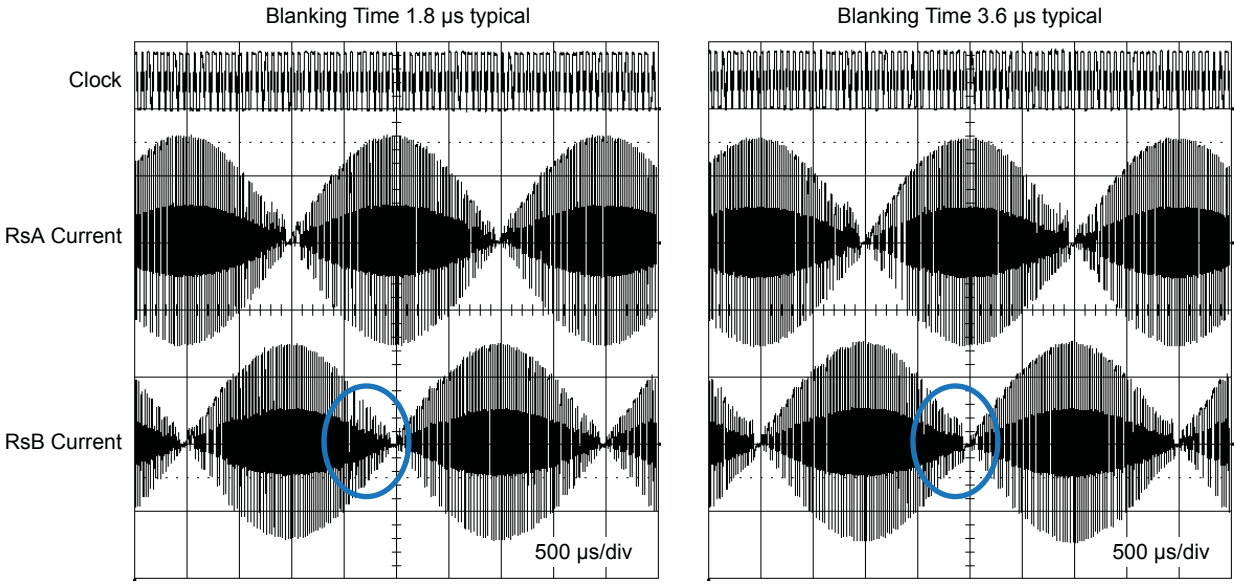


Figure 4. Rsx pins waveforms during high speed rotation. Circles indicate regions of waveform distortion.

The term *Bigger* in the table 1, represents that, considered under same conditions, the longer the blanking time, the lower the frequency at which waveform distortion occurs. Also, if the clock frequency is the same, the waveform distortion gets bigger at shorter blanking times.

However, even if such waveform distortion appears, it does not necessary mean that motor performance is affected. So, thorough evaluation of the trade-offs is necessary.

PWM Off-Time The PWM off-time, t_{off}, for the SI-7321M is controlled at a fixed duration by an internal oscillator. It also is switched at 3 levels by current proportion (see the Electrical Characteristics table).

In addition, the SI-7321M provides a synchronous rectification function that decreases losses occurring when the PWM turns off. This function dissipates back EMF stored in the motor coil at MOSFET turn-on, as well as at PWM turn-on.

Figure 5 shows the back EMF generative system. The SI-7321M performs on-off operations using only the MOSFET on the PWM-off side. To prevent simultaneous switching of the MOSFETs at synchronous rectification operation, the IC has a dead time of approximately 0.5 µs. During dead time, the back EMF flows through the body diode on the MOSFETs.

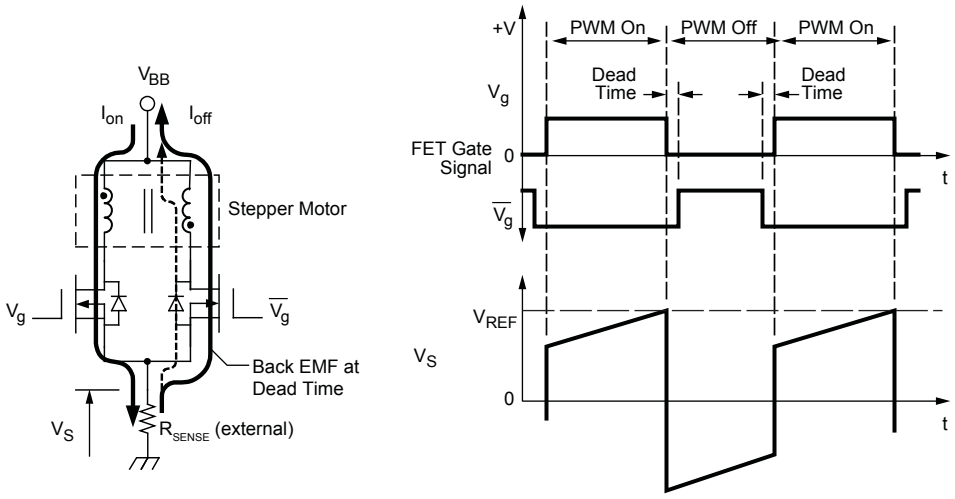


Figure 5. Synchronous rectification operation. During dead time, the back EMF flows through the body diodes of the MOSFETs on the PWM-off side.

Electrical Specifications

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_M		46	V
Main Power Supply Voltage	V_{BB}		46	V
Logic Supply Voltage	V_{DD}		6	V
Output Current	I_O	Current ratio mode F; output current rating may be limited by duty cycle, ambient temperature, and heat sinking; under any set of conditions, do not exceed the specified junction temperature, T_J	1.5	A
Logic Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
REF Input Voltage	V_{REF}		–0.3 to V_{DD}+0.3	V
Sense Voltage	V_{RS}	t_w < 1 µs not considered	±2	V
Power Dissipation	P_D	Using Sanken evaluation board at 25°C; rating significantly affected by the application PCB layout	3.5	W
Junction Temperature	T_J		150	°C
Ambient Temperature	T_A		–20 to 80	°C
Storage Temperature	T_{stg}		–30 to 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Load Supply Voltage	V_M		3	–	44	V
Main Power Supply Voltage	V_{BB}		10	–	44	V
Logic Supply Voltage	V_{DD}	Surge voltage at VDD pin should be less than ±0.5 V to avoid malfunctioning in operation	3.3	–	5.5	V
REF Input Voltage	V_{REF}	Protection features disabled	0.04	–	1.0	V
		Protection features enabled	0.04	–	0.5	V
Case Temperature	T_C	Measured at center of case on branded side	–	–	85	°C

ELECTRICAL CHARACTERISTICS, valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Main Power Supply Current	I_{BB}	Normal operation	–	–	15	mA
	I_{BBS}	Sleep1 or Sleep2 modes	–	–	100	µA
Logic Supply Current	I_{DD}		–	–	5	mA
MOSFET Breakdown Voltage	V_{DSS}	V_{BB} = 44 V, I_{DS} = 1 mA	100	–	–	V
MOSFET Output On-Resistance	$R_{DS(on)}$	I_{DS} = 1.5 A	–	0.25	0.4	Ω
MOSFET Body Diode Forward Voltage	V_F	I_F = 1.5 A	–	0.95	1.2	V
Maximum Clock Frequency[1]	f_{clk}	Clock duty cycle = 50%, at rising clock edge	250	–	–	kHz
Logic Input Voltage	V_{IL}		–	–	0.25 × V_{DD}	V
	V_{IH}		0.75 × V_{DD}	–	–	V
Logic Input Current	I_{IL}		–	±1	–	µA
	I_{IH}		–	±1	–	µA
REF Input Voltage Range[2]	V_{REF}	Protection functions disabled	0.04	–	1.5	V
		Protection functions enabled	0.04	–	0.6	V
	V_{REFS}	Sleep1 mode, output off, sequencer enabled, I_{BBS} within specification	2.0	–	V_{DD}	V
REF Input Current	I_{REF}	V_{REF} = 0 to V_{DD}	–	±10	–	µA
SENSE Voltage	V_{SENSE}	V_{REF} = 0.2 V, current ratio mode F	–	0.2	–	V
SENSE Current	I_{SENSE}		–	±10	–	µA
Overcurrent Protection Threshold Voltage	V_{OCP}	Motor coil short circuit, $V_{SENSE} \geq V_{OCP}$	0.65	0.7	0.75	V
Flag Pin Logic Output Voltage	V_{FLAGL}	I_{FLAGL} = 1.25 mA	–	–	1.25	V
	V_{FLAGH}	I_{FLAGH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Flag Pin Logic Output Current[3]	I_{FLAGL}		–	–	1.25	mA
	I_{FLAGH}		– 1.25	–	–	mA
Mo Pin Logic Output Voltage	V_{MOL}	I_{MOL} = 1.25 mA	–	–	1.25	V
	V_{MOH}	I_{MOH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Mo Pin Logic Output Current[3]	I_{MOL}		–	–	1.25	mA
	I_{MOH}		– 1.25	–	–	mA

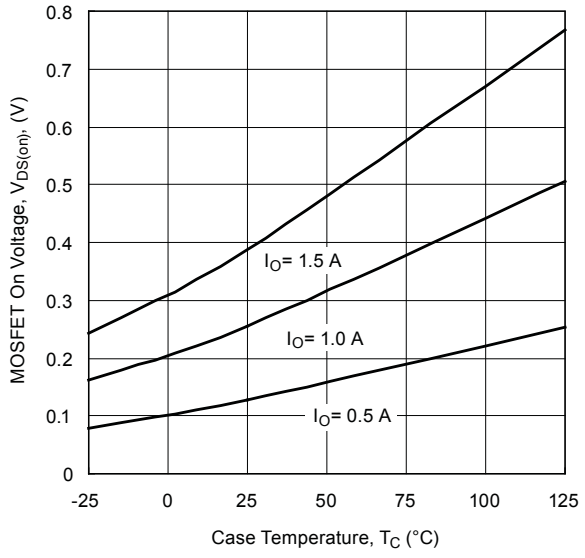
[1]Operation at a step frequency greater than the specified minimum value is possible but not warranted.
[2]V_{REF} setting range affected by whether or not protection features are enabled.
[3]Negative current is defined as coming out of the specified pin.

STEPPING CHARACTERISTICS valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

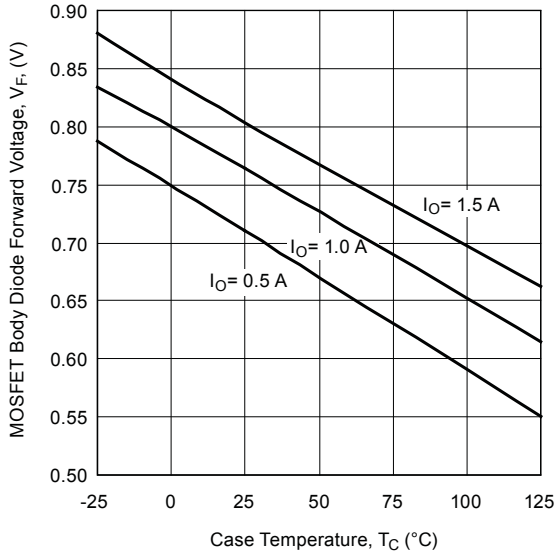
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Step Reference Current Ratio	Mode F	V_{REF} = V_{RSx} = 100 %, V_{REF} = 0.04 to 1.5 V	–	100.0	–	%
	Mode E		–	98.1	–	%
	Mode D		–	95.7	–	%
	Mode C		–	92.4	–	%
	Mode B		–	88.2	–	%
	Mode A		–	83.1	–	%
	Mode 9		–	77.3	–	%
	Mode 8		–	70.7	–	%
	Mode 7		–	63.4	–	%
	Mode 6		–	55.5	–	%
	Mode 5		–	47.1	–	%
	Mode 4		–	38.2	–	%
	Mode 3		–	29.0	–	%
	Mode 2		–	19.5	–	%
	Mode 1		–	9.8	–	%
Sleep-Enable Recovery Time	t_{SE}	Sleep1 and Sleep2 modes	100	–	–	µs
Switching Time	t_{con}	Measured from Clock edge to output on	–	2.0	–	µs
	t_{coff}	Measured from Clock edge to output off	–	1.5	–	µs
PWM Minimum On-Time	$t_{on(min)}$	B_SEL = low	–	1.8	–	µs
		B_SEL = high	–	3.6	–	µs
PWM Off-Time	t_{off1}	Current ratio modes 8 through F	–	13	–	µs
	t_{off2}	Current ratio modes 4 through 7	–	9.5	–	µs
	t_{off3}	Current ratio modes 1 through 3	–	7.5	–	µs
Load Disconnection Undetected Time	t_{opp}	Measured from PWM off	1.5	2	2.5	µs

Characteristic Data

Output MOSFET On-Voltage, $V_{DS(on)}$



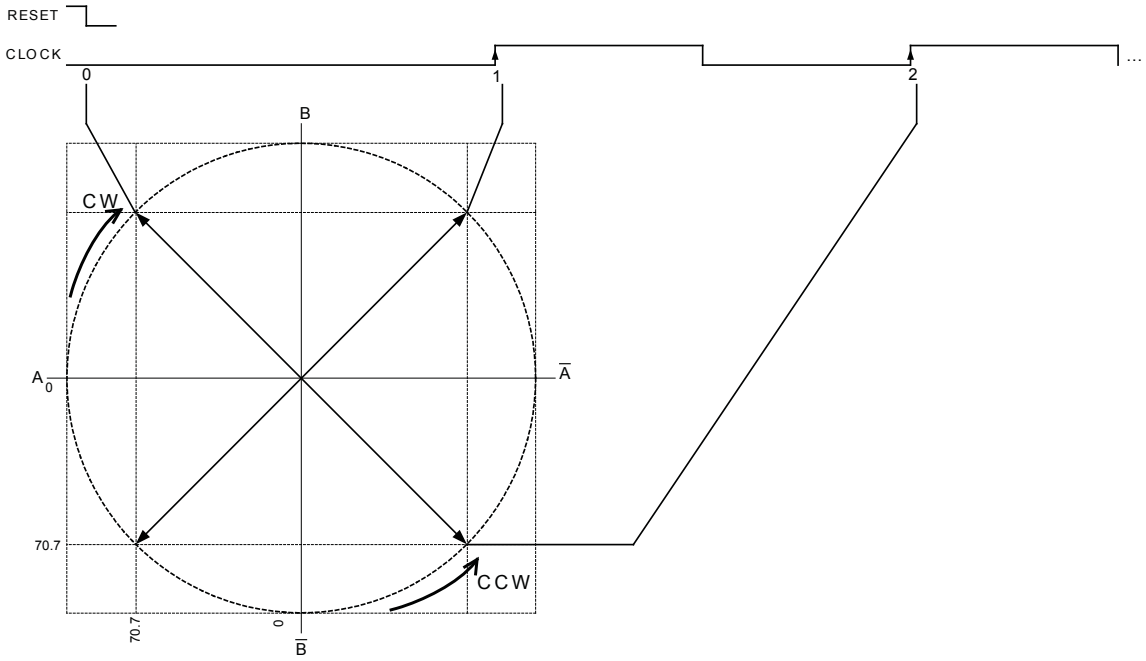
Output MOSFET Body Diode Forward Voltage, V_F



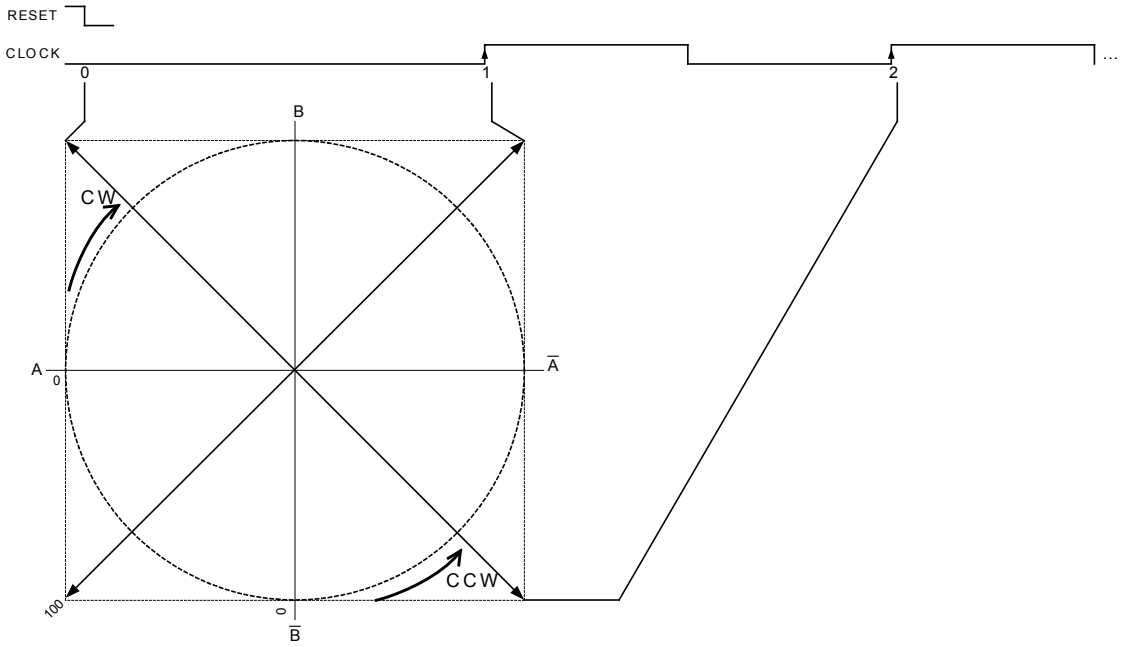
Step Sequencing

All illustrations in this section are based on step sequencing using the POS edge option. When the POS/NEG edge option is used, step sequences occur at both the rising edge and the falling edge of the Clock pulse.

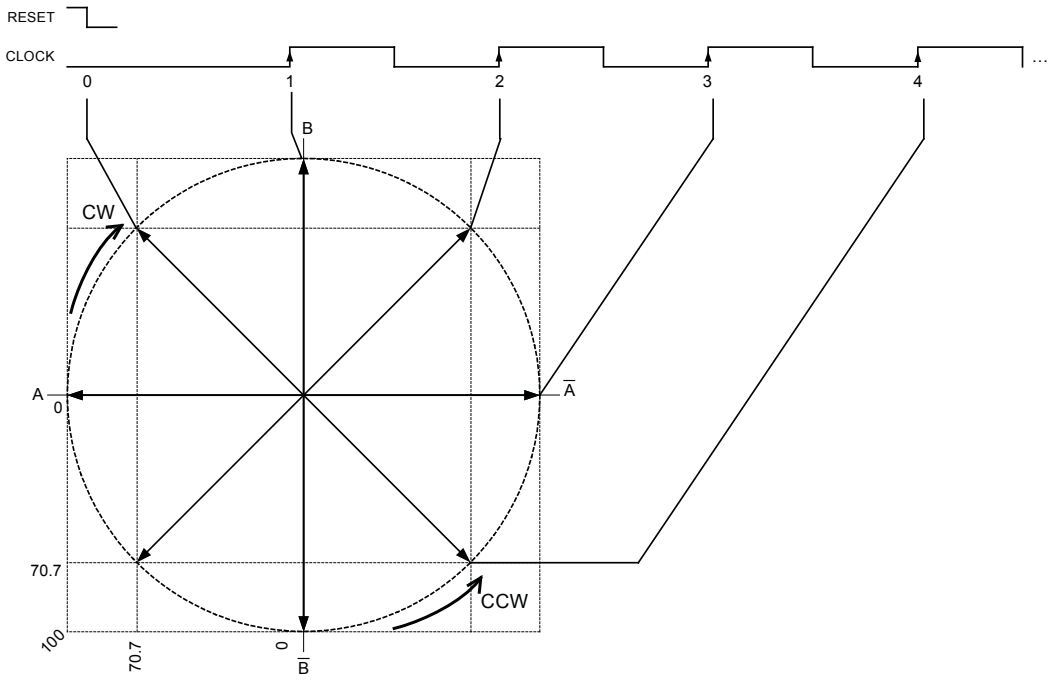
Full step
M1: Low, M2: Low, M3: Low (Mode 8)



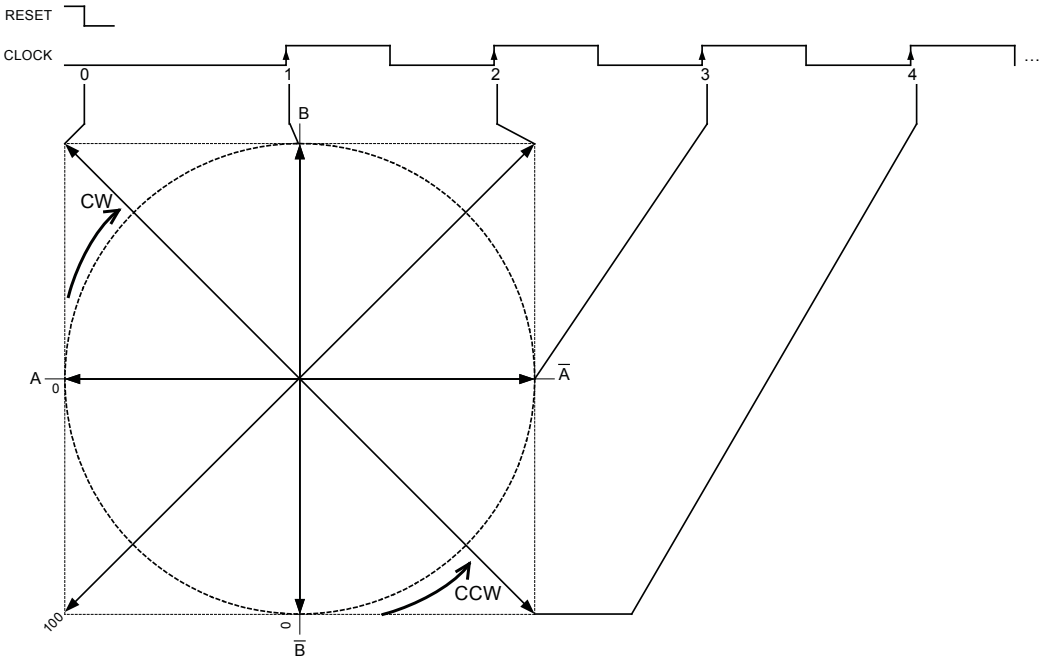
M1: High, M2: Low, M3: Low (Mode F)



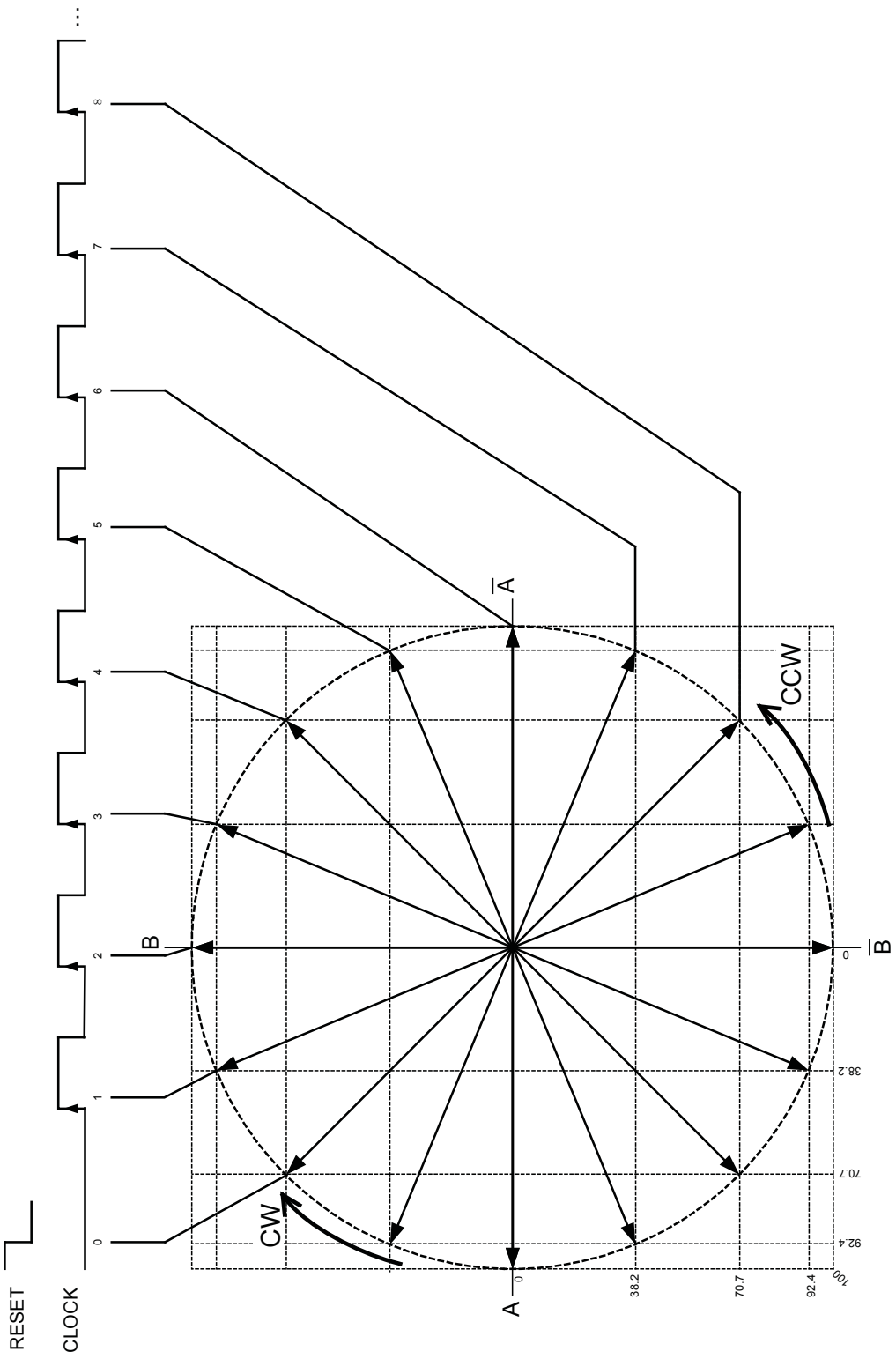
Half step
M1: Low, M2: High, M3: Low (Mode 8, F)



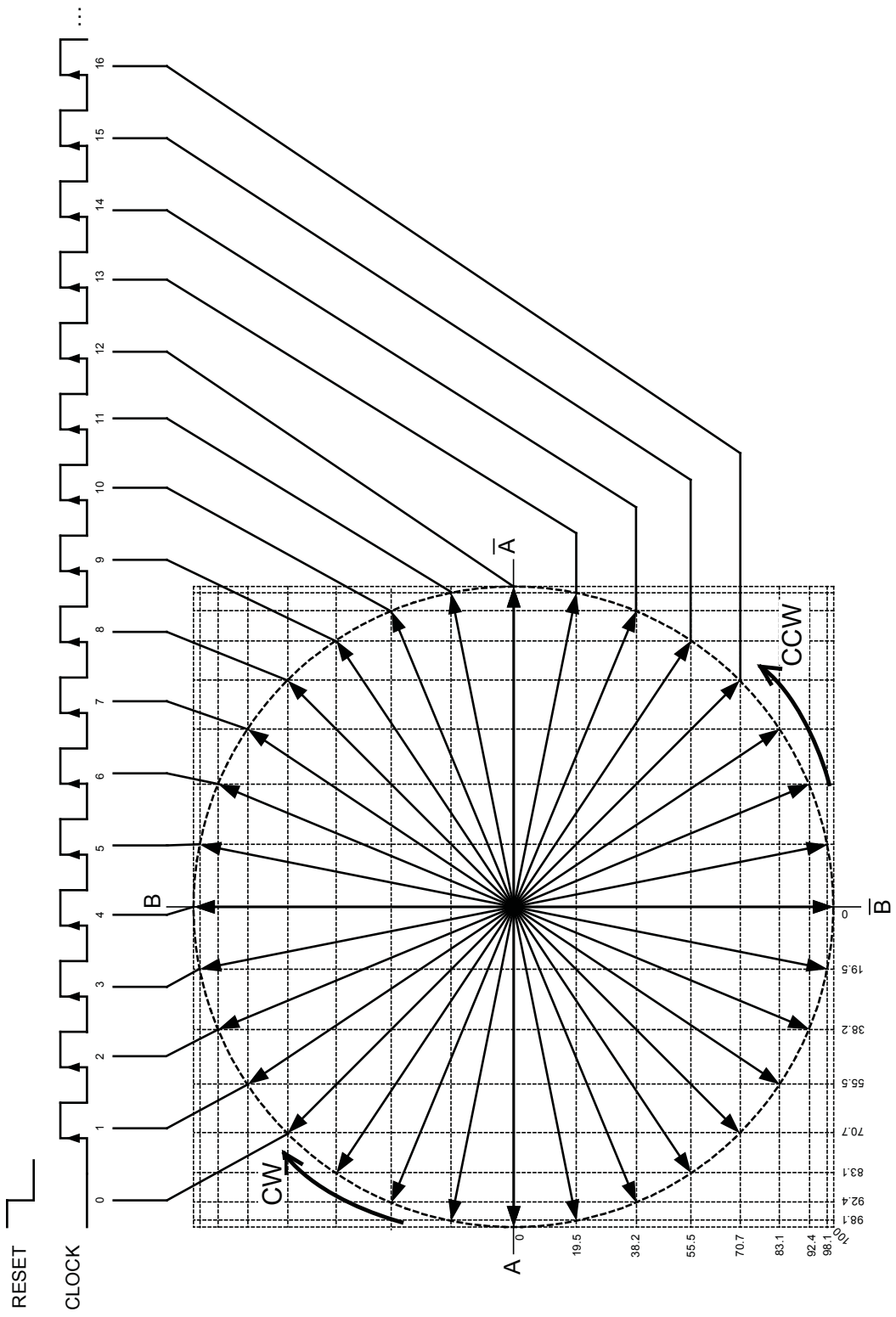
M1: High, M2: High, M3: Low (Mode F)



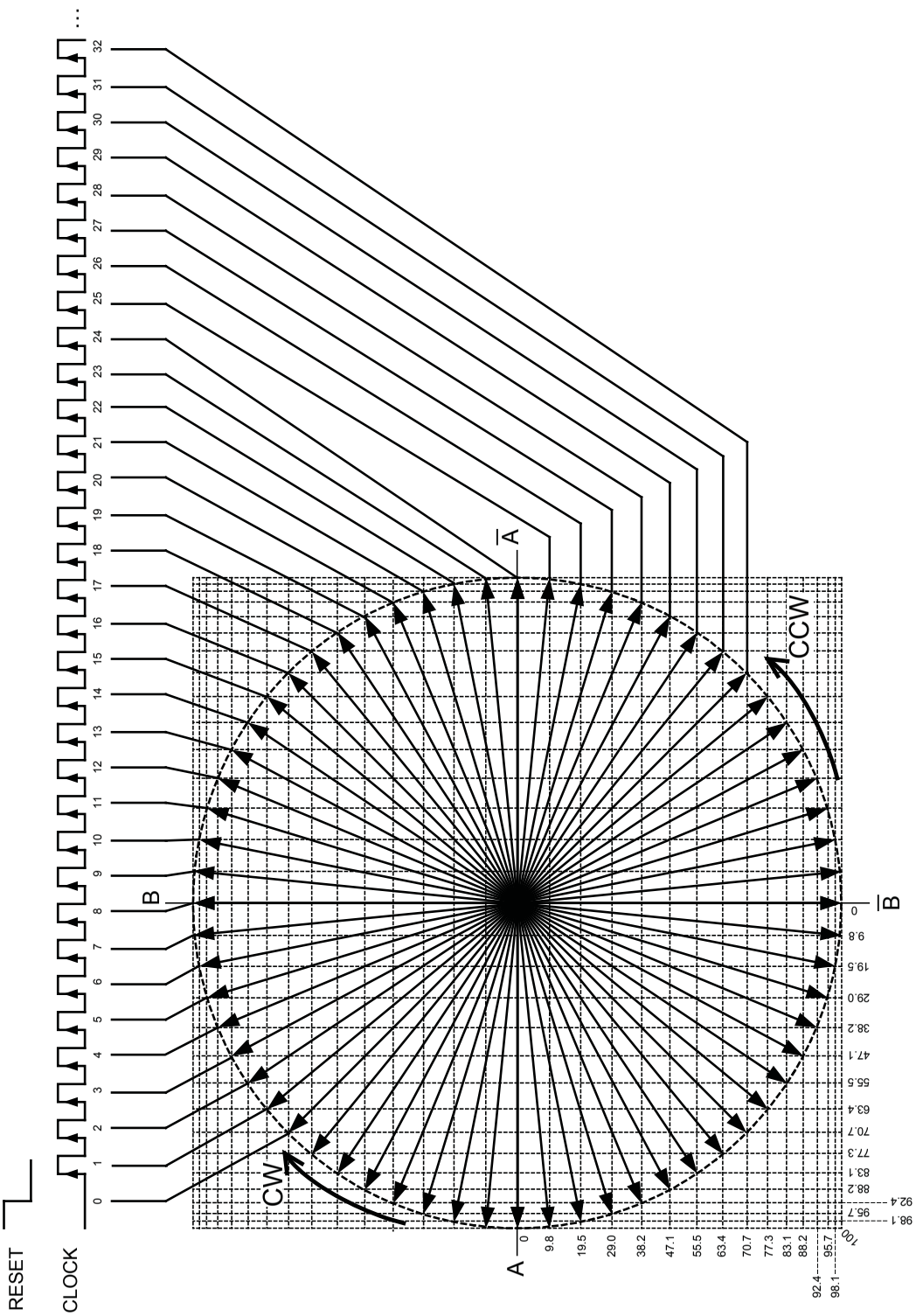
Quarter step
M1: Low, M2: Low, M3: High



Eighth step
M1: High, M2: Low, M3: High



Sixteenth step
M1: Low, M2: High, M3: High



Excitation Mode State Table[a]

Direction	Internal Sequence State				Step Sequencing						
	Phase A		Phase B		Full Step		Half Step		1/4 Step	1/8 Step	1/16 Step
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8, F	Mode F			
	A	8	B	8	X	X[b]	X	X[b]	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
CCW	A	3	B	D							X
▲	A	2	B	E						X	X
	A	1	B	F							X
	–	–	B	F			X	X	X	X	X
	$\overline{A}$	1	B	F							X
	$\overline{A}$	2	B	E						X	X
	$\overline{A}$	3	B	D							X
	$\overline{A}$	4	B	C					X	X	X
	$\overline{A}$	5	B	B							X
	$\overline{A}$	6	B	A						X	X
	$\overline{A}$	7	B	9							X
	$\overline{A}$	8	B	8	X	X[b]	X	X[b]	X	X	X
	$\overline{A}$	9	B	7							X
	$\overline{A}$	A	B	6						X	X
	$\overline{A}$	B	B	5							X
	$\overline{A}$	C	B	4					X	X	X
	$\overline{A}$	D	B	3							X
	$\overline{A}$	E	B	2						X	X
	$\overline{A}$	F	B	1							X
	$\overline{A}$	F	–	–			X	X	X	X	X
	$\overline{A}$	F	$\overline{B}$	1							X
	$\overline{A}$	E	$\overline{B}$	2						X	X
	$\overline{A}$	D	$\overline{B}$	3							X
	$\overline{A}$	C	$\overline{B}$	4					X	X	X
	$\overline{A}$	B	$\overline{B}$	5							X
	$\overline{A}$	A	$\overline{B}$	6						X	X
	$\overline{A}$	9	$\overline{B}$	7							X
	$\overline{A}$	8	$\overline{B}$	8	X	X[b]	X	X[b]	X	X	X
	$\overline{A}$	7	$\overline{B}$	9							X
	$\overline{A}$	6	$\overline{B}$	A						X	X
	$\overline{A}$	5	$\overline{B}$	B							X
	$\overline{A}$	4	$\overline{B}$	C					X	X	X
	$\overline{A}$	3	$\overline{B}$	D							X
	$\overline{A}$	2	$\overline{B}$	E						X	X
	$\overline{A}$	1	$\overline{B}$	F							X
	–	–	$\overline{B}$	F			X	X	X	X	X
	A	1	$\overline{B}$	F							X
	A	2	$\overline{B}$	E						X	X
	A	3	$\overline{B}$	D							X
	A	4	$\overline{B}$	C					X	X	X
	A	5	$\overline{B}$	B							X
	A	6	$\overline{B}$	A						X	X
	A	7	$\overline{B}$	9							X
	A	8	$\overline{B}$	8	X	X[b]	X	X[b]	X	X	X
	A	9	$\overline{B}$	7							X
	A	A	$\overline{B}$	6						X	X
	A	B	$\overline{B}$	5							X
	A	C	$\overline{B}$	4					X	X	X
	A	D	$\overline{B}$	3							X
	A	E	$\overline{B}$	2						X	X
	A	F	$\overline{B}$	1							X
▼	A	F	–	–			X	X	X	X	X
	A	F	B	1							X
CW	A	E	B	2						X	X
	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

[a]The change behavior is determined by the settings of the excitation pins (M1, M2, and M3) before and after the Clock edge.

[b]Sequence state is Mode 8, but step reference current ratio is Mode F. Mode F has step reference current ratio of 100%, and PWM off-time of 14 µs.

Application Information

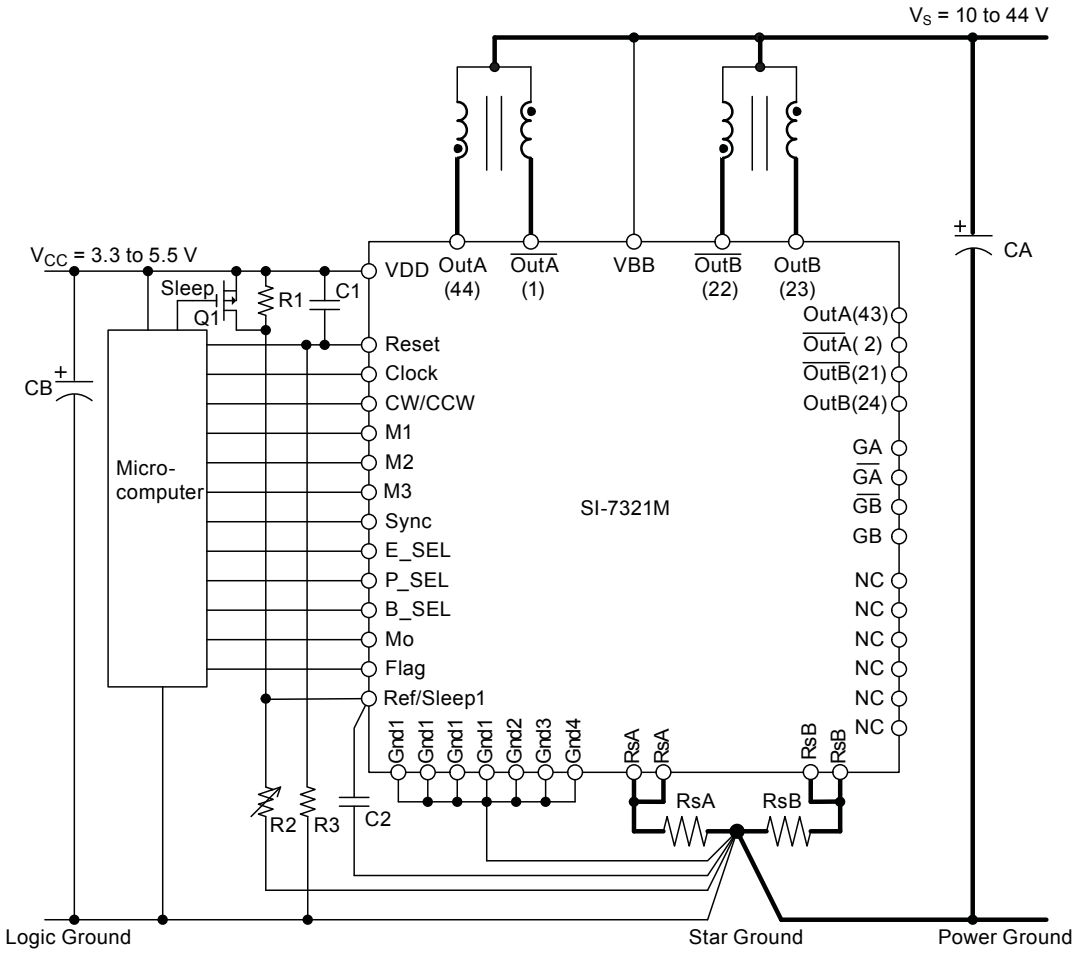


Figure 6. Typical application circuit

- Take precautions to avoid noise on the V_{DD} line; noise levels greater than 0.5 V on the V_{DD} line may cause device malfunction. Noise can be reduced by separating the logic ground and the power ground on a PCB from the Gnd pins.
- Constants, for reference use only:

  R1, R3 = 10 kΩ
  R2 = 1 kΩ (RV)
  CA = 100 µF / 50 V
  CB = 10 µF / 10 V
  C1, C2 = 0.1 µF

- Unused logic input pins (CW/CCW, M1, M2, M3, Reset, and Sync) *must* be pulled up/down to V_{DD} or ground. If those unused pins are left open, the device malfunctions.
- Unused logic output pins (Mo, Flag) *must* be kept open.

Motor Current Ratio Setting (R_1, R_2, R_{Sx})

The calculated value of motor current, Io , is determined by the ratios of external components R1, R2, and RSX (refer to the application example circuit, figure 6). The following is a formula for calculating Io :

$$I_O = \frac{R_2}{R_1 + R_2} \times \frac{V_{DD}}{R_{Sx}} \quad , \qquad (1)$$

when V_{REF} is within specification. If V_{REF} is set less than 0.1 V, variation or impedance of the wiring pattern may influence the IC and the possibility of less accurate current sensing becomes high.

The standard voltage of current ITRIP that controls is partially divided by the internal DAC:

$$I_{TRIP} = \frac{V_{REF}}{R_{Sx}} \times Current\ Mode\ Ratio \quad . \qquad (2)$$

Lower Limit of Control Current

The SI-732 1M uses a self-oscillating PWM current control topology in which the of - time is fixed. As energy stored in motor coil is eliminated within fixed the PWM of -time, coil current flows intermittently, as shown in figure 7.

Thus, average current decrease and motor torque also decrease. The point intermittent current starts flowing to the coil is considered as the lower limit of the control current. The lower limit of control current differs by the motor characteristics and other factors, but it is calculated from the following formula:

$$I_{O(min)} = \frac{V_M + R_{DS(on)} \times I_O}{R_M} + \exp\left(\frac{t_{OFF}}{T_C}\right)^{-1} - 1 \quad , \qquad (3)$$

where:

$$T_C = R_M \times L_M \text{ , and} \qquad (4)$$

V_M is the motor supply voltage,

$R_{DS(on)}$ is the MOSFET on resistance,

I_O is the target current level,

R_M is the motor winding resistance,

L_M is the motor winding inductance, and

t_{OFF} is the PWM of -time.

Even if the control current value is set at less than the lower limit of the control current, there is no setting at which the IC fails to operate. However, control current will worsen against setting current.

Avalanche Energy

In the unipolar topology of the SI-732 1M, a surge voltage (ringing noise) that exceeds the MOSFET capacity to withstand might be applied to the IC. To prevent damage, the SI-7321M MOSFET are designed with sufficient avalanche resistance to withstand this surge voltage. Therefore, even if surge voltages occur, users will be able to use the IC without any problems. However, in cases in which the motor harness is long or the IC is used above its rated current or voltage, there is a possibility that an avalanche energy could be applied that exceeds Sanken design expectations. Thus, users must test the avalanche energy applied to the IC under actual application conditions.

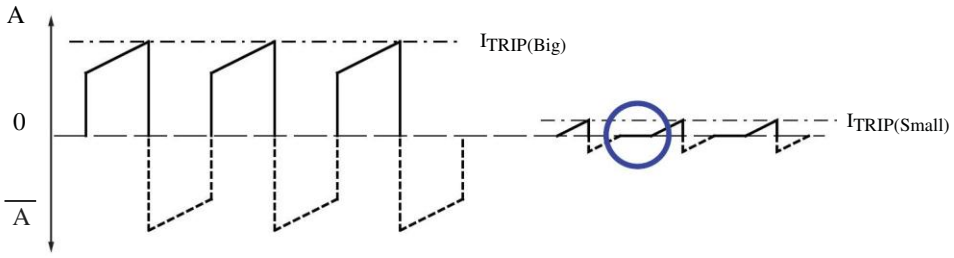


Figure 7. Control current lower limit model waveform. The circled area indicates the interval in which the coil current generated is 0 A.

The following procedure can be used to check the avalanche energy in an application. The schematic in figure 8 illustrates the location for the voltage test points and circuit characteristics. The timing diagram illustrates the waveform characteristics resultant.

Given:

$V_{DS(av)}$ = 1 A,

I_D = 1 A, and

t = 0.5 µs,

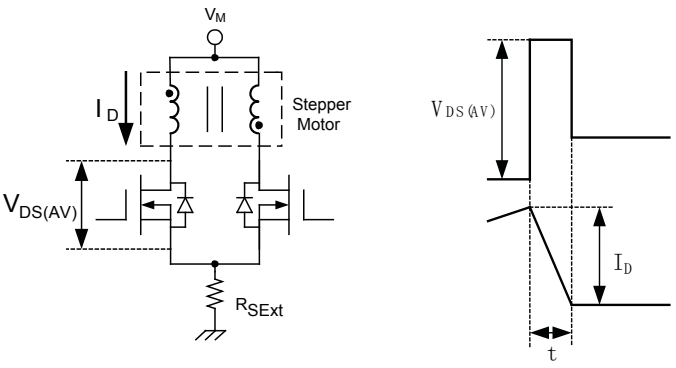


Figure 8. Test points and characteristics (left panel) and breakdown waveform timing (right)

the avalanche energy, E_{AV}, can be calculated using the following formula:

$$E_{AV} = V_{DS(av)} \times 0.5 \times I_D \times t \quad (5)$$
$$= 140\ V \times 0.5 \times 1A \times 10^{-6}$$
$$= 0.035\ mJ$$

By comparing the calculated E_{AV} to the graph shown in figure 9, the application can be evaluated if it is safe for the IC by being within the avalanche energy-tolerated dose range of the MOSFET.

On-Off Sequence of Power Supply (VBB and VDD)

There is no restriction of the on-off sequence of the main power supply, VBB, and the logic supply, VDD.

Motor Supply Voltage (V_M) and Main Power Supply Voltage (V_{BB})

Because the SI-7321M series has a structure that separates the control IC (MIC) and the power MOSFETs (as shown in the Functional Block diagram), motor supply and main power supply are separated. Therefore, it is possible to drive the IC using different power supplies and different voltages for motor supply and main power supply. However, extra caution is needed because the supply voltage ranges differ among power supplies.

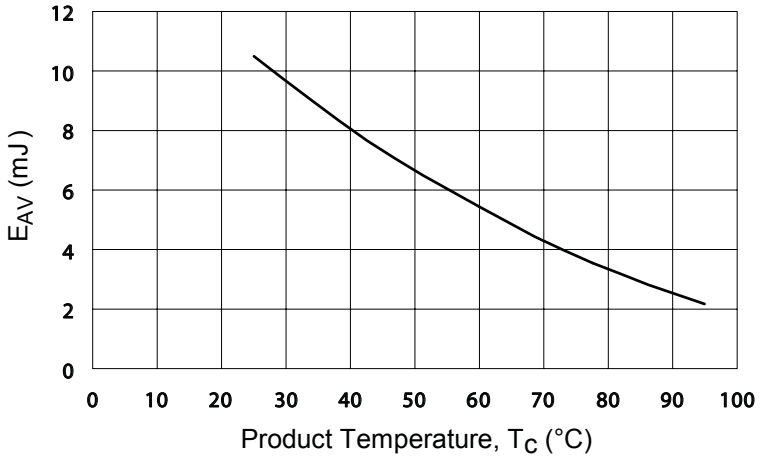


Figure 9. Iterated avalanche energy tolerated dose, $E_{AV(max)}$.

Internal Logic Circuits

Reset The sequencer circuit of this product is initialized after logic supply (V_{DD}) is applied, and the power on reset function operates. To initialize the sequencer, the output immediately after power-on indicates that the status that the power circuits are in the home state. In a case where the sequencer must be reset after motor has been operating, a reset signal must be applied to the Reset pin. In a case in which external reset control is not necessary, and the Reset pin is not used, it must be tied to ground on the application circuit board.

Clock When the Clock input signal stops, excitation changes to the motor Hold state. At this time, there is no difference if the Clock input signal is at logic low or logic high. The SI-7321M is designed to move 1 step at a time, when a Clock pulse edge is detected (rising if POS option selected, either rising or falling if POS/NEG selected).

Chopping Synchronous Circuit The SI-7321M has a chopping synchronous function to protect from abnormal noises that may occasionally occur during the motor Hold state. This function can be operated by setting the Sync terminal at logic high. However, if this function is used during motor rotation, control current does not stabilize, and therefore this may cause reduction of motor torque or increased vibration. So, Sanken does not recommend using this function while the motor is rotating. In addition, the synchronous circuit should be disabled in order to control motor current properly in case it is used other than in dual excitation state (Modes 8 and F) or single excitation Hold state.

In normal operation, generally the input signal for switching can be sent from an external microcomputer. However, in applications where the input signal cannot be transmitted adequately due to limitations of the port, the following method can be taken to use the functions.

The schematic diagram in figure 10 shows how the IC is designed so that the Sync signal can be determined by the Clock input signal. When a logic high signal is received on the Clock pin, the internal capacitor, C, is charged, and the Sync signal is set to logic low level. However, if the Clock signal cannot rise above logic low level (such as when the circuit between the microcomputer and the IC is not adequate), the capacitor is discharged by the internal resistor, R, and the Sync signal is set to logic high, causing the IC to shift to synchronous mode.

The RC time constant in the circuit should be determined by the minimum clock frequency used. In the case of a sequence that keeps the Clock input signal at logic high, an inverter circuit must be added. In a case where the Clock signal is set at an undetermined level, or when the POS/NEG edge option is used, an edge detection circuit (figure 10) can be used to prepare the signal for the Clock input, allowing correct processing by the circuit shown in figure 11.

Output Disable (Sleep1 and Sleep2) Circuits There are two methods to set this IC at motor free-state (coast, with outputs disabled). One is to set the Ref/Sleep1 pin to more than 2 V (Sleep1), and the other (Sleep2) is to set the excitation signals (pins M1, M2, and M3). In either way, the IC will change to Sleep mode, stopping the main power supply at the same time, and decreasing circuit current. The difference between the two methods is that, in the first way, the internal sequencer remains in an enabled state, and in the latter method, the IC enters the Hold state. Moreover, in the method using the excitation signals (Sleep2), excitation timing remains in a standby state, even if a signal is inputted on the Clock pin during Sleep2 mode.

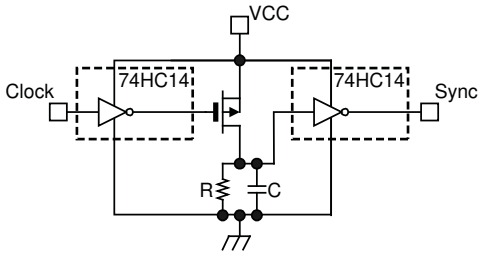


Figure 10. Clock signal shutoff detection circuit; using 74HC14s

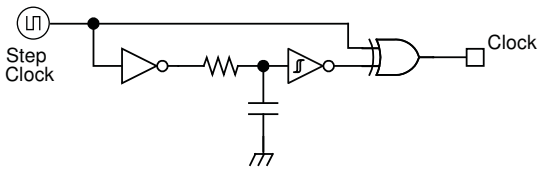


Figure 11. Clock signal edge detection circuit; inputs to example circuit shown in figure 10

When awaking to normal operating mode (motor rotation) from disabled (Sleep1 or Sleep2) mode, set an appropriate delay time from cancellation of the disable mode to the initial Clock input edge. In doing so, consider not only of rise time for the IC, but also of the rise time for the motor excitation current, is important (see figure 12). When using POS/NEG edge option, the case can occur in which the Clock signal negative edge should be used for calculating the delay.

Ref/Sleep1 Pin The Ref/Sleep1 pin provides access to the following functions:

- Standard voltage setting for output current level setting
- Output enable-disable control input

Figure 2 shows the general relationship between the reference voltage, V_{REF}, (Ref/Sleep1 pin) setting voltage and performance. There are, however, situations in which extra caution should be exercised. These are shown in figure 13:

- Range A. In this range, the control current value also varies in accordance with V_{REF}. Therefore, losses in the IC and the sense resistors must be given extra consideration.
- Range B. In this range, the voltage that switches output enable and disable (Sleep mode) exists. At enable, the same cautions apply as in range A. In addition, for some cases, there are possibilities that the output status will become unstable as a result of iteration between enable and disable.

Logic Input Pins If a logic input pin (Clock, Reset, CW/CCW, M1, M2, M3, or Sync) is not used (fixed logic level), the pin must be tied to V_{DD} or Gnd. Please do not leave them floating, because there is possibility of undefined effects on IC performance when they are left open.

Output Pins The Mo and Flag output pins are designed as monitor outputs, and inside of the IC is an output inverter (see figure 14). Therefore, let these pins float if they are not used.

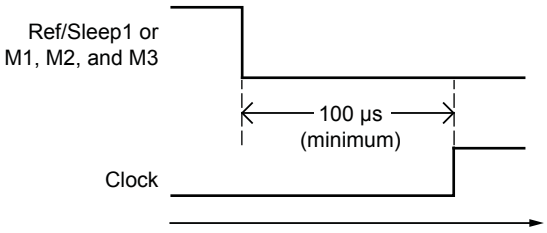


Figure 12. Timing delay between disable cancellation and the next Clock input

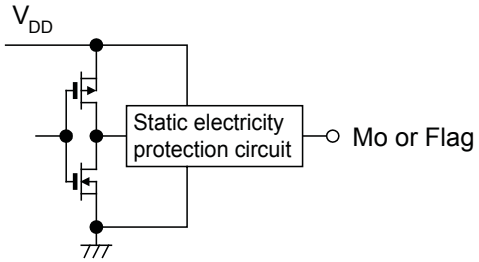


Figure 14. Mo pin and Flag pin general internal circuit layout

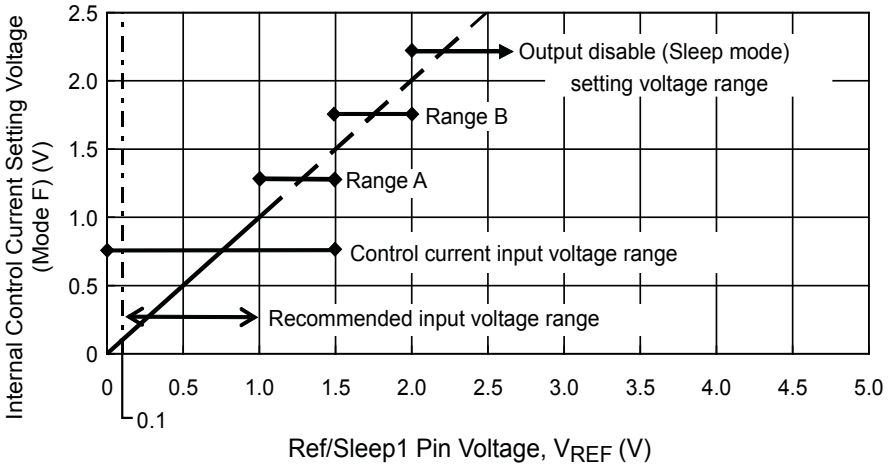


Figure 13. Relationship between external and internal reference voltages and performance

Thermal Design Information

It is not practical to calculate the power dissipation of the SI-7321M accurately, because that would require factors that are variable during operation, such as time periods and excitation modes during motor rotation, input frequencies and sequences, and so forth. Given this situation, it is preferable to perform an approximate calculation at worst case conditions. The following are simplified formulas for calculation of power dissipation:

$$P_D = I_O^2 \times R_{DS(on)} \times 2 \quad , \tag{6}$$

where:

P_D is the power dissipation in the IC,

I_O is the operating output current, and

$R_{DS(on)}$ is the on resistance of the output MOSFET.

Based on the P_D calculated using the above formula, the expected increase in operating junction temperature, ΔT_J, of the IC can be estimated using figure 15.

This result must be added to the worst case ambient temperature when operating, $T_{A(max)}$. Based on the calculation, there is no problem unless $T_{A(max)} + \Delta T_J > 150°C$. However, final confirmation must be made by measuring the IC temperature during operation and then verifying power dissipation and junction temperature in the graph.

When the IC ground is connected to a large area of exposed copper on the PCB that acts as a heat sink, device package thermal resistance, $R_{\theta JA}$, is a variable used in calculating ΔT_{JA}.

The value of $R_{\theta JA}$ is calculated from the following formula:

$$R_{\theta JA} + R_{\theta JC} = R_{\theta JA} - R_{\theta CA} \quad . \tag{7}$$

ΔT_{JA} can be calculated using the value of $R_{\theta JA}$:

$$\Delta T_J = \Delta T_{JC} + P_D \times R_{\theta JC} \quad . \tag{8}$$

The following procedure should be used to measure product temperature in actual operation and then estimate junction temperature:

1. Measure the ambient temperature, T_A.
2. With the device mounted but not operating, measure the temperature of the device case at the center of the branded side.
3. Power-on the device, and after it reaches operating temperature, take the measurement again.
4. Subtract the value found in step 2 from the value found in step 3. This will provide a value for ΔT_{CA}.
5. Refer to figure 15 and locate the value found in step 4 on the ΔT_{CA} trace.
6. Determine the corresponding power dissipation, P_D.
7. Substitute the values into equation 8.

CAUTION: The SI-7321M is designed as a multichip, with separate power elements (MOSFET) and control IC (MIC). Consequently, because the control IC cannot accurately detect the temperature of the power elements (which are the primary sources of heat), the ICs do not provide a protection function against overheating. For thermal protection, users must conduct sufficient thermal evaluations to be able to ensure that the junction temperature does not exceed the warranty level (150°C).

This thermal design information is provided for preliminary design estimations only. The thermal performance of the IC will be significantly determined by the conditions of the application, in particular the state of the mounting PCB, exposed copper area heat sink, and the ambient air. Before operating the IC in an application, the user must experimentally determine the actual thermal performance.

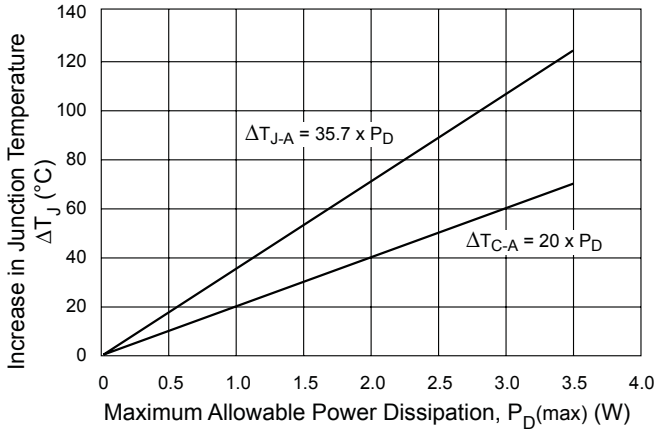


Figure 15. Temperature increase relationship