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Si1000/1/2/3/4/5

Ultra Low Power, 64/32 kB, 10-Bit ADC MCU with Integrated 240–960 MHz EZRadioPRO® Transceiver

Ultra Low Power: 0.9 to 3.6 V Operation

- Typical sleep mode current < 0.1 µA; retains state and RAM contents over full supply range; fast wakeup of < 2 µs
- Less than 600 nA with RTC running
- Less than 1 µA with RTC running and radio state retained
- On-chip dc-dc converter allows operation down to 0.9 V.
- Two built-in brown-out detectors cover sleep and active modes

10-Bit Analog to Digital Converter

- Up to 300 ksps
- Up to 18 external inputs
- External pin or internal VREF (no external capacitor required)
- Built-in temperature sensor
- External conversion start input option
- Autonomous burst mode with 16-bit automatic averaging accumulator

Dual Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5 µA)

On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 4352 bytes internal data RAM (256 + 4096)
- 64 kB (Si1000/2/4) or 32 kB (Si1001/3/5) flash; In-system programmable in 1024-byte sectors—1024 bytes are reserved in the 64 kB devices

EZRadioPRO® Transceiver

- Frequency range = 240–960 MHz
- Sensitivity = –121 dBm
- FSK, GFSK, and OOK modulation
- Max output power = +20 dBm (Si1000/1), +13 dBm (Si1002/3/4/5)
- RF power consumption
  - 18.5 mA receive
  - 18 mA @ +1 dBm transmit
  - 30 mA @ +13 dBm transmit
  - 85 mA @ +20 dBm transmit
- Data rate = 0.123 to 256 kbps
- Auto-frequency calibration (AFC)
- Antenna diversity and transmit/receive switch control
- Programmable packet handler
- TX and RX 64 byte FIFOs
- Frequency hopping capability
- On-chip crystal tuning

Digital Peripherals

- 19 or 16 port I/O plus 3 GPIO pins; Hardware enhanced UART, SPI, and I^2C serial ports available concurrently
- Low power 32-bit SmaRTClock
- Four general purpose 16-bit counter/timers; six channel programmable counter array (PCA)

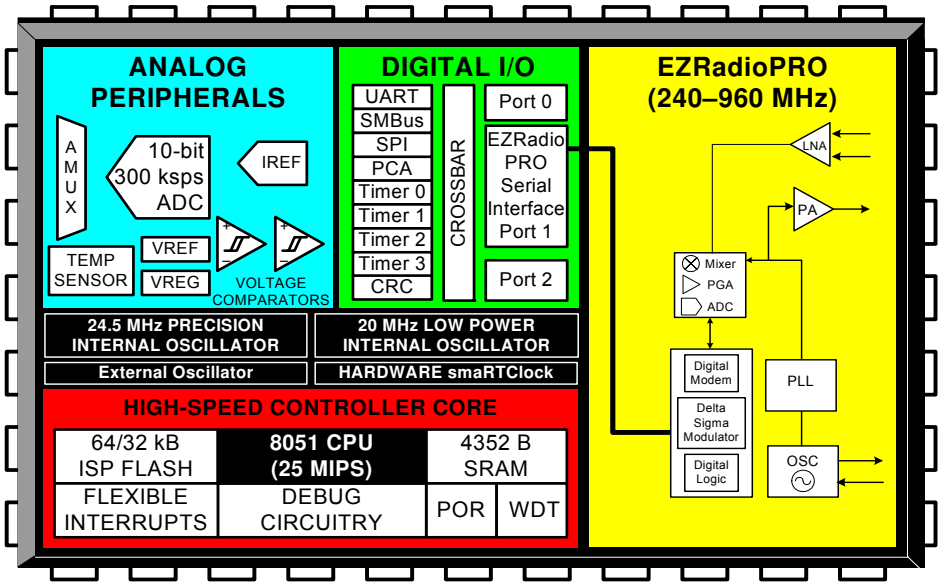
Clock Sources

- Precision internal oscillators: 24.5 MHz with ±2% accuracy supports UART operation; spread-spectrum mode for reduced EMI; Low power 20 MHz internal oscillator
- External oscillator: Crystal, RC, C, CMOS clock
- SmaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

Package

- 42-pin LGA (5 x 7 mm)

Temperature Range: –40 to +85 °C



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1. System Overview

Si1000/1/2/3/4/5 devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- 240–960 MHz EZRadioPRO® transceiver
- Single/Dual battery operation with on-chip dc-dc boost converter
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 300 ksps 23-channel single-ended ADC with analog multiplexer
- 6-bit programmable current reference
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology
- 64 kB or 32 kB of on-chip flash memory
- 4352 bytes of on-chip RAM
- SMBus/I^2C, Enhanced UART, and two Enhanced SPI serial interfaces implemented in hardware (SPI1 is dedicated for communication with the EZRadioPRO peripheral)
- Four general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with six capture/compare modules and watchdog timer (WDT) function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- Two on-chip voltage comparators with 18 touch sense inputs
- 19 or 22 port I/O (5 V tolerant except for GPIO_0, GPIO_1, and GPIO_2)

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the Si1000/1/2/3/4/5 devices are truly standalone system-on-a-chip solutions. The flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The Si1000/1/2/3/4/5 are available in a 42-pin LGA package (lead-free and RoHS compliant). See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.6.

The transceiver's extremely low receive sensitivity (–121 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. The advanced radio features including continuous frequency coverage from 240–960 MHz in 156 Hz or 312 Hz steps allow precise tuning control. Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption. The transceivers digital receive architecture features a high-performance ADC and DSP-based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance. The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading, ensuring compliance with global regulations including FCC, ETSI, ARIB, and 802.15.4d regulations.

An easy-to-use calculator is provided to quickly configure the radio settings, simplifying customer's system design and reducing time to market.

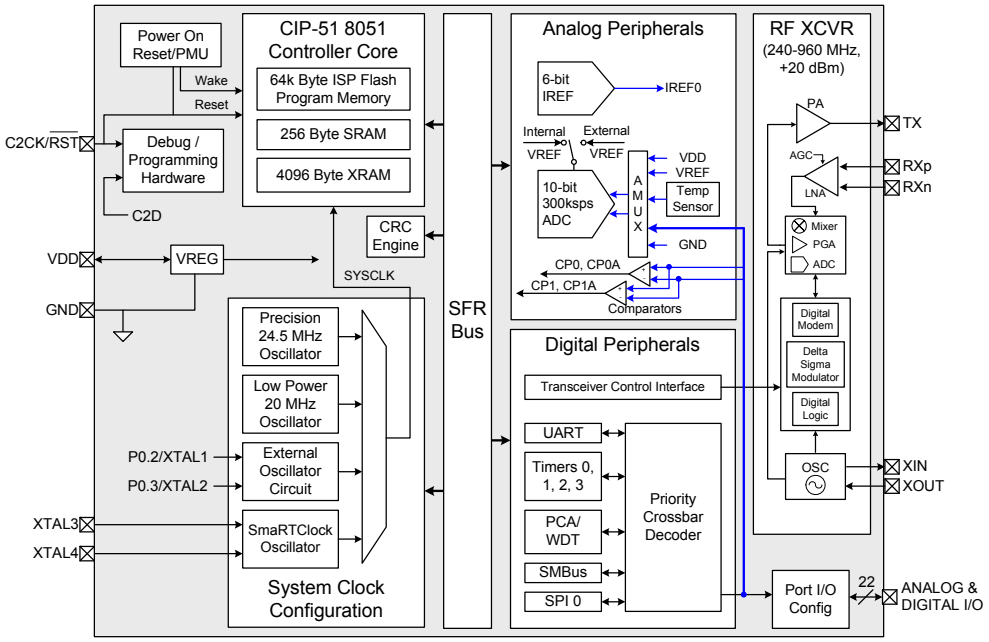

Figure 1.1. Si1000 Block Diagram

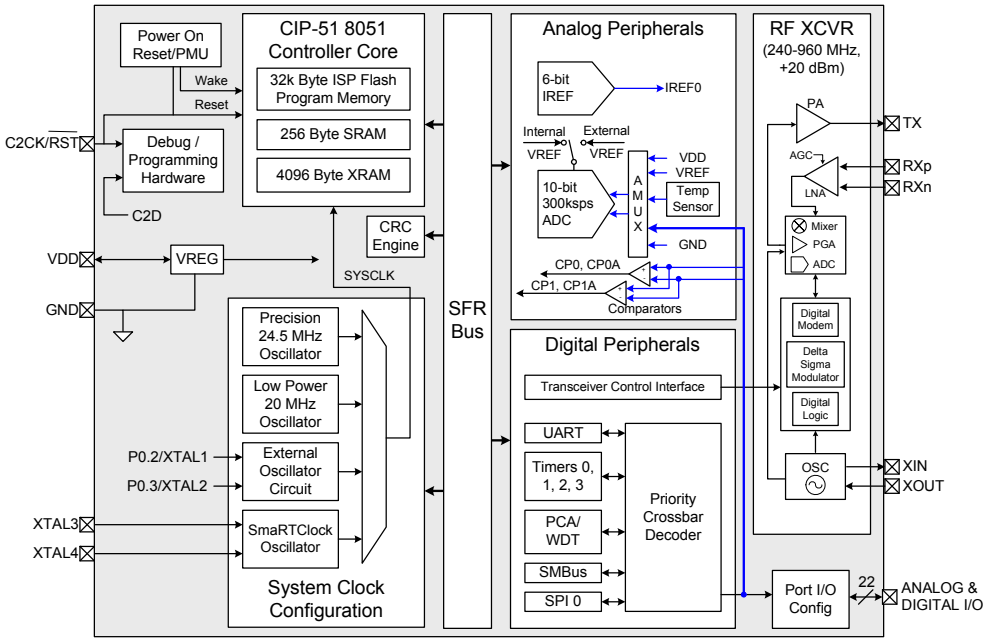

Figure 1.2. Si1001 Block Diagram

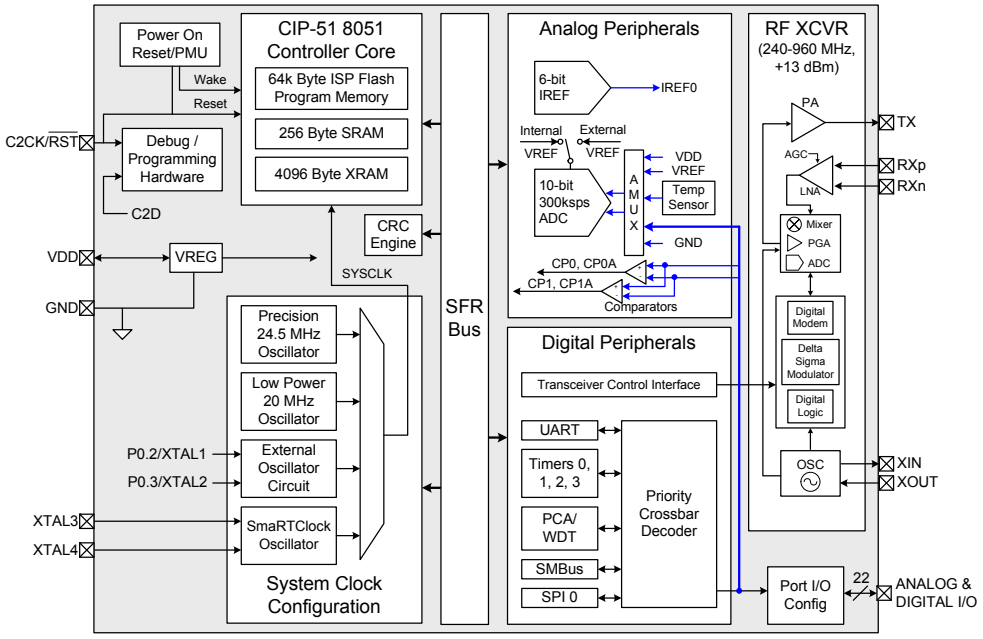

Figure 1.3. Si1002 Block Diagram

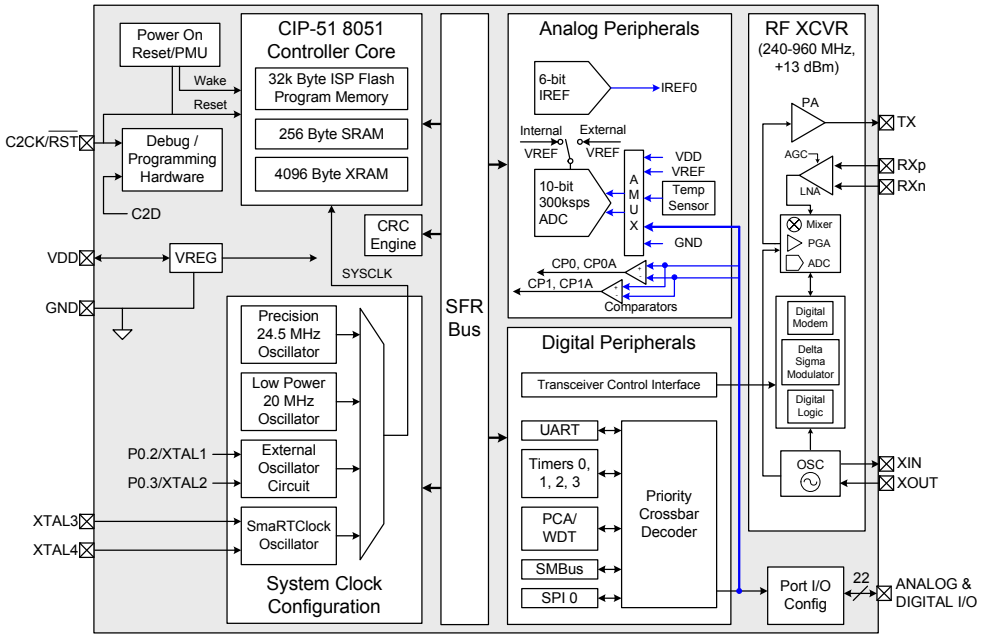

Figure 1.4. Si1003 Block Diagram

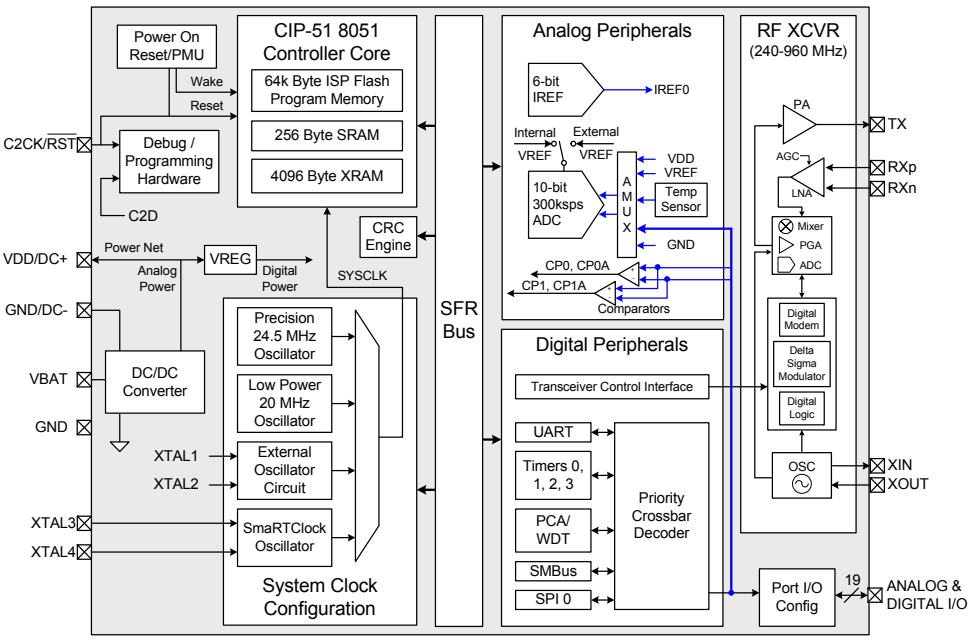

Figure 1.5. Si1004 Block Diagram

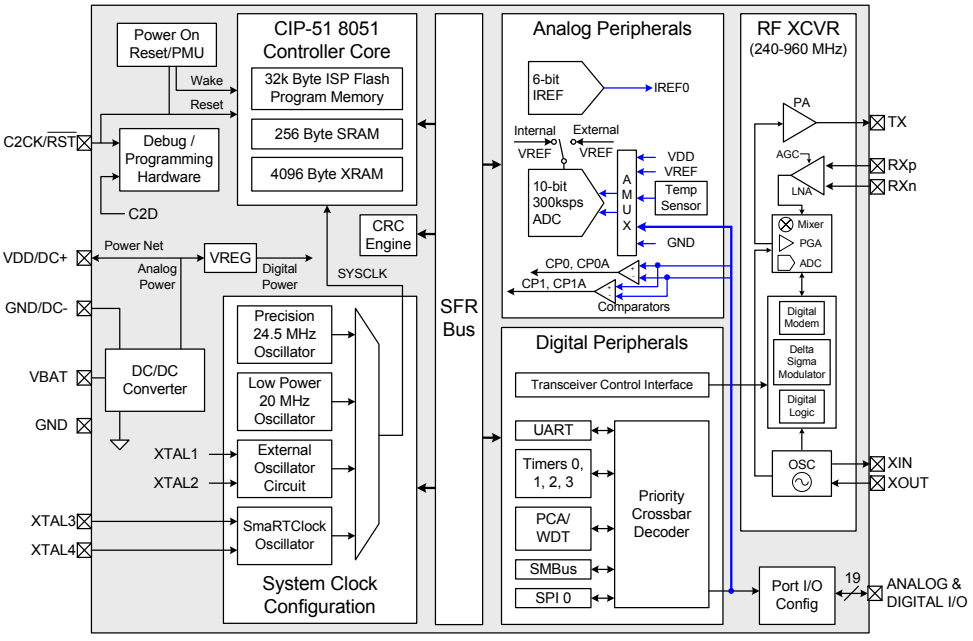

Figure 1.6. Si1005 Block Diagram

1.1. Typical Connection Diagram

The application shown in Figure 1.7 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A complete direct-tie reference design is available from Silicon Laboratories applications support.

For applications seeking improved performance in the presence of multipath fading, antenna diversity can be used. Antenna diversity support is integrated into the EZRadioPRO transceiver and can improve the system link budget by 8–10 dB in the presence of these fading conditions, resulting in substantial range increases. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

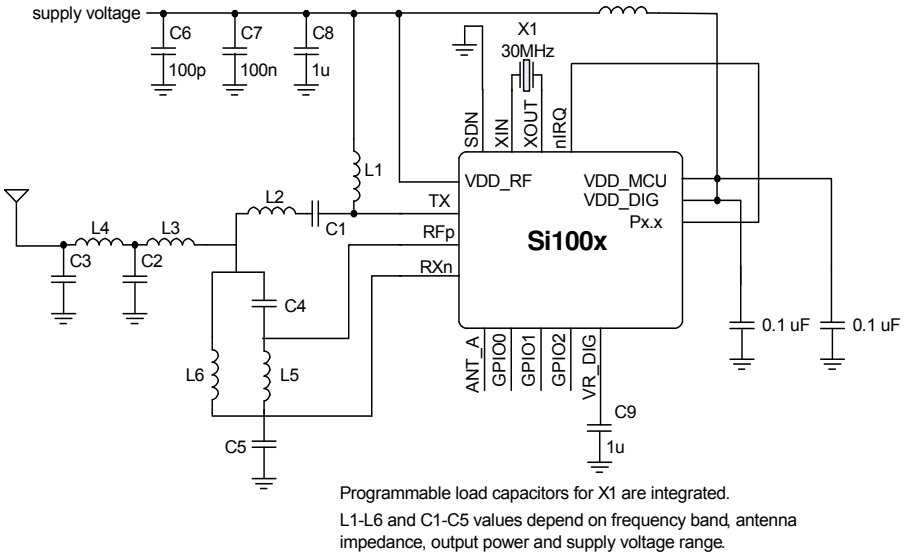

Figure 1.7. Si1002/3 RX/TX Direct-tie Application Example

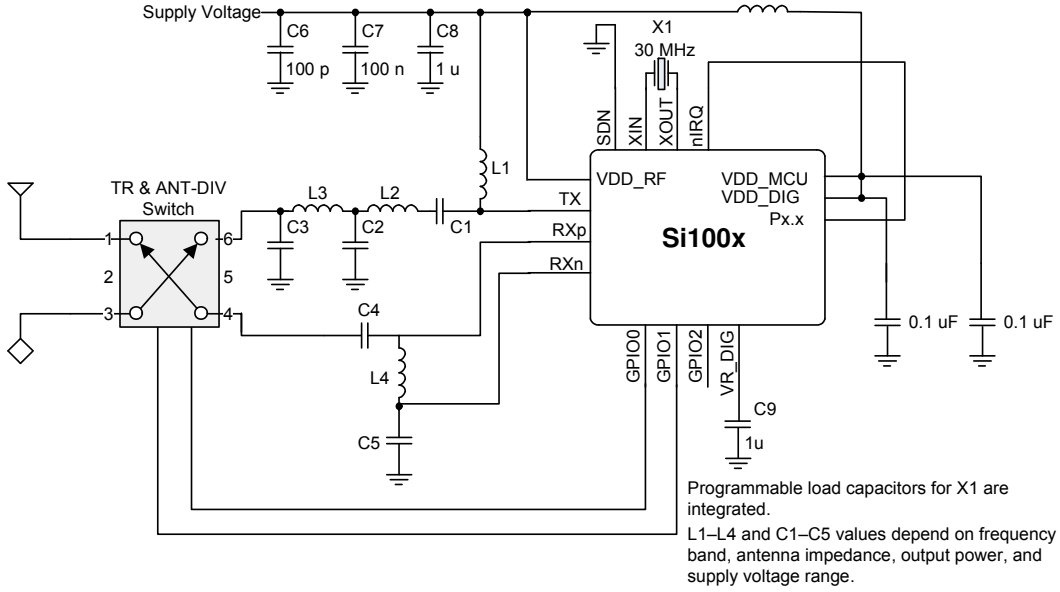

Figure 1.8. Si1000/1 Antenna Diversity Application Example

1.2. CIP-51™ Microcontroller Core

1.2.1. Fully 8051 Compatible

The Si1000/1/2/3/4/5 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.2.3. Additional Features

The Si1000/1/2/3/4/5 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51, allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a watchdog timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory is calibrated to 24.5 MHz and is accurate to ±2% over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

1.3. Port Input/Output

Digital and analog resources are available through 19 (Si1000/1/2/3) or 16 (Si1004/5) I/O pins. Three additional GPIO pins are available through the EZRadioPRO peripheral. Port pins are organized as three byte-wide ports. Port pins P0.0–P2.6 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P1.0, P1.1, P1.2, and P1.4 are dedicated for communication with the EZRadioPRO peripheral. P1.3 is not available. P2.7 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “29. Device Specific Behavior” on page 376 for more details.

The designer has complete control over which digital and analog functions are assigned to individual port pins and is limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “21.3. Priority Crossbar Decoder” on page 214 for more information on the crossbar.

All Px.x Port I/Os are 5 V tolerant when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the VDD_MCU supply. Port I/Os used for analog functions can operate up to the VDD_MCU supply voltage. See Section “21.1. Port I/O Modes of Operation” on page 211 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

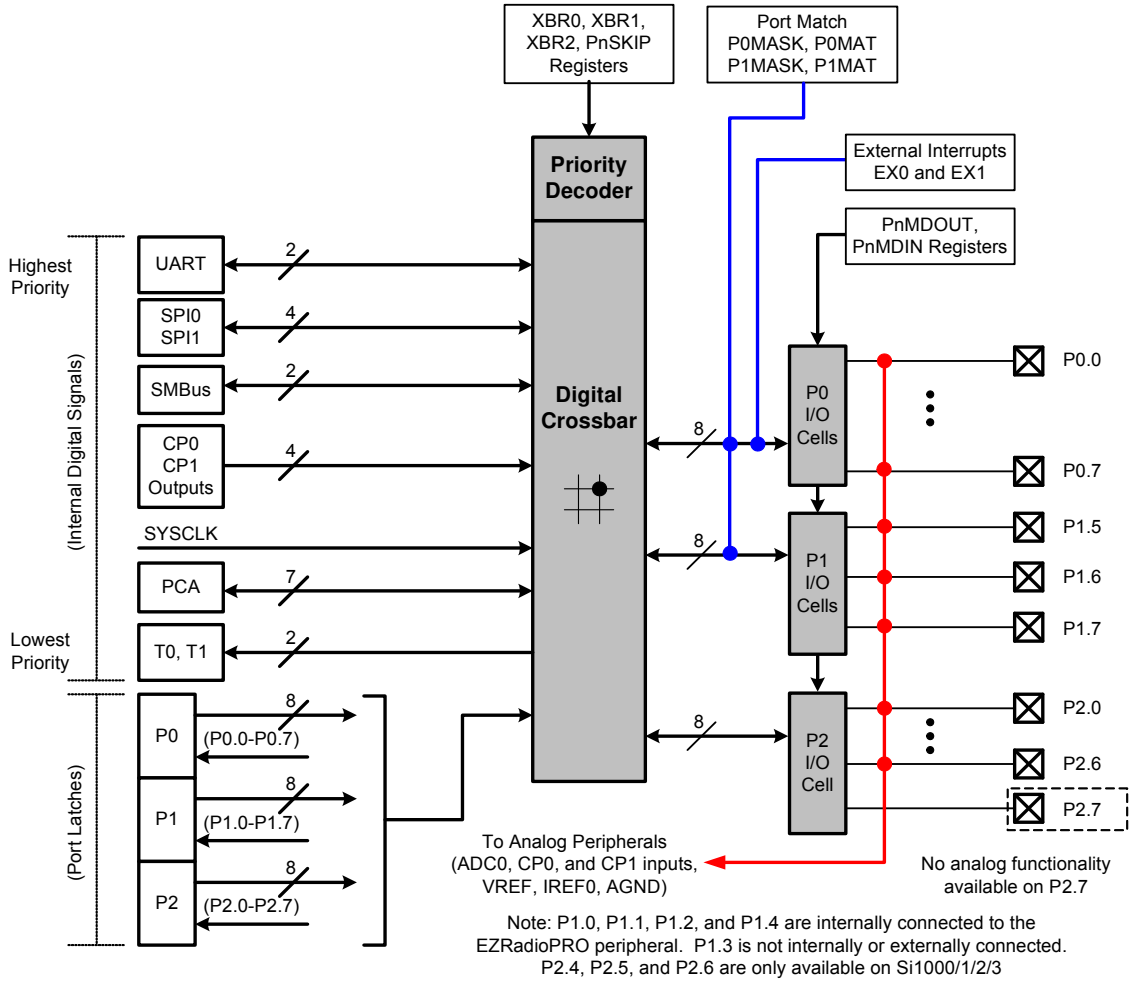

Figure 1.9. Port I/O Functional Block Diagram

1.4. Serial Ports

The Si1000/1/2/3/4/5 family includes an SMBus/I^2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention. There is also a dedicated EZRadioPRO Serial Interface (SPI1) to allow communication with the EZRadioPRO peripheral.

1.5. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with six programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8.

Each capture/compare module can be configured to operate in a variety of modes: edge-triggered capture, software timer, high-speed output, pulse width modulator (8, 9, 10, 11, or 16-bit), or frequency output. Additionally, Capture/Compare Module 5 offers watchdog timer capabilities. Following a system reset, Module 5 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

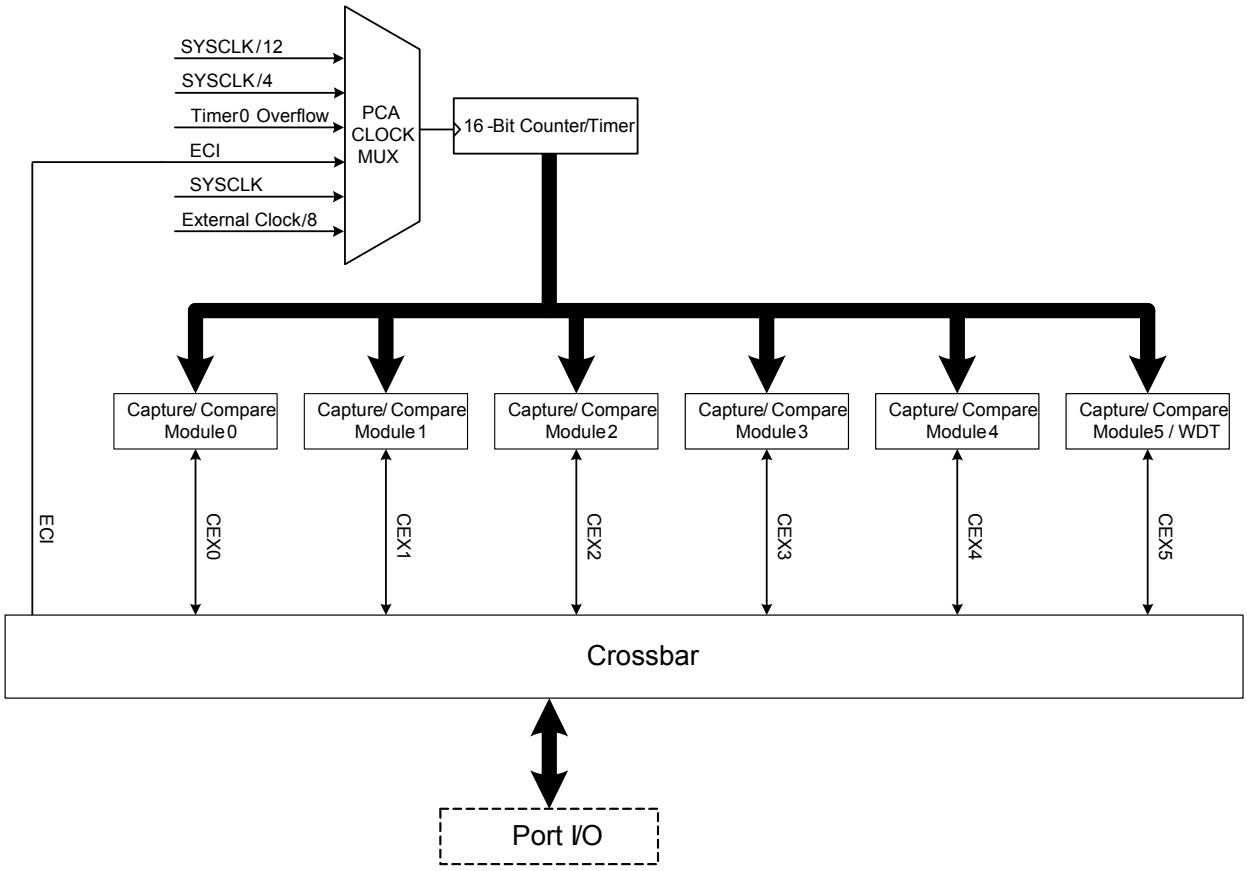

Figure 1.10. PCA Block Diagram

1.6. 10-bit SAR ADC with 16-bit Auto-Averaging Accumulator and Autonomous Low Power Burst Mode

Si1000/1/2/3/4/5 devices have a 300 ksps, 10-bit successive-approximation-register (SAR) ADC with integrated track-and-hold and programmable window detector. ADC0 also has an autonomous low power Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically average the ADC results, providing an effective 11, 12, or 13-bit ADC result without any additional CPU intervention.

The ADC can sample the voltage at any of the GPIO pins (with the exception of P2.7) and has an on-chip attenuator that allows it to measure voltages up to twice the voltage reference. Additional ADC inputs include an on-chip temperature sensor, the VDD_MCU supply voltage, the VBAT supply voltage, and the internal digital supply voltage.

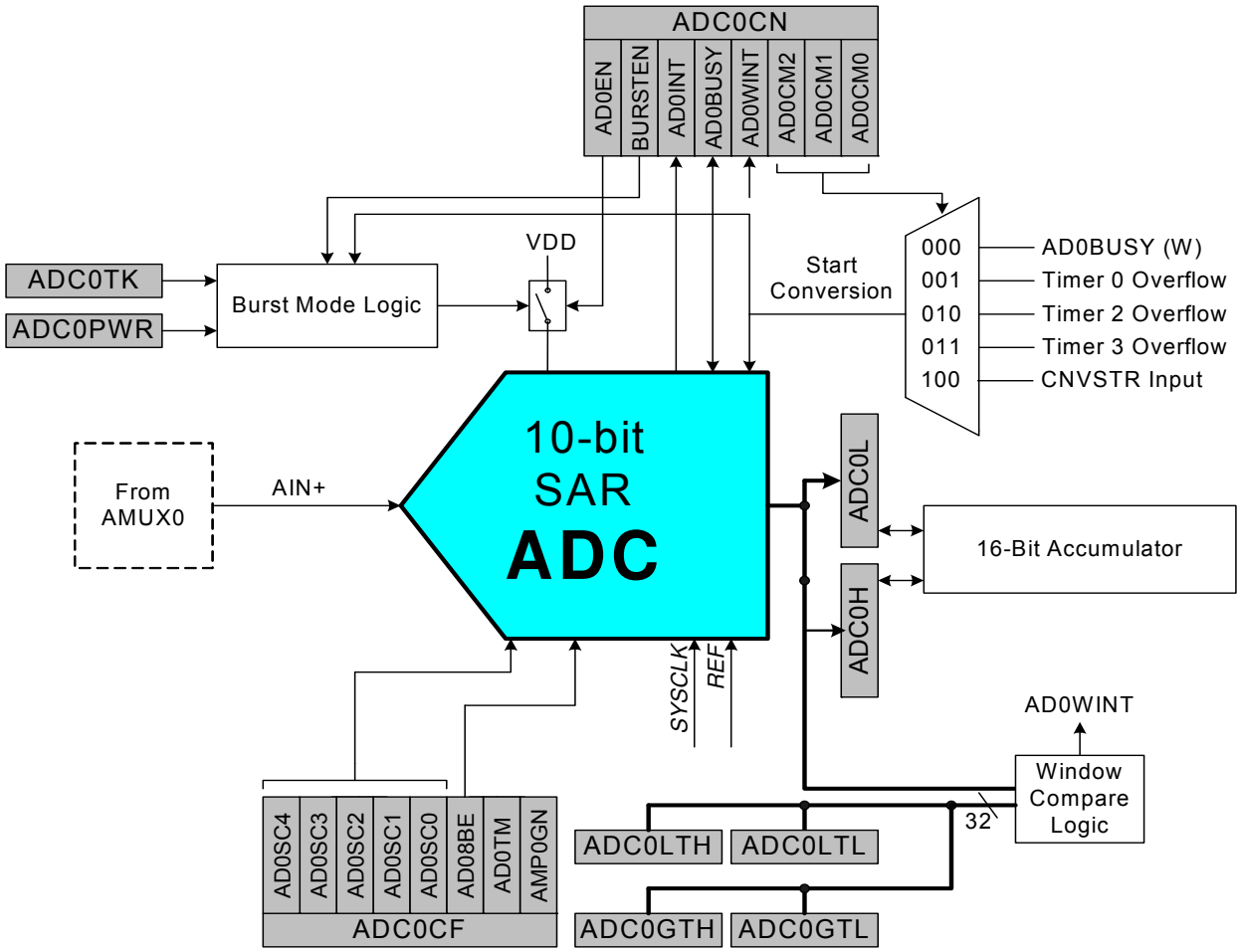

Figure 1.11. ADC0 Functional Block Diagram