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Si1010/1/2/3/4/5

Ultra Low Power, 64/32 kB, 10-Bit ADC MCU with Integrated 240–960 MHz EZRadioPRO® Transceiver

Ultra Low Power: 0.9 to 3.6 V Operation

- Typical sleep mode current < 0.1 µA; retains state and RAM contents over full supply range; fast wakeup of < 2 µs
- Less than 600 nA with RTC running
- Less than 1 µA with RTC running and radio state retained
- On-chip dc-dc converter allows operation down to 0.9 V.
- Two built-in brown-out detectors cover sleep and active modes

10-Bit or 12-Bit Analog to Digital Converter

- Up to 300 ksps
- Up to 18 external inputs
- External pin or internal VREF (no external capacitor required)
- Built-in temperature sensor
- External conversion start input option
- Autonomous burst mode with 16-bit automatic averaging accumulator

Dual Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5 µA)

On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 768 bytes RAM 16 kB (Si1010/2/4) or 8 kB (Si1011/3/5) Flash; In-system programmable

EZRadioPRO® Transceiver

- Frequency range = 240–960 MHz
- Sensitivity = –121 dBm
- FSK, GFSK, and OOK modulation
- Max output power = +20 dBm (Si1010/1), +13 dBm (Si1012/3/4/5)
- RF power consumption
  - 18.5 mA receive
  - 18 mA @ +1 dBm transmit
  - 30 mA @ +13 dBm transmit
  - 85 mA @ +20 dBm transmit (Si1010/1)
- Data rate = 0.123 to 256 kbps
- Auto-frequency calibration (AFC)
- Antenna diversity and transmit/receive switch control
- Programmable packet handler
- TX and RX 64 byte FIFOs
- Frequency hopping capability
- On-chip crystal tuning

Digital Peripherals

- 12 port I/O plus 3 GPIO pins; Hardware enhanced UART, SPI, and I^2C serial ports available concurrently
- Low power 32-bit SmaRTClock
- Four general purpose 16-bit counter/timers; six channel programmable counter array (PCA)

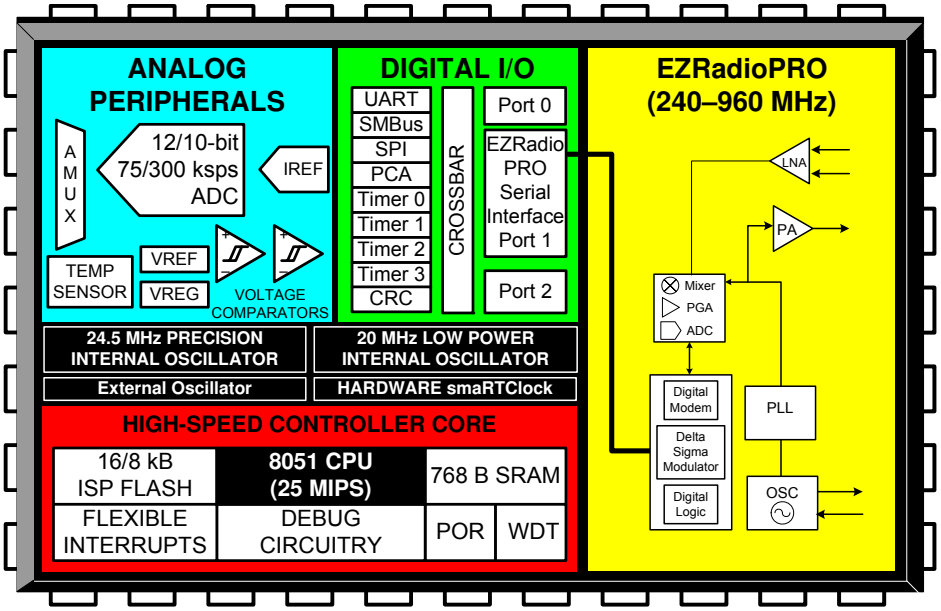
Clock Sources

- Precision internal oscillators: 24.5 MHz with ±2% accuracy supports UART operation; spread-spectrum mode for reduced EMI; Low power 20 MHz internal oscillator
- External oscillator: Crystal, RC, C, CMOS clock
- SmaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in power saving modes and in implementing various power saving modes

Package

- 42-pin LGA (5 x 7 mm)

Temperature Range: –40 to +85 °C



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1. System Overview

Si1010/1/2/3/4/5 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- 240–960 MHz EZRadioPRO® transceiver
- Single/Dual Battery operation with on-chip dc-dc boost converter.
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 10-bit 300 ksps or 12-bit 75 ksps single-ended ADC with analog multiplexer
- 6-Bit Programmable Current Reference. Resolution can be increased with PWM.
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology.
- 16 kB or 8 kB of on-chip Flash memory
- 768 bytes of on-chip RAM
- SMBus/I^2C, Enhanced UART, and two Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- Two On-chip Voltage Comparators with 11 Capacitive Touch Sense inputs.
- 15 Port I/O (5 V tolerant except for GPIO_0, GPIO_1, and GPIO_2)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the Si1010/1/2/3/4/5 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 0.9 to 1.8 V, 0.9 to 3.6 V or 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. The Si1010/1/2/3/4/5 devices are available in a 42-pin LGA package which is lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.4.

The transceiver's extremely low receive sensitivity (–121 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. The advanced radio features including continuous frequency coverage from 240–960 MHz in 156 Hz or 312 Hz steps allow precise tuning control. Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption. The transceivers digital receive architecture features a high-performance ADC and DSP-based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance. The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading, ensuring compliance with global regulations including FCC, ETSI, ARIB, and 802.15.4d regulations. An easy-to-use calculator is provided to quickly configure the radio settings, simplifying customer's system design and reducing time to market.

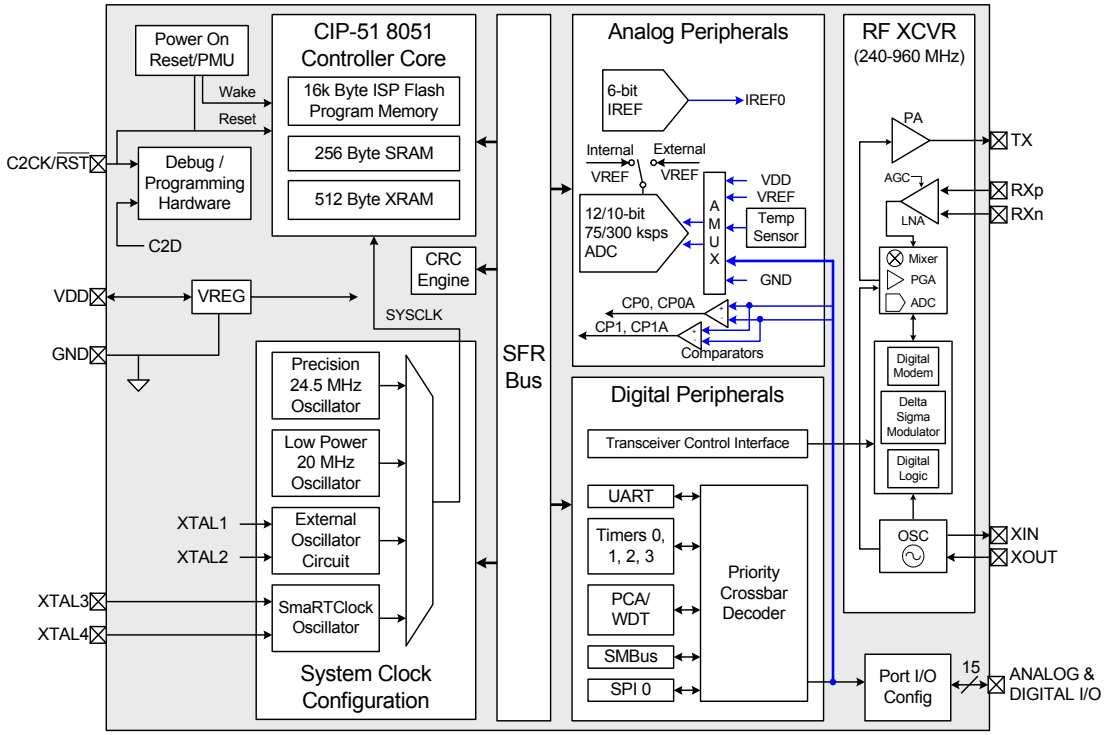

Figure 1.1. Si1010 Block Diagram

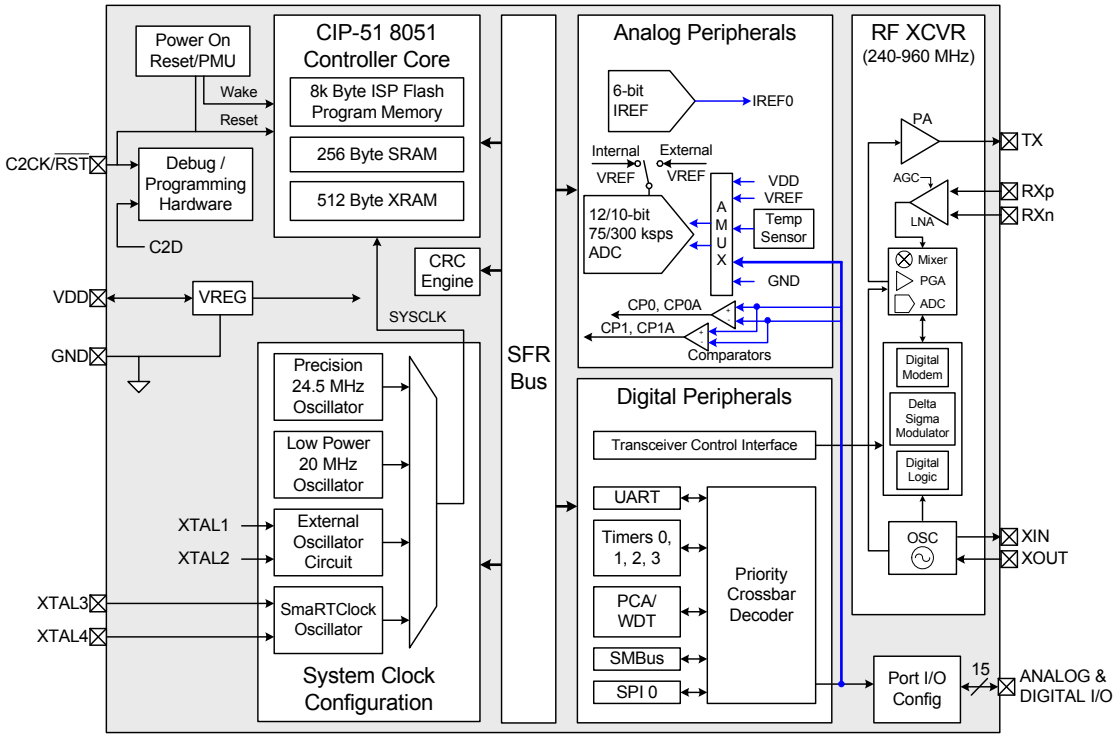

Figure 1.2. Si1011 Block Diagram

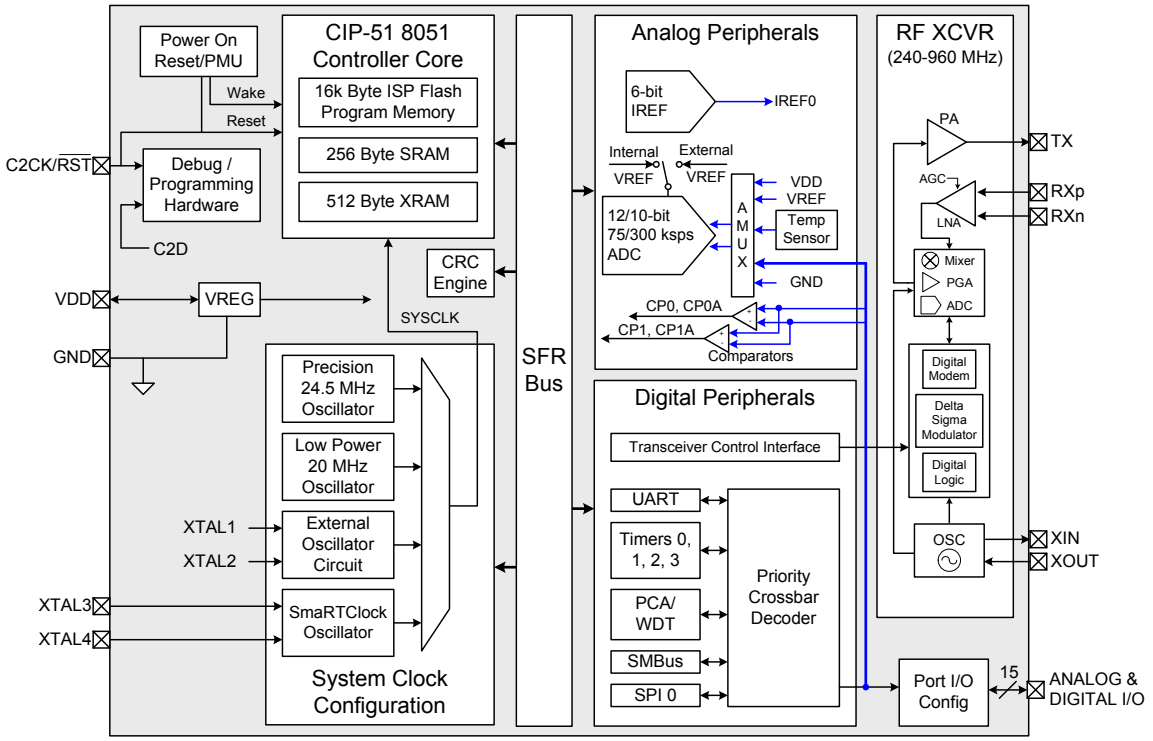

Figure 1.3. Si1012 Block Diagram

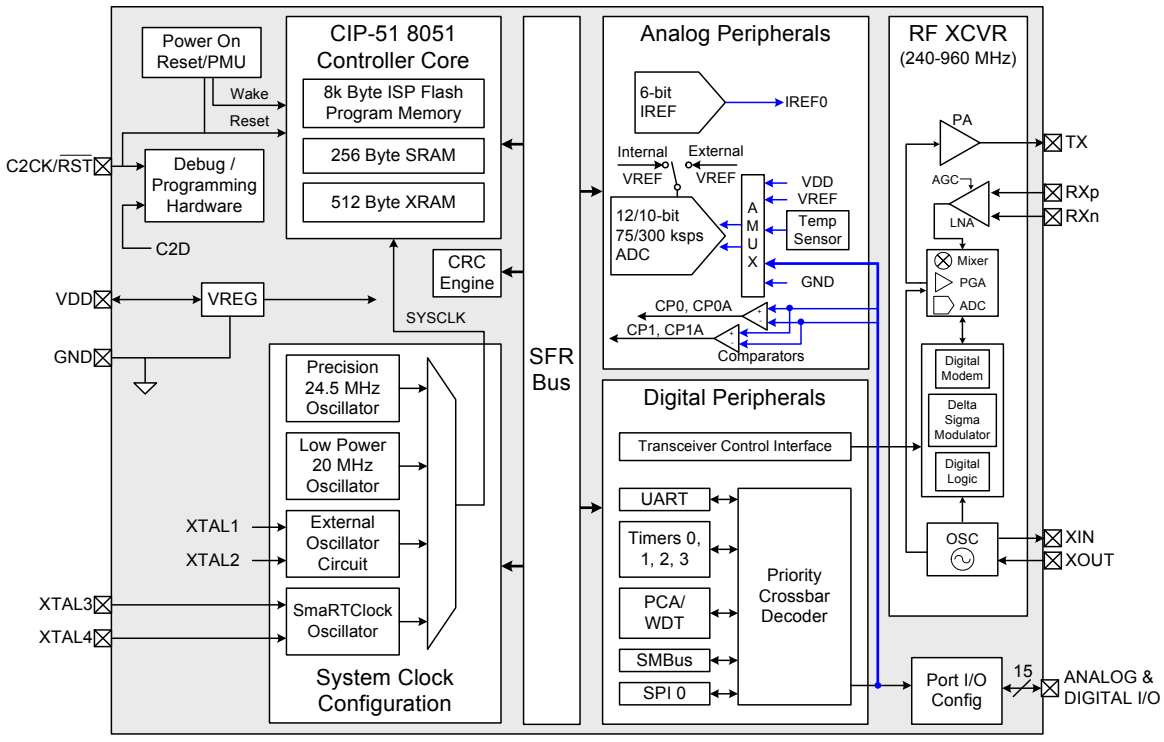

Figure 1.4. Si1013 Block Diagram

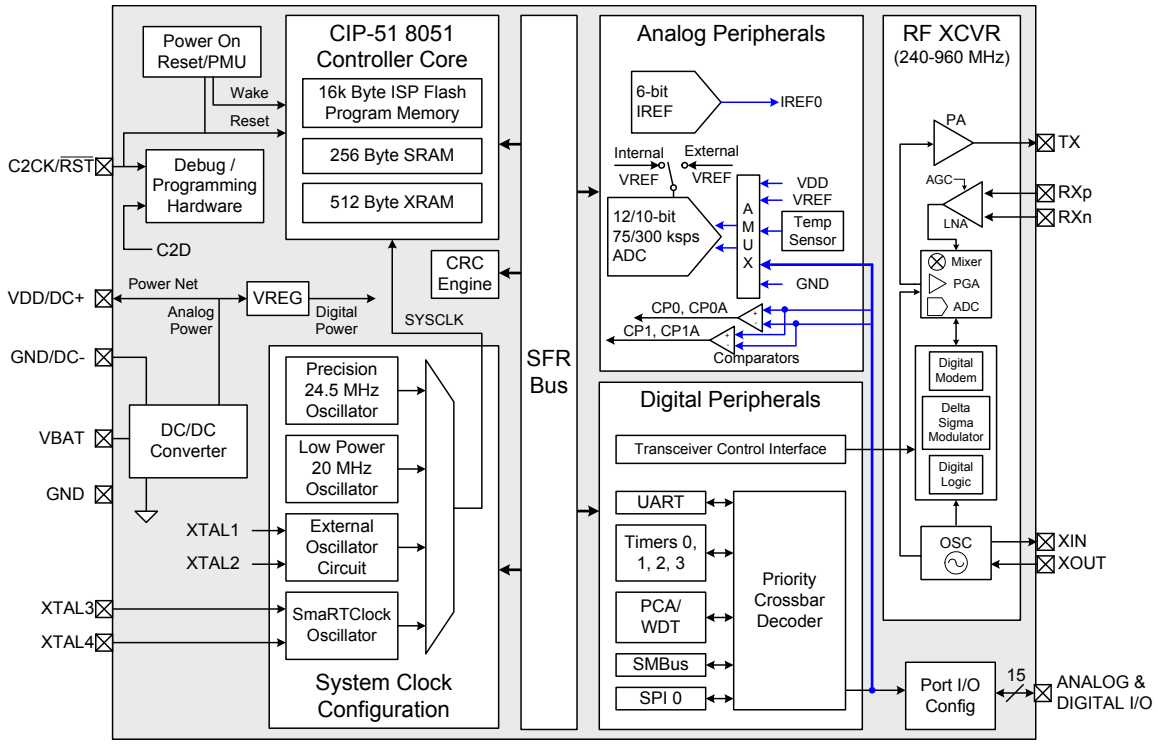

Figure 1.5. Si1014 Block Diagram

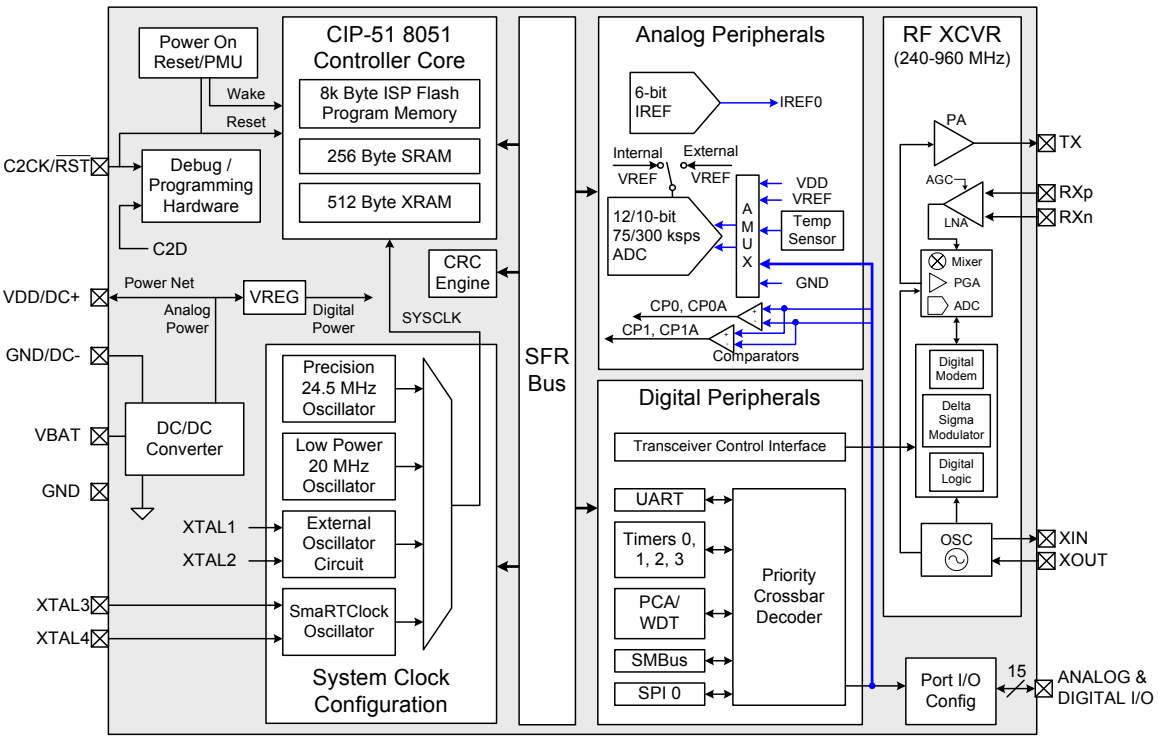

Figure 1.6. Si1015 Block Diagram

1.1. Typical Connection Diagram

The application shown in Figure 1.7 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A complete direct-tie reference design is available from Silicon Laboratories applications support.

For applications seeking improved performance in the presence of multipath fading, antenna diversity can be used. Antenna diversity support is integrated into the EZRadioPRO transceiver and can improve the system link budget by 8–10 dB in the presence of these fading conditions, resulting in substantial range increases. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

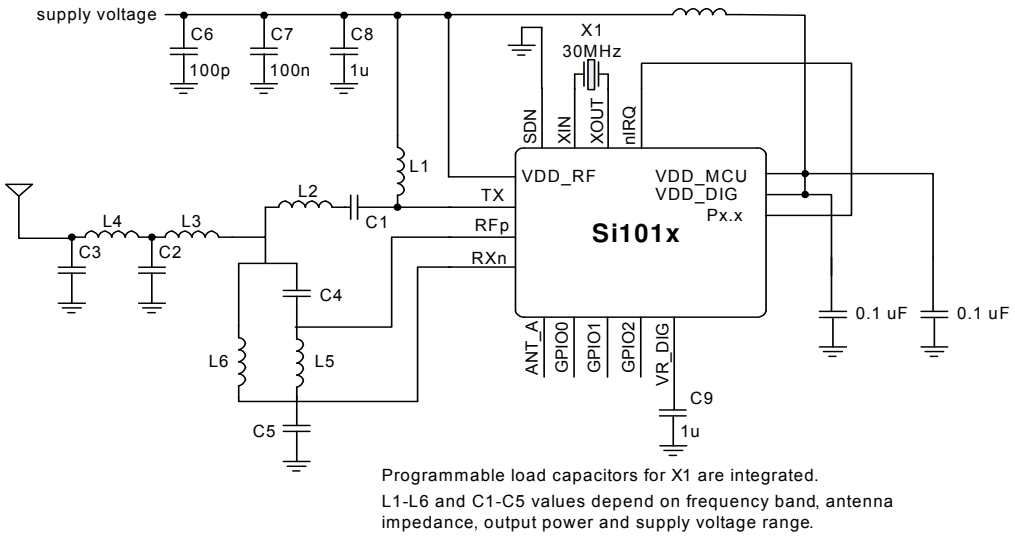

Figure 1.7. Si1012/3 RX/TX Direct-Tie Application Example

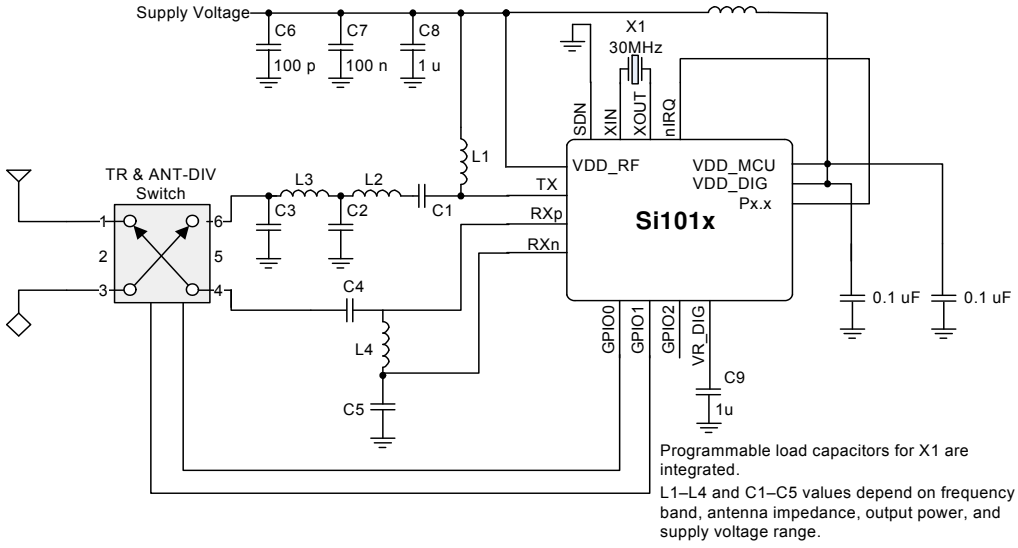

Figure 1.8. Si1010/1 Antenna Diversity Application Example

1.2. CIP-51™ Microcontroller Core

1.2.1. Fully 8051 Compatible

The Si1010/1/2/3/4/5 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.2.3. Additional Features

The Si1010/1/2/3/4/5 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a Watchdog Timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz and is accurate to ±2% over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.