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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
N-Channel	20	0.70 at $V_{GS} = 4.5$ V	600
		0.85 at $V_{GS} = 2.5$ V	500
		1.25 at $V_{GS} = 1.8$ V	350
P-Channel	- 20	1.2 at $V_{GS} = - 4.5$ V	- 400
		1.6 at $V_{GS} = - 2.5$ V	- 300
		2.7 at $V_{GS} = - 1.8$ V	- 150

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 2000 V ESD Protection
- Very Small Footprint
- High-Side Switching
- Low On-Resistance:
N-Channel, 0.7 Ω
P-Channel, 1.2 Ω
- Low Threshold: ± 0.8 V (Typ.)
- Fast Switching Speed: 14 ns
- 1.8 V Operation
- Compliant to RoHS Directive 2002/95/EC



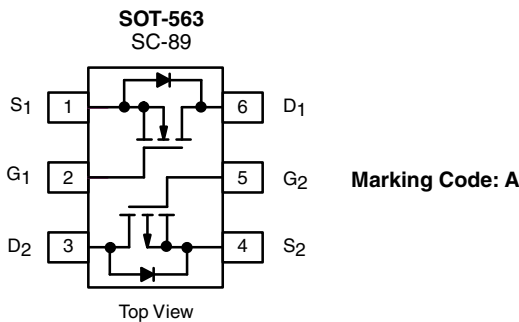
RoHS
COMPLIANT
HALOGEN
FREE

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits



Ordering Information: Si1016X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		5 s	Steady State	5 s	Steady State		
Drain-Source Voltage	V_{DS}	20		- 20		V	
Gate-Source Voltage	V_{GS}	± 6					
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	515	485	- 390	- 370	mA
		$T_A = 85$ °C	370	350	- 280	- 265	
Pulsed Drain Current ^b	I_{DM}	650		- 650			
Continuous Source Current (Diode Conduction) ^a	I_S	450	380	- 450	- 380	mW	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	280	250	280		250
		$T_A = 85$ °C	145	130	145		130
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150				°C	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000				V	

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	0.45		1	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-0.45		-1	
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 4.5\ \text{V}$	N-Ch P-Ch		± 0.5 ± 1.0	± 1.0 ± 2.0	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\ \text{V}, V_{GS} = 0\ \text{V}$	N-Ch		0.3	100	nA
		$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}$	P-Ch		-0.3	-100	
		$V_{DS} = 16\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85\text{ }^\circ\text{C}$	N-Ch			5	μA
		$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85\text{ }^\circ\text{C}$	P-Ch			-5	
On State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	N-Ch	700			mA
		$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	P-Ch	-700			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 600\ \text{mA}$	N-Ch		0.41	0.70	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -350\ \text{mA}$	P-Ch		0.80	1.2	
		$V_{GS} = 2.5\ \text{V}, I_D = 500\ \text{mA}$	N-Ch		0.53	0.85	
		$V_{GS} = -2.5\ \text{V}, I_D = -300\ \text{mA}$	P-Ch		1.20	1.6	
		$V_{GS} = 1.8\ \text{V}, I_D = 350\ \text{mA}$	N-Ch		0.70	1.25	
		$V_{GS} = -1.8\ \text{V}, I_D = -150\ \text{mA}$	P-Ch		1.80	2.7	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 400\ \text{mA}$	N-Ch		1.0		S
		$V_{DS} = -10\ \text{V}, I_D = -250\ \text{mA}$	P-Ch		0.4		
Diode Forward Voltage ^a	V_{SD}	$I_S = 150\ \text{mA}, V_{GS} = 0\ \text{V}$	N-Ch		0.8	1.2	V
		$I_S = -150\ \text{mA}, V_{GS} = 0\ \text{V}$	P-Ch		-0.8	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 250\ \text{mA}$ P-Channel $V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -250\ \text{mA}$	N-Ch		750		pC
Gate-Source Charge	Q_{gs}		N-Ch		75		
			P-Ch		150		
Gate-Drain Charge	Q_{gd}	N-Ch		225			
		P-Ch		450			
Turn-On Time	t_{ON}	N-Channel $V_{DD} = 10\ \text{V}, R_L = 47\ \Omega$ $I_D \cong 200\ \text{mA}, V_{GEN} = 4.5\ \text{V}, R_g = 10\ \Omega$ P-Channel $V_{DD} = -10\ \text{V}, R_L = 47\ \Omega$ $I_D \cong -200\ \text{mA}, V_{GEN} = -4.5\ \text{V}, R_g = 10\ \Omega$	N-Ch		5		ns
Turn-Off Time	t_{OFF}		N-Ch		25		
		P-Ch		35			

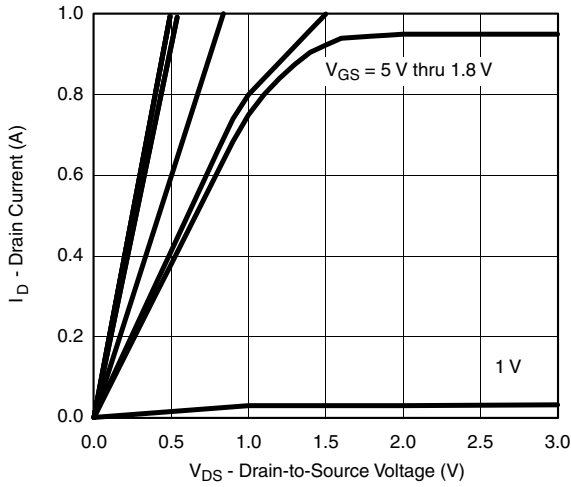
Notes:

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

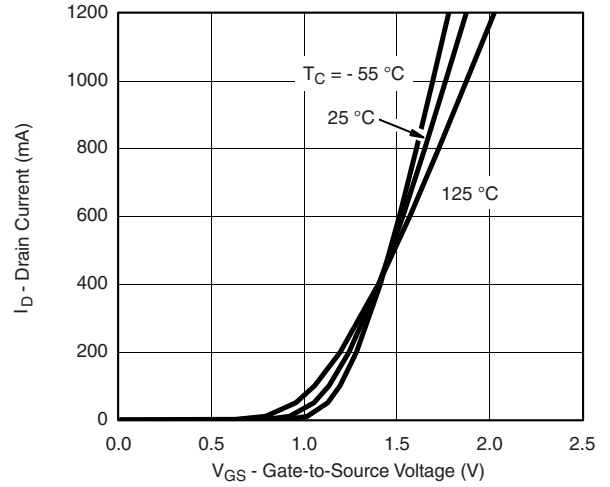
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

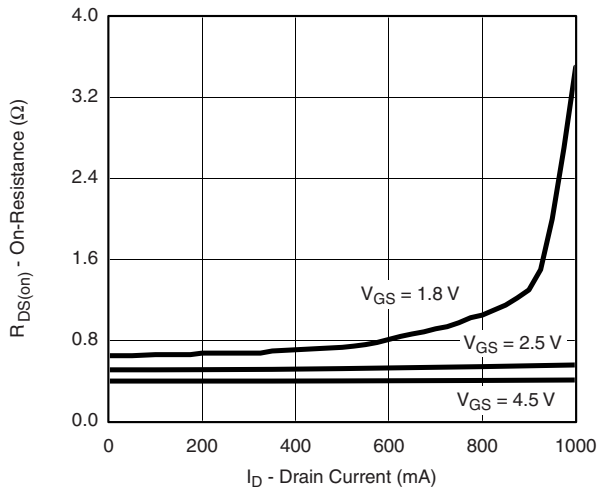
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



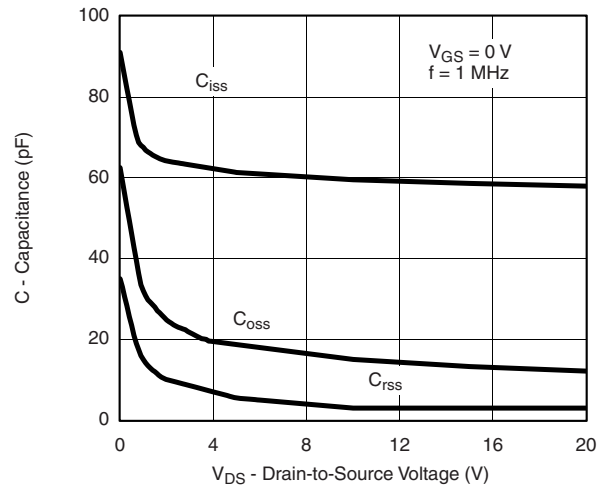
Output Characteristics



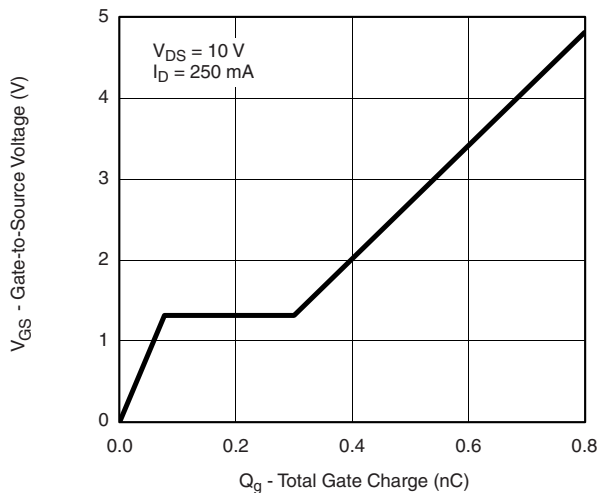
Transfer Characteristics



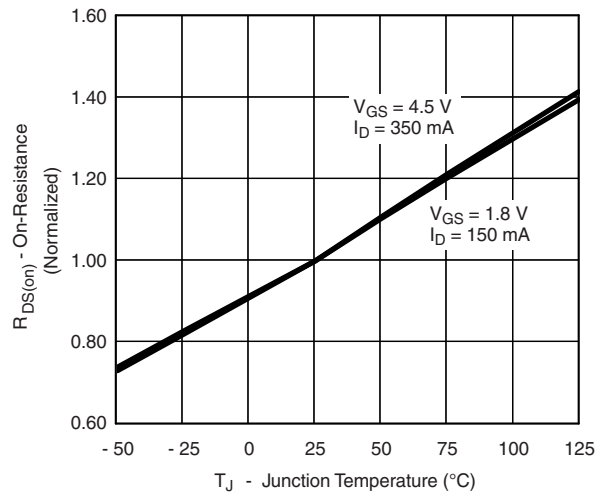
On-Resistance vs. Drain Current



Capacitance

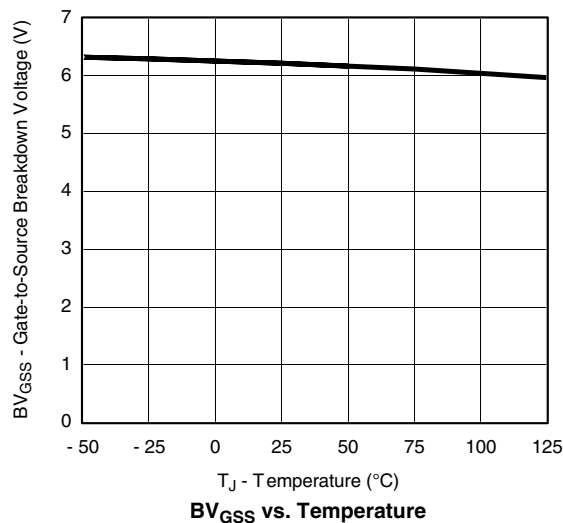
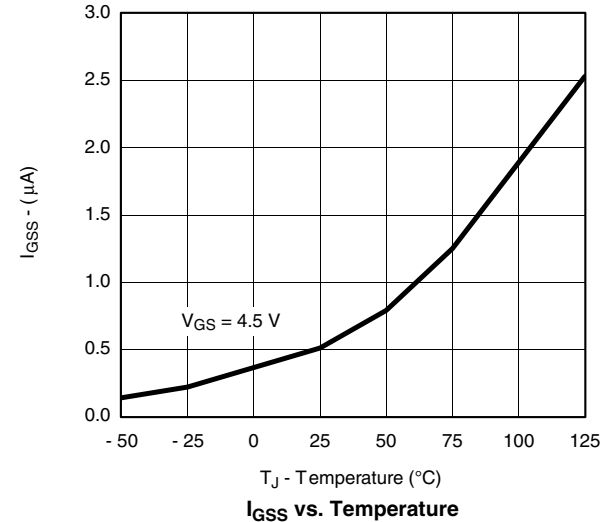
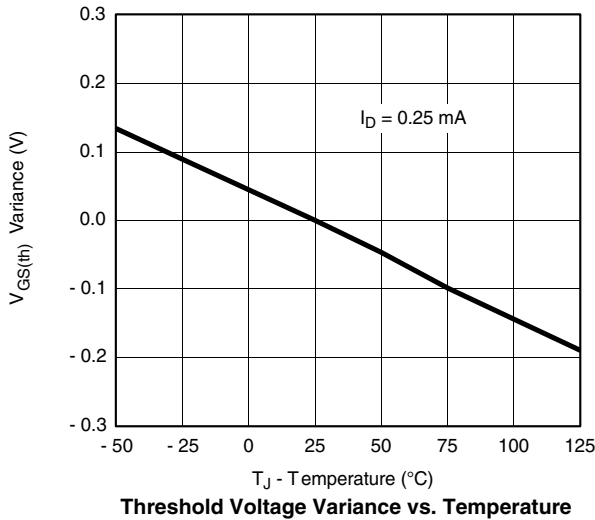
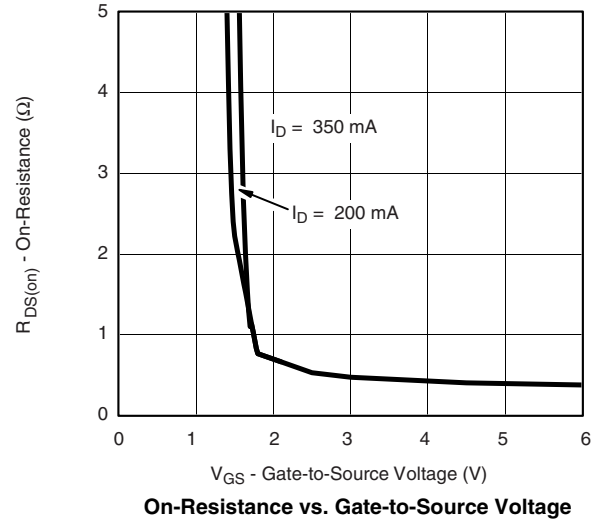
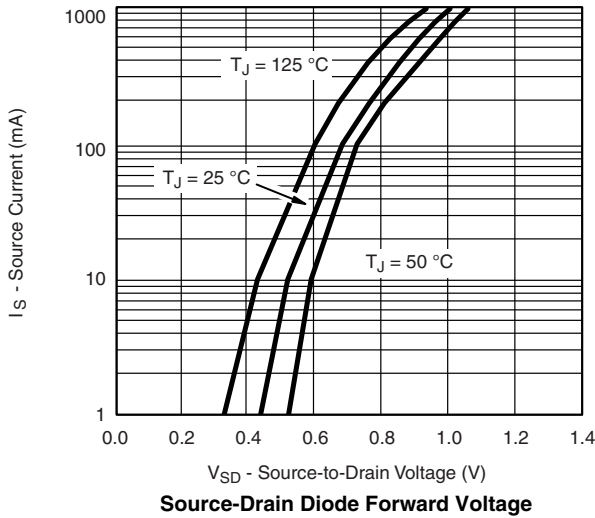


Gate Charge

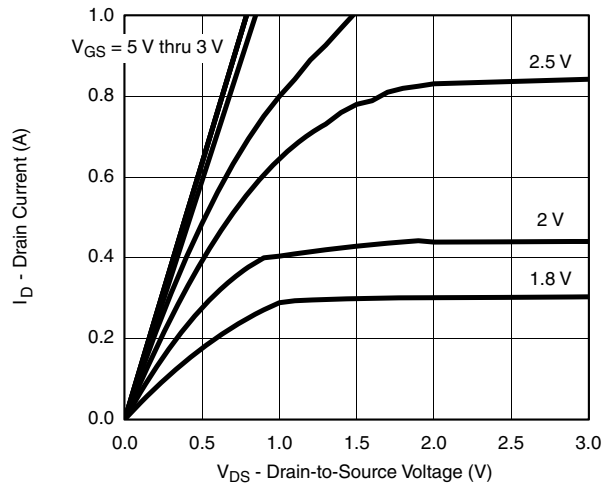


On-Resistance vs. Junction Temperature

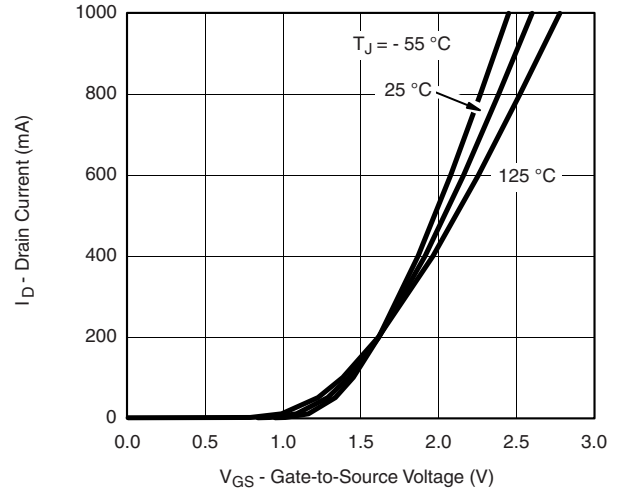
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



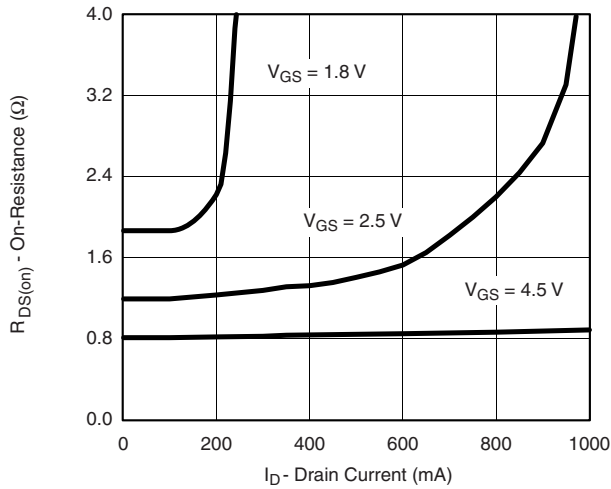
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



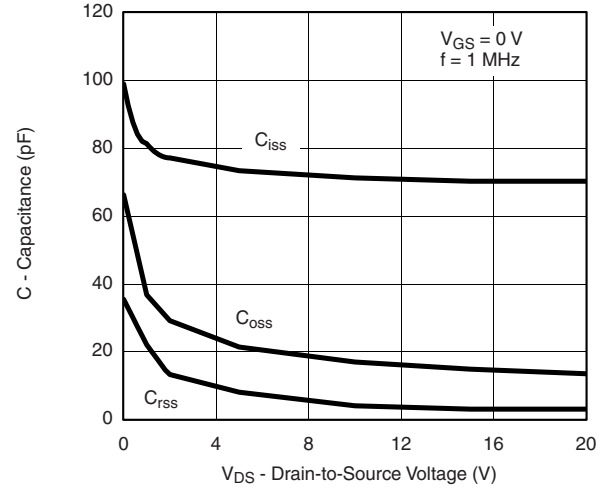
Output Characteristics



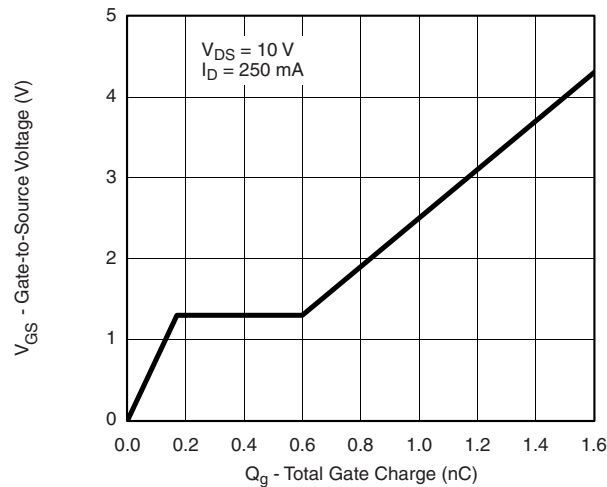
Transfer Characteristics



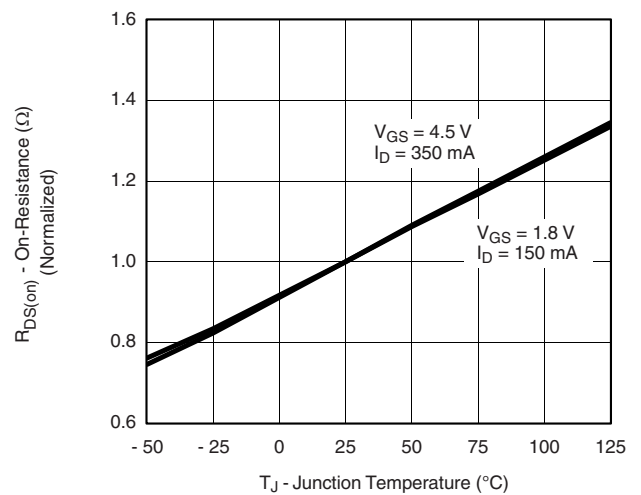
On-Resistance vs. Drain Current



Capacitance

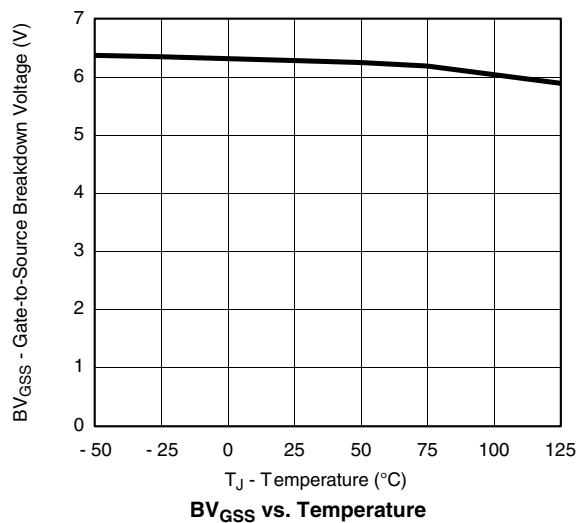
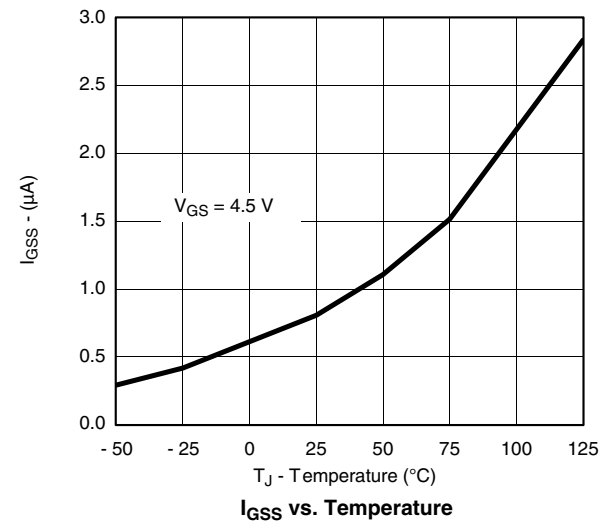
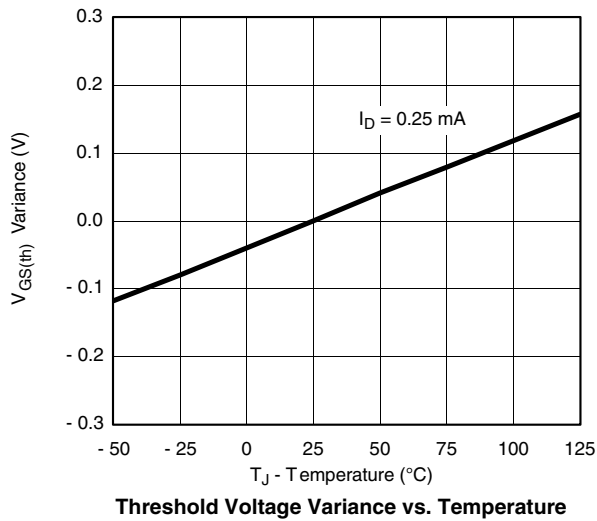
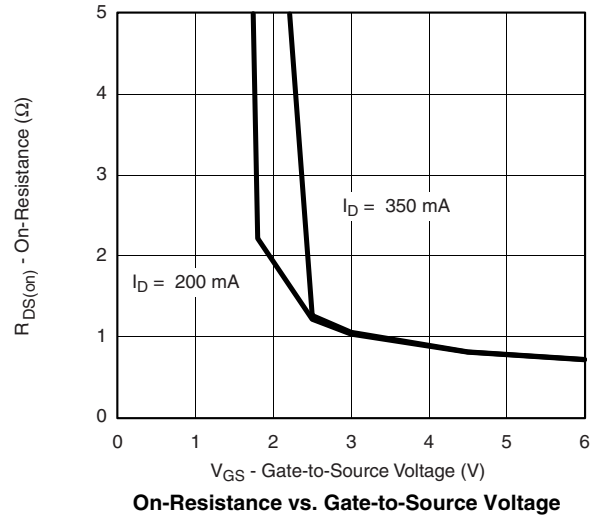
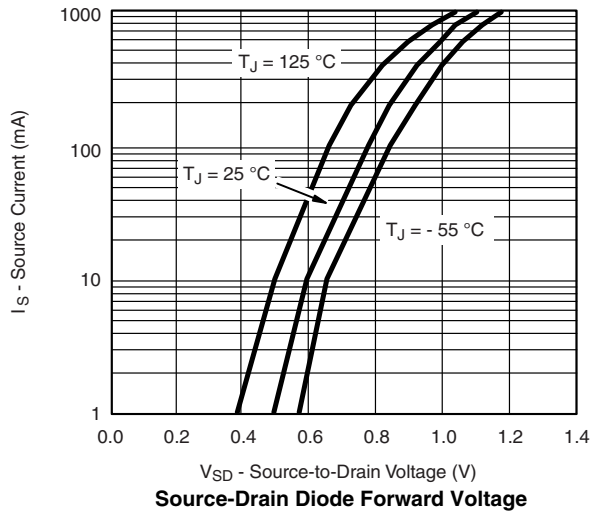


Gate Charge

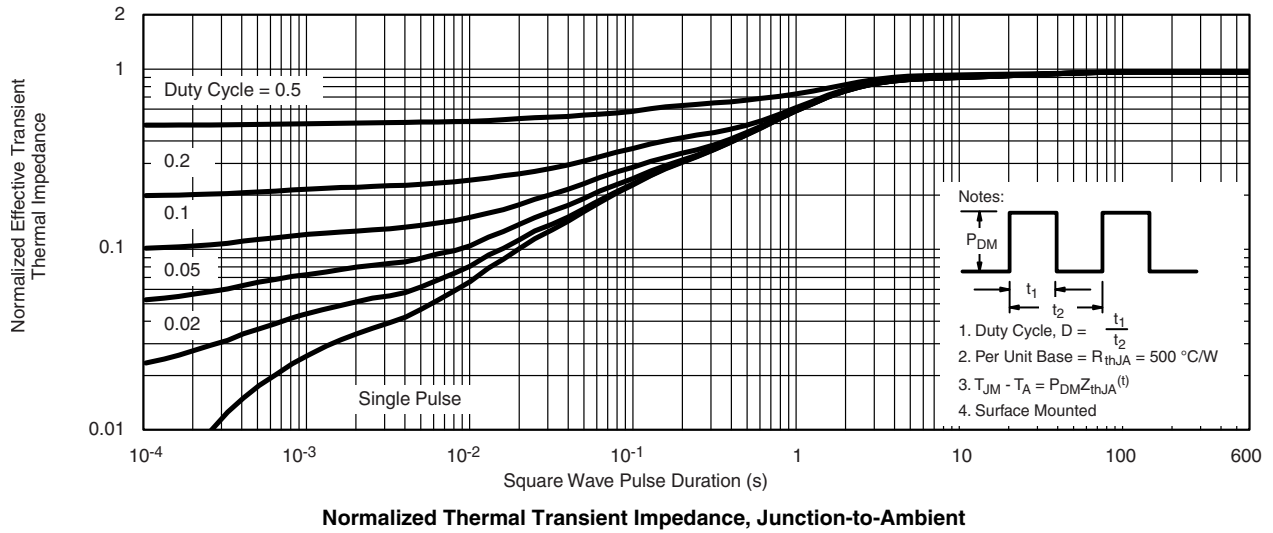


On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

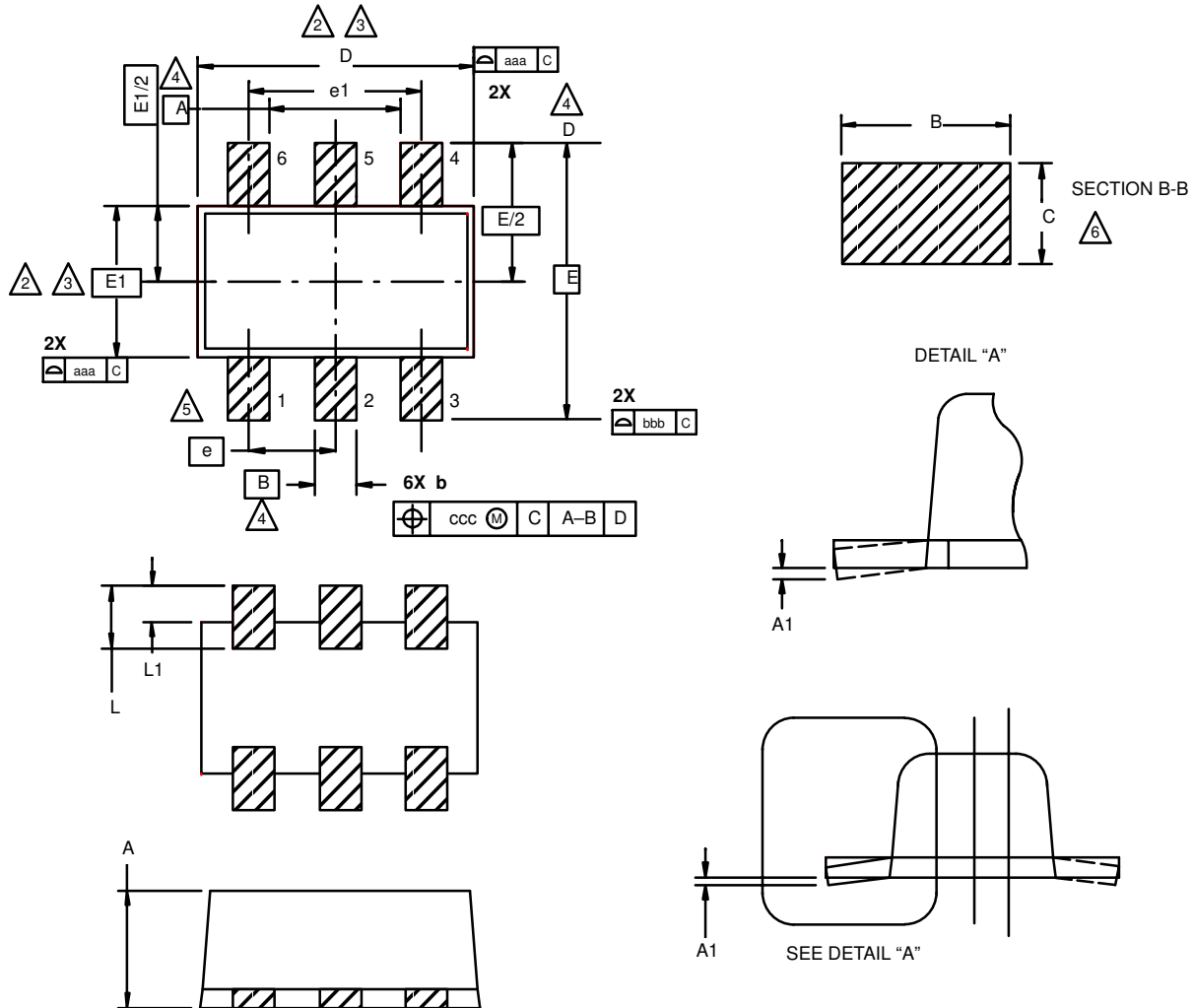


N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71168.

SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.

2 Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

3 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

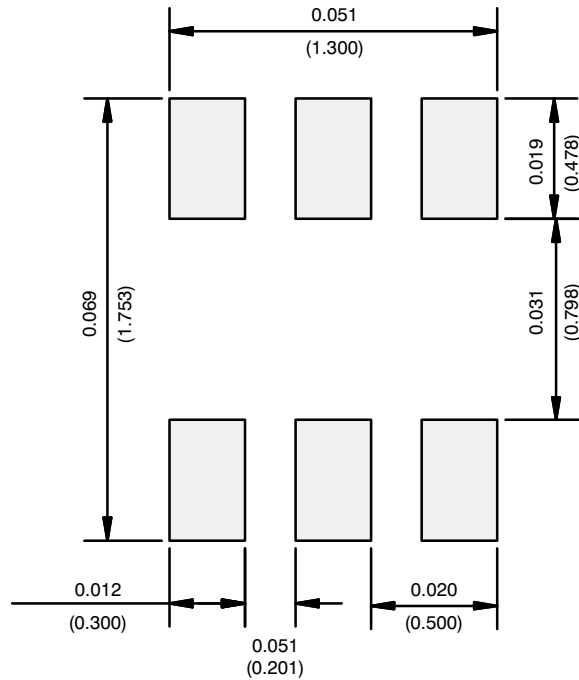
4 Datums A, B and D to be determined 0.10 mm from the lead tip.

5 Terminal numbers are shown for reference only.

6 These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

Dim	MILLIMETERS		Note	Symbol	Tolerances Of Form And Position
	Min	Max			
A	0.56	0.60		aaa	0.10
A1	0.00	0.10		bbb	0.10
b	0.15	0.30		ccc	0.10
c	0.10	0.18			
D	1.50	1.70	2, 3		
E	1.55	1.70			
E1	1.20 BSC		2, 3		
e	0.50 BSC				
e1	1.00 BSC				
L	0.35 BSC				
L1	0.20 BSC				
ECN: E-00499—Rev. B, 02-Jul-01 DWG: 5880					

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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