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Si102x/3x

Ultra Low Power, 64/32 kB, 10-Bit ADC MCU with Integrated 240–960 MHz EZRadioPRO® Transceiver

Ultra Low Power at 3.6V

- 130 µA/MHz IBAT; dc-dc enabled
- 110 nA sleep current with data retention; POR monitor enabled
- 400 nA sleep current with smaRTClock (internal LFO)
- 700 nA sleep current with smaRTClock (external XTAL)
- 2 µs wake-up from any sleep mode

12-Bit; 16 Ch. Analog-to-Digital Converter

- Up to 75 ksps 12-bit mode or 300 ksps 10-bit mode
- External pin or internal VREF (no external capacitor required)
- On-chip PGA allows measuring voltages up to twice the reference voltage
- Autonomous burst mode with 16-bit automatic averaging accumulator
- Integrated temperature sensor

Two Low Current Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source

Internal 6-Bit Current Reference

- Up to ±500 µA; source and sink capability
- Enhanced resolution via PWM interpolation

Integrated LCD Controller (Si102x Only)

- Supports up to 128 segments (32x4)
- Integrated charge pump for contrast control

Metering-Specific Peripherals

- DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output)
- Sleep-mode pulse accumulator with programmable switch de-bounce and pull-up control interfaces directly to metering sensor
- Dedicated Packet Processing Engine (DPPE) includes hardware AES, DMA, CRC, and encoding blocks for acceleration of wireless protocols
- Manchester and 3 out of 6 encoder hardware for power efficient implementation of the wireless M-bus specification

EZRadioPRO® Transceiver

- Frequency range = 240–960 MHz
- Sensitivity = –121 dBm
- FSK, GFSK, and OOK modulation
- Max output power = +20 dBm or +13 dBm
- RF power consumption
  - 18.5 mA receive
  - 18 mA @ +1 dBm transmit
  - 30 mA @ +13 dBm transmit
  - 85 mA @ +20 dBm transmit
  - Data rate = 0.123 to 256 kbps
  - Auto-frequency calibration (AFC)
  - Antenna diversity and transmit/receive switch control
  - Programmable packet handler
  - TX and RX 64-byte FIFOs
  - Frequency hopping capability
  - On-chip crystal tuning

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks

Memory

- Up to 128 kB Flash; In-system programmable; Full read/write/erase functionality over the entire supply range
- Up to 8 kB internal data RAM

Digital Peripherals

- 53 port I/O; All 5 V tolerant with high sink current and programmable drive strength
- Hardware SMBus™ (I2C™ compatible), 2 x SPI™, and UART serial ports available concurrently
- Four general-purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with six capture/compare modules and watchdog timer

Clock Sources

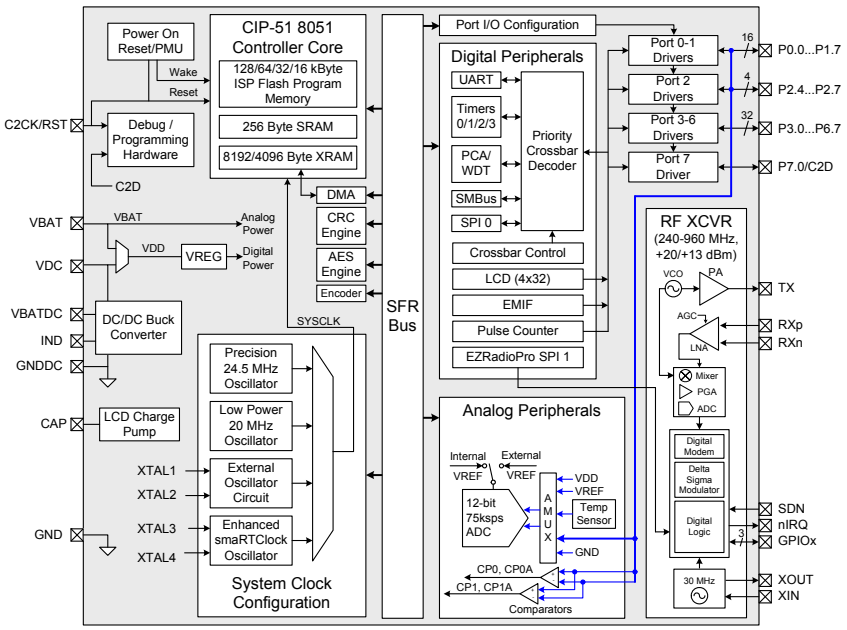
- Precision internal oscillators: 24.5 MHz with ±2% accuracy supports UART operation; spread-spectrum mode for reduced EMI
- Low power internal oscillator: 20 MHz
- External oscillator: Crystal, RC, C, CMOS clock
- smaRTClock oscillator: 32.768 kHz crystal or 16.4 kHz internal LFO with three independent alarms

On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive, in-system debug (no emulator required)
- Provides 4 breakpoints, single stepping

Packages

- –85 pin LGA (6 x 8 mm)



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1. System Overview

Si102x/3x devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- 240-960 MHz EZRadioPRO® transceiver
- Power efficient on-chip dc-dc buck converter
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 300 ksps, or 12-bit 75 ksps single-ended ADC with 16 external analog inputs and 4 internal inputs such as various power supply voltages and the temperature sensor
- 6-bit programmable current reference
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology
- 128 kB, 64 kB, 32 kB, or 16 kB of on-chip flash memory
- 8448 or 4352 bytes of on-chip RAM
- 128 segment LCD driver
- SMBus/I^2C, enhanced UART, and two enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with six capture/compare modules and watchdog timer function
- Hardware AES, DMA, and pulse counter
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- Two on-chip voltage comparators
- 53-port I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the Si102x/3x devices are truly stand-alone system-on-a-chip solutions. The flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-wire (C2) development interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The port I/O and $\overline{RST}$ pins are tolerant of input signals up to VIO + 2.0 V. The Si102x/3x devices are available in an 85-pin LGA package that is lead-free and RoHS-compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 and Figure 1.2.

The transceiver's extremely low receive sensitivity (–121 dBm) coupled with industry leading +13 or +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. The advanced radio features including continuous frequency coverage from 240–960 MHz in 156 Hz or 312 Hz steps allow precise tuning control. Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption.