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Si106x/108x

Ultra Low Power, 64/32 kB, 10-Bit ADC

MCU with Integrated 240–960 MHz EZRadioPRO® Transceiver

Ultra-low power 8051 µC Core

- 25 MHz, single-cycle 8051 compatible CPU
  - 25 MIPS peak throughput with 25 MHz clock
- Industry's lowest active and sleep currents
- 160 µA/MHz: active mode
- 10 nA sleep with brownout detectors disabled
- 50 nA sleep with brownout detectors enabled
- 600 nA sleep with internal RTC
- 2 µs wake-up time
- On-chip debug

Memory

- Up to 64 kB of flash and 4 kB of RAM

Peripherals

- 10-bit analog-to-digital converter
  - Temperature sensor
- Dual comparators
- 11 general purpose I/O
  - UART, SPI, I^2C
- Four general purpose 16-bit counter/timers
- Precision internal oscillators
  - 24.5 MHz with ±2% accuracy
  - Low power 20 MHz internal oscillator
- External oscillator: crystal, RC, C, CMOS clock
- RTC: 32.768 kHz crystal or self-oscillate

Transceiver Features (Si1060)

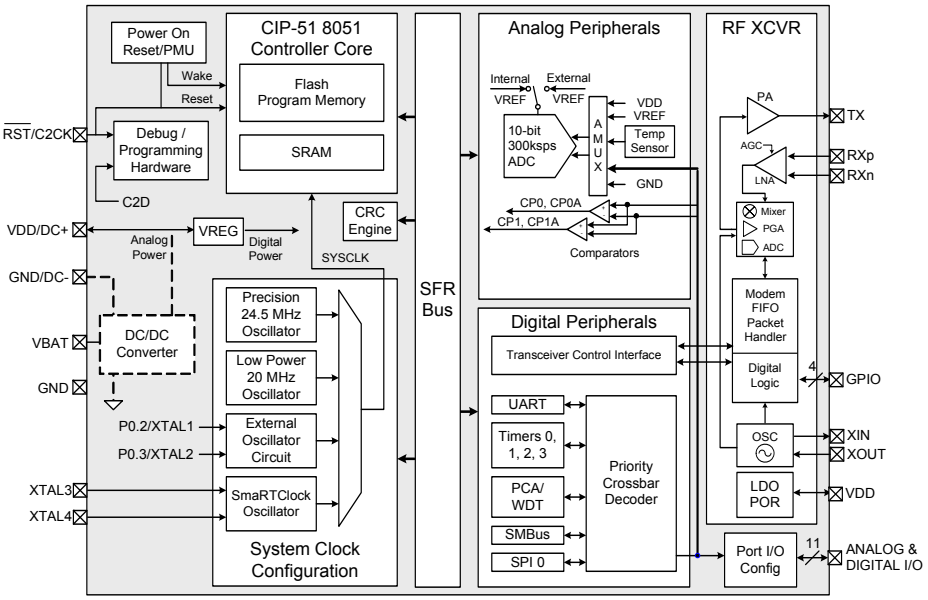
- Data rate up to 1 Mbps
- 142–1050 MHz frequency range
- On-chip crystal tuning
- –126 dBm receive sensitivity @ 500 bps, GFSK
- Modulation: OOK, (G)FSK, and 4(G)FSK
- Up to +20 dBm output power
- Low power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
  - 30 nA shutdown, 50 nA standby
  - Fast wake and hop times
- Excellent selectivity performance
  - 60 dB adjacent channel
  - 73 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- IEEE 802.15.4g compliant

System

- Supply voltage: 1.8 to 3.6 V
  - 0.9–3.6 V operation with built-in dc-dc converter
  - Brownout detectors cover sleep and active modes
- Low battery detector
- Low BOM count
- 5x6 36-pin QFN package

Applications

- Home automation
- Home security
- Remote control
- Garage door openers
- Remote keyless Entry
- Home health care
- Smart metering
- Building Lighting control
- Building HVAC control
- Fire and Security monitoring
- Security and Access control
- Telemetry



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1. System Overview

Silicon Laboratories' Si106x Wireless MCUs combine high-performance wireless connectivity and ultra-low power microcontroller processing into a small 5x6 mm form factor. Support for major frequency bands in the 142 to 1050 MHz range is provided including an integrated advanced packet handling engine and the ability to realize a link budget of up to 146 dB. The devices have been optimized to minimize energy consumption for battery-backed applications by minimizing TX, RX, active, and sleep mode current as well as supporting fast wake-up times. The Si106x and Si108x Wireless MCUs are pin-compatible and can scale from 8 to 64 kB of flash and provides a robust set of analog and digital peripherals including an ADC, dual comparators, timers, and GPIO. All devices are designed to be compliant with the 802.15.4g smart metering standard and support worldwide regulatory standards including FCC, ETSI, and ARIB. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the Si106x devices are truly standalone system-on-a-chip solutions. The flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). Select devices will work down to 0.9 V with the dc-dc boost converter, supporting operation on a single alkaline cell battery. The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The Si106x devices are available in a 36-pin QFN package (lead-free and RoHS compliant). See Table 2.1 for ordering information. See Figure 1.1 for the block diagram.

The transceiver's extremely low receive sensitivity (–126 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. The advanced radio supports major frequency bands in the 119 to 1050 MHz range. The Si106x family includes optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications such as FCC Part90 and 169 MHz wireless Mbus. The 60 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation.

The Si106x offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry-leading link budget of 146 dB allowing extended ranges and highly robust communication links. The active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The Si106x wireless MCUs can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices are highly flexible and can be configured via Silicon Labs' graphical configuration tools.

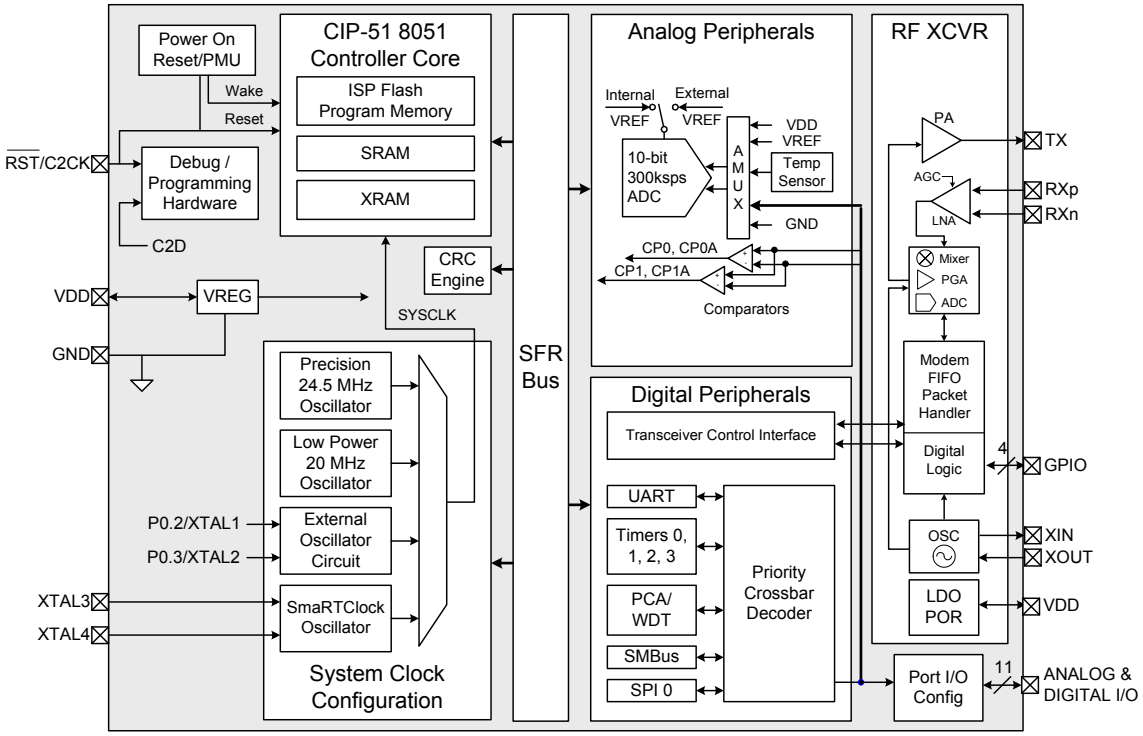

Figure 1.1. Si106x/Si108x Block Diagram

1.1. Typical Connection Diagram

The application shown in Figure 1.2 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A complete direct-tie reference design is available from Silicon Laboratories applications support.

For applications seeking improved performance in the presence of multipath fading, antenna diversity can be used. Antenna diversity support is integrated into the EZRadioPRO transceiver and can improve the system link budget by 8–10 dB in the presence of these fading conditions, resulting in substantial range increases. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

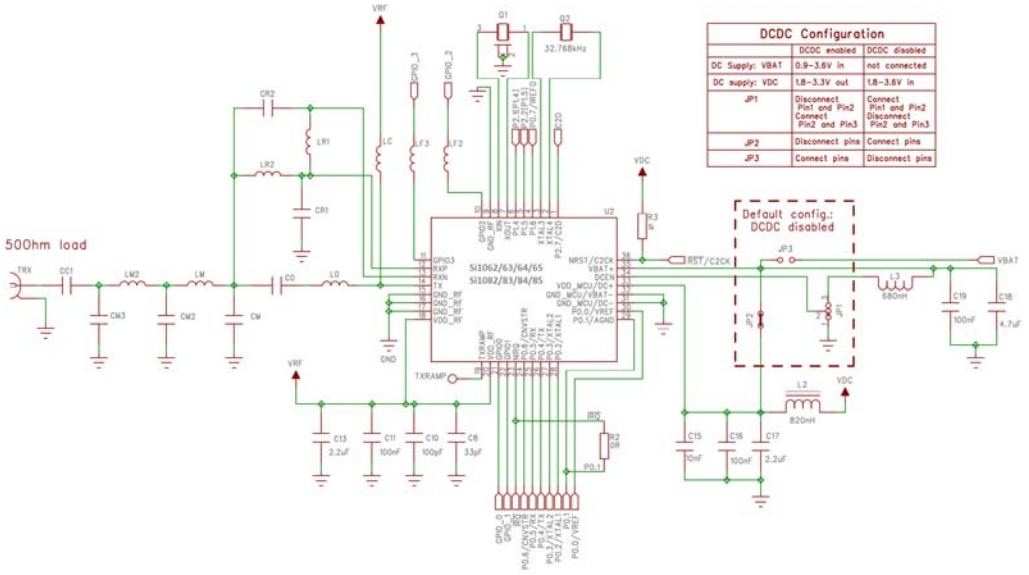

Figure 1.2. Si106x/108x RX/TX Direct-Tie Application Example

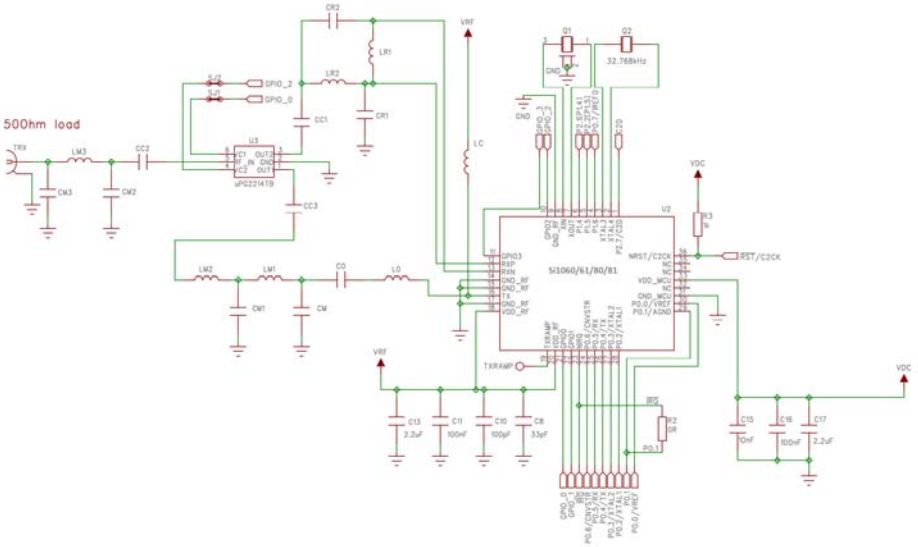

Figure 1.3. Si106x/108x Antenna Diversity Application Example

1.2. CIP-51™ Microcontroller Core

1.2.1. Fully 8051 Compatible

The Si106x/108x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.2.3. Additional Features

The Si106x/108x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51, allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a watchdog timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory is calibrated to 24.5 MHz and is accurate to ±2% over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

1.3. Port Input/Output

Digital and analog resources are available through 11 I/O pins. Four additional GPIO pins are available through the radio peripheral. Port pins are organized as three byte-wide ports. Port pins P0.0–P0.6 and P1.4–P1.6 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P2.7 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “33. Device Specific Behavior” on page 352 for more details.

The designer has complete control over which digital and analog functions are assigned to individual port pins and is limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “20.3. Priority Crossbar Decoder” on page 221 for more information on the crossbar.

All Px.x Port I/Os are 5 V tolerant when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the VDD_MCU supply. Port I/Os used for analog functions can operate up to the VDD_MCU supply voltage. See Section “20.1. Port I/O Modes of Operation” on page 218 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

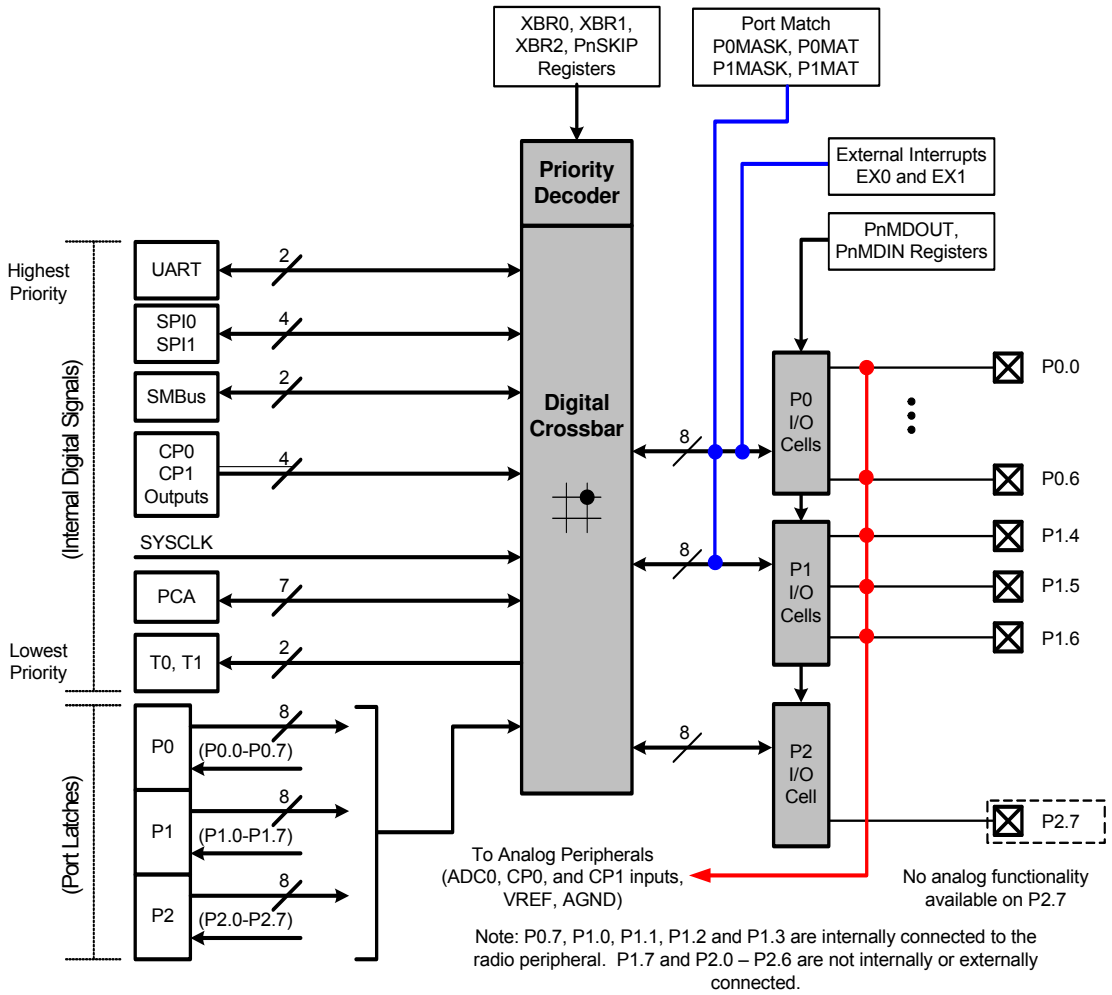

Figure 1.4. Port I/O Functional Block Diagram

1.4. Serial Ports

The Si106x/108x family includes an SMBus/I^2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention. There is also a dedicated radio serial interface (SPI1) to allow communication with the radio peripheral.

1.5. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with six programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8.

Each capture/compare module can be configured to operate in a variety of modes: edge-triggered capture, software timer, high-speed output, pulse width modulator (8, 9, 10, 11, or 16-bit), or frequency output. Additionally, Capture/Compare Module 5 offers watchdog timer capabilities. Following a system reset, Module 5 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

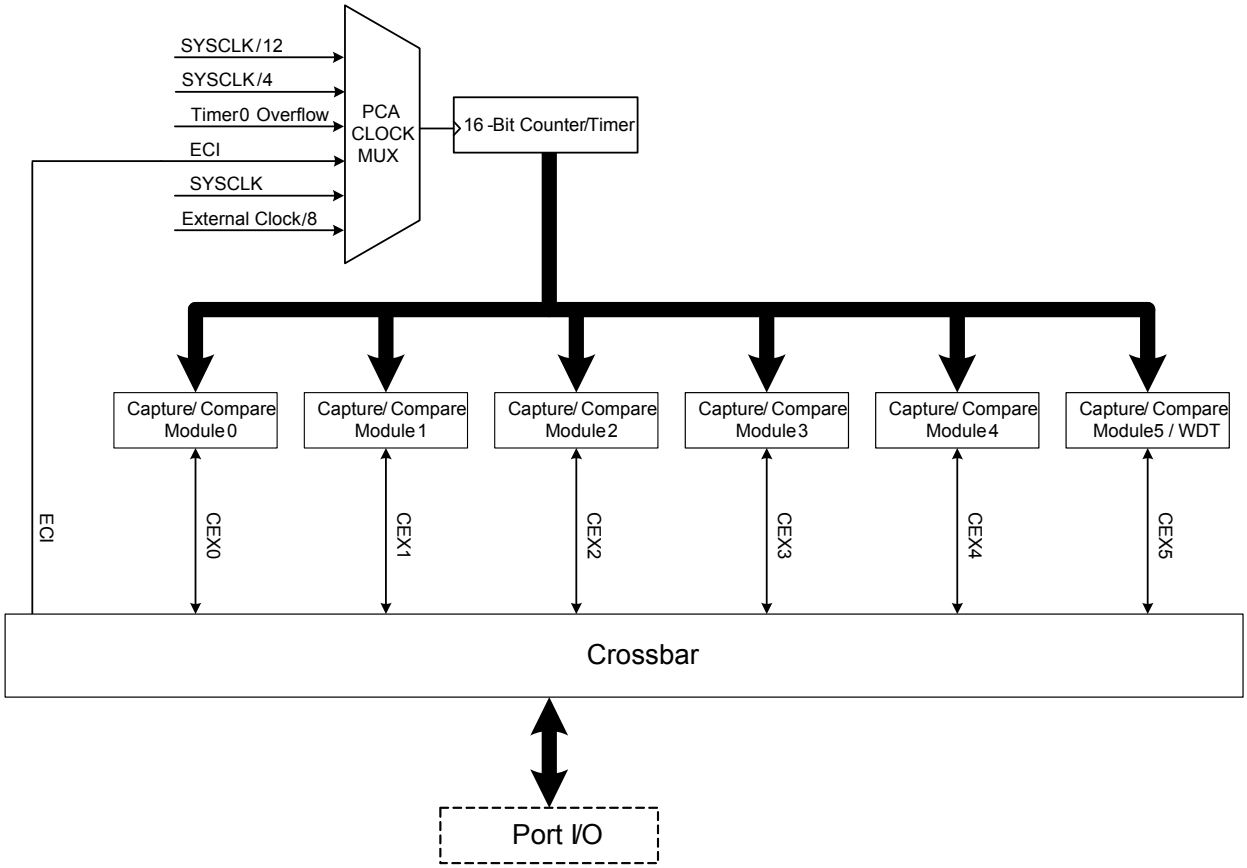

Figure 1.5. PCA Block Diagram

1.6. 10-bit SAR ADC with 16-bit Auto-Averaging Accumulator and Autonomous Low Power Burst Mode

Si106x/108x devices have a 300 ksps, 10-bit successive-approximation-register (SAR) ADC with integrated track-and-hold and programmable window detector. ADC0 also has an autonomous low power Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically average the ADC results, providing an effective 11, 12, or 13-bit ADC result without any additional CPU intervention.

The ADC can sample the voltage at any of the MCU GPIO pins (with the exception of P2.7) and has an on-chip attenuator that allows it to measure voltages up to twice the voltage reference. Additional ADC inputs include an on-chip temperature sensor, the VDD_MCU supply voltage, the VBAT supply voltage, and the internal digital supply voltage.

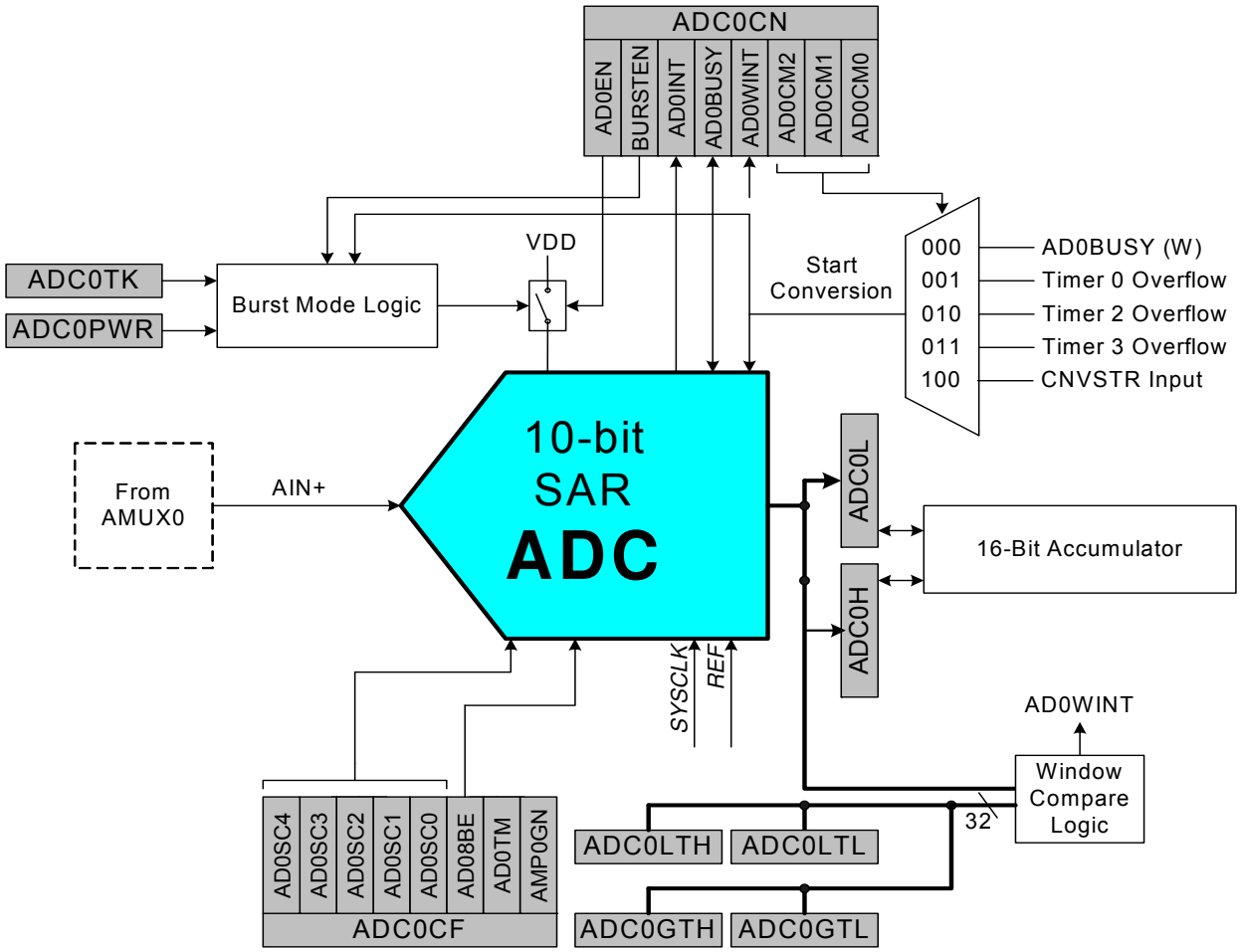

Figure 1.6. ADC0 Functional Block Diagram

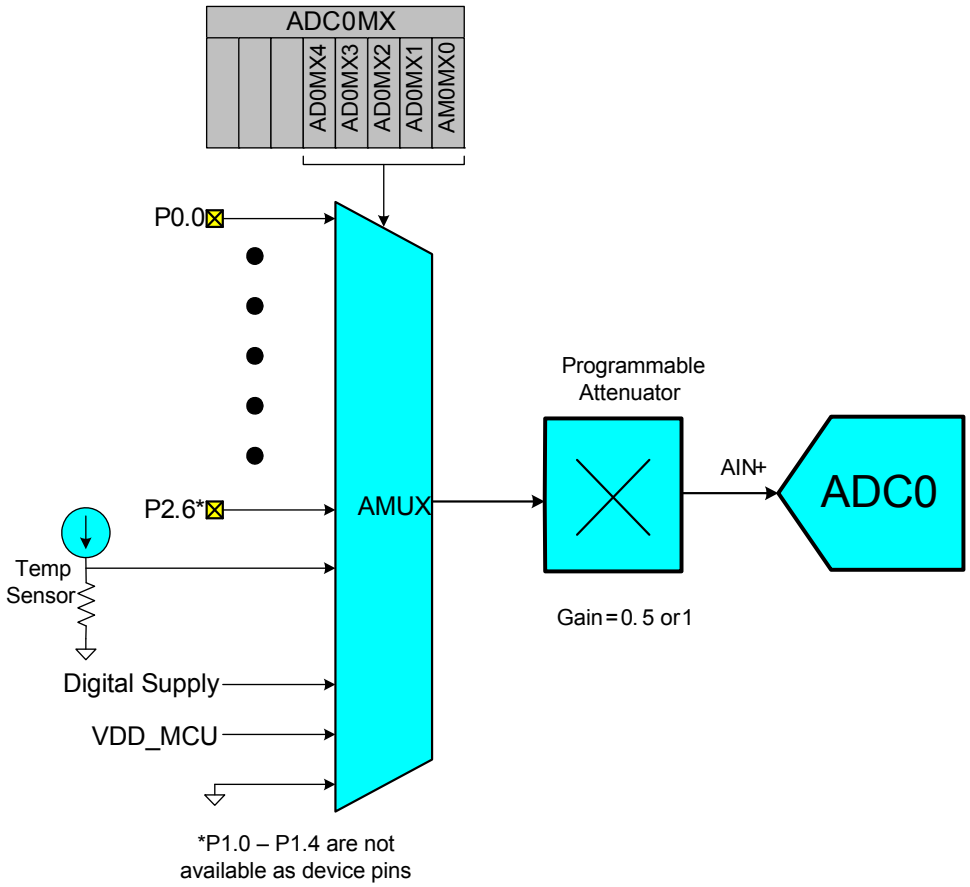

Figure 1.7. ADC0 Multiplexer Block Diagram

1.7. Comparators

Si106x/108x devices include two on-chip programmable voltage comparators: Comparator 0 (CPT0), which is shown in Figure 1.8, and Comparator 1 (CPT1), which is shown in Figure 1.9. The two comparators operate identically but may differ in their ability to be used as reset or wake-up sources. See Section “17. Reset Sources” on page 185 and Section “13. Power Management” on page 160 for details on reset sources and low power mode wake-up sources, respectively.

The comparators offer programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0, CP1), or an asynchronous “raw” output (CP0A, CP1A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the comparator to operate and generate an output when the device is in some low power modes.

The comparator inputs may be connected to Port I/O pins or to other internal signals. Port pins may also be used to directly sense capacitive touch switches. See Application Note “AN338: Capacitive Touch Sense Solution” for details on Capacitive Touch Switch sensing.

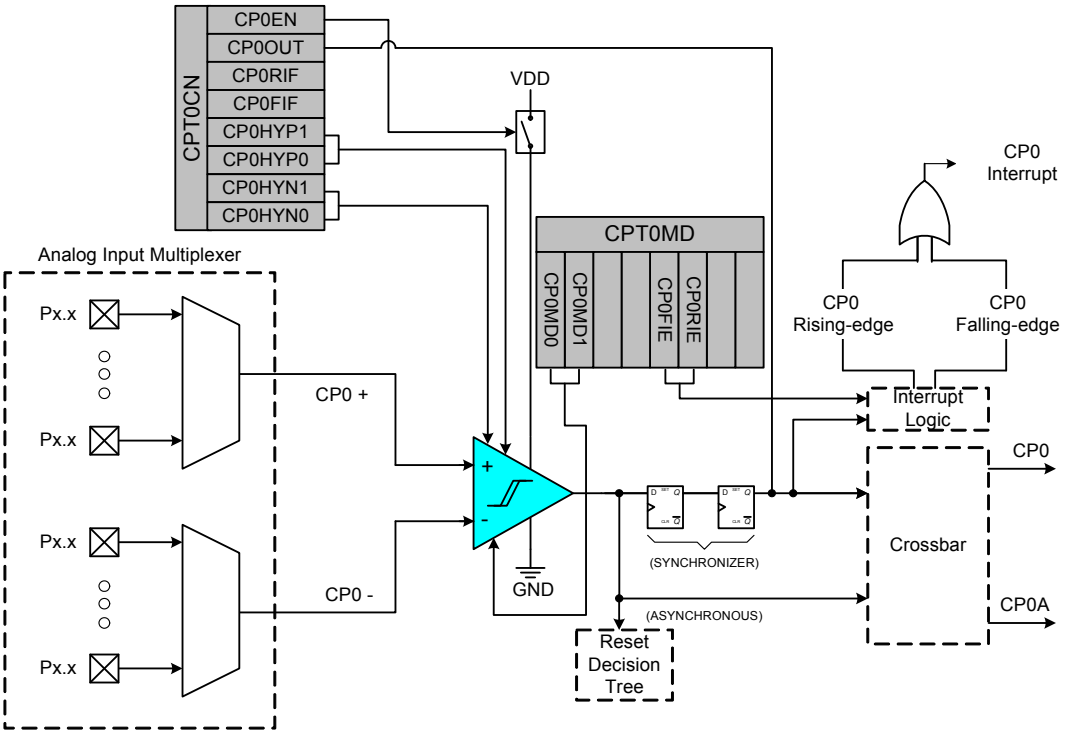

Figure 1.8. Comparator 0 Functional Block Diagram

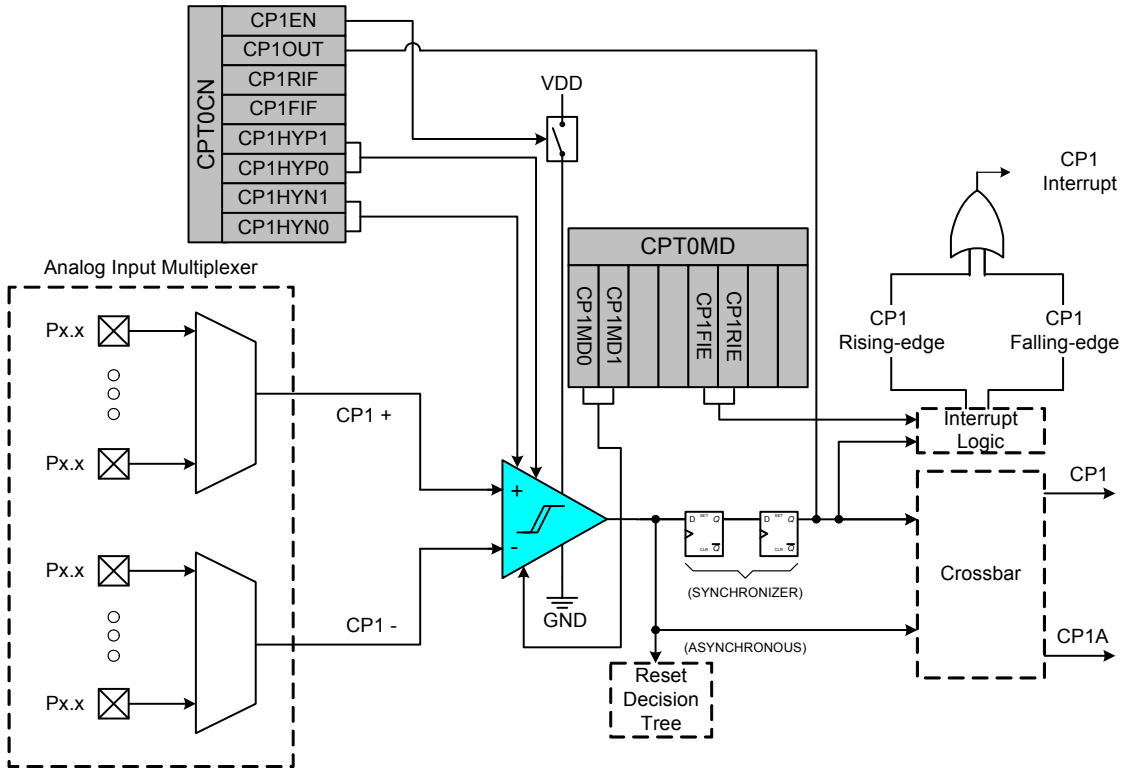

Figure 1.9. Comparator 1 Functional Block Diagram

2. Si106x/108x Ordering Information

Table 2.1. Orderable Part Number

Orderable Part Number	Radio	Flash	RAM	DC-DC Boost	Frequency					Max Output Power	Max Data Rate	Sensitivity		Advanced Features*
					142-175 MHz	283-350 MHz	425-525 MHz	850-960 MHz	960-1050 MHz			Max	40Kbps, GFSK	
Si1060-A-GM	EZRadioPro	64 KB	4 KB	No	✓		✓	✓	✓	+20 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1062-A-GM	EZRadioPro	64 KB	4 KB	Yes	✓	✓	✓	✓	✓	+13 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1064-A-GM	EZRadio	64 KB	4 KB	Yes		✓	✓	✓		+13 dBm	500 kbps	-116 dBm	-108 dBm	No
Si1061-A-GM	EZRadioPro	32 KB	4 KB	No	✓	✓	✓	✓	✓	+20 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1063-A-GM	EZRadioPro	32 KB	4 KB	Yes	✓	✓	✓	✓	✓	+13 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1065-A-GM	EZRadio	32 KB	4 KB	Yes		✓	✓	✓		+13 dBm	500 kbps	-116 dBm	-108 dBm	No
Si1080-A-GM	EZRadioPro	16 KB	768 bytes	No	✓	✓	✓	✓	✓	+20 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1082-A-GM	EZRadioPro	16 KB	768 bytes	Yes	✓	✓	✓	✓	✓	+13 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1084-A-GM	EZRadio	16 KB	768 bytes	Yes		✓	✓	✓		+13 dBm	500 kbps	-116 dBm	-108 dBm	No
Si1081-A-GM	EZRadioPro	8 KB	768 bytes	No	✓	✓	✓	✓	✓	+20 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1083-A-GM	EZRadioPro	8 KB	768 bytes	Yes	✓	✓	✓	✓	✓	+13 dBm	1 Mbps	-126 dBm	-110 dBm	Yes
Si1085-A-GM	EZRadio	8 KB	768 bytes	Yes		✓	✓	✓		+13 dBm	500 kbps	-116 dBm	-108 dBm	No

***Note:** Advanced features include antenna diversity, narrowband support and autonomous low-duty cycle support.

3. Pinout and Package Definitions

Table 3.1. Si1060/Si1061/Si1080/Si1081 Pin Definitions

Pin	Designation	Description
1	P2.7/C2D	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. See Port I/O section for a complete description. Bi-directional data signal for the C2 Debug Interface.
2	XTAL4	SmaRTClock Oscillator Crystal Output. See Section 20 for a complete description.
3	XTAL3	SmaRTClock Oscillator Crystal Input. See Section 20 for a complete description.
4	P1.6	Port 1.6. See Port I/O section for a complete description.
5	P1.5	Port 1.5. See Port I/O section for a complete description.
6	P1.4	Port 1.4. See Port I/O section for a complete description.
7	XOUT	Crystal Oscillator Output. Connect to an external 25 to 32 MHz crystal, or leave floating when driving with an external source on XIN.
8	XIN	Crystal Oscillator Input. Connect to an external 25 to 32 MHz crystal, or connect to an external source.
9	GND_RF	Required ground for the digital and analog portions of the EZRadioPRO peripheral.
10	GPIO2	General Purpose I/O controlled by the EZRadioPRO peripheral. May be configured through the EZRadioPRO registers to perform various functions including: Clock Output, FIFO status, POR, Wake-Up Timer, TRSW, AntDiversity control, etc. See the EZRadioPRO GPIO Configuration Registers for more information.
11	GPIO3	General Purpose I/O controlled by the EZRadioPRO peripheral. May be configured through the EZRadioPRO registers to perform various functions including: Clock Output, FIFO status, POR, Wake-Up Timer, TRSW, AntDiversity control, etc. See the EZRadioPRO GPIO Configuration Registers for more information.
12	RXP	EZRadioPRO peripheral differential RF input pins of the LNA. See application schematic for example matching network.
13	RXN	EZRadioPRO peripheral differential RF input pins of the LNA. See application schematic for example matching network.
14	GND_RF	Required ground for the digital and analog portions of the EZRadioPRO peripheral.
15	GND_RF	Required ground for the digital and analog portions of the EZRadioPRO peripheral.