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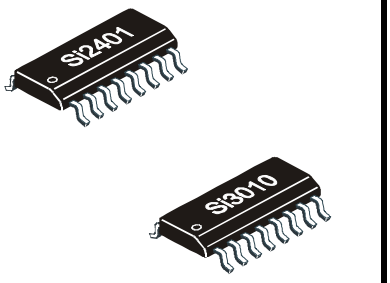
Si2401

V.22bis ISOmodem® with Integrated Global DAA

Features

- Data modem formats
  - 2400 bps: V.22bis
  - 1200 bps: V.22, V.23, Bell 212A
  - 300 bps: V.21, Bell 103
  - Fast connect and V.23 reversing
  - SIA and other security protocols
- 27 MHz CLKIN support
- Caller ID detection and decoding
- UART with flow control
- Integrated third-generation DAA
  - Fewer external components required
  - Over 5000 V capacitive isolation
  - Parallel phone detect
  - Globally-compliant line interface
- AT command set support
- Call progress support
- 3.3 V Power
- Lead-free, RoHS-compliant packages



Ordering Information

See page 72.

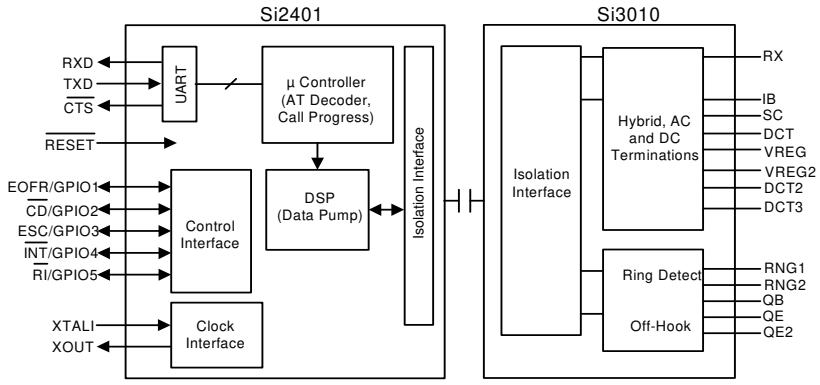
Applications

- Set-top boxes
- ATM terminals
- Medical monitoring
- Point-of-sale
- Security systems
- Power meters

Description

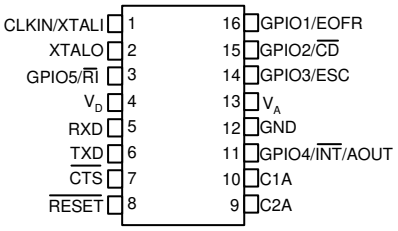
The Si2401 ISOmodem® is a complete, two-chip 2400 bps modem integrating Silicon Labs' third-generation direct access arrangement (DAA), which provides a globally-programmable telephone line interface with an unprecedented level of integration. Available in two 16-pin SOIC packages, this compact solution eliminates the need for a separate DSP data pump, modem controller, codec, isolation transformer, relay, opto-isolators, and 2–4 wire hybrid. The Si2401 provides conventional data formats at connect rates of up to 2400 bps with full-duplex operation over the Public Switched Telephone Network (PSTN). Additionally, the Si2401 is fully-programmable to meet global standards with a single design. Other features include fast connect times for electronic point-of-sale (EPOS) applications and alarm protocols for security systems. The device is ideal for embedded modem applications due to its small size, low external component count, and low power consumption.

Functional Block Diagram

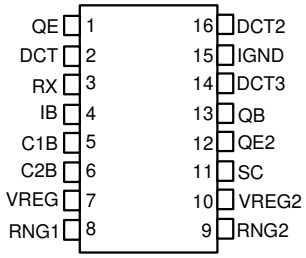


Pin Assignments

Si2401



Si3010



U.S. Patent #5,870,046
U.S. Patent #6,061,009
Other patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F-Grade	0	25	70	°C
Si2401 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:

1. The Si2401 specifications are guaranteed when the typical application circuit (including component tolerance) and Si2401 and Si3010 are used. See "2. Typical Application Schematic" on page 10.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, operates from 3.0 to 3.6 V. The Si2401 interface supports 5 V logic (CLKIN/XTALI supports 3.3 V logic only).

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F-Grade, see Figure 1 on page 6)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	40	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT = 0	12	15	18	V_{RMS}
Ring Detect Voltage*	V_{RD}	RT = 1	18	21	25	V_{RMS}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

Table 3. DC Characteristics*

(V_D = 3.0 to 3.6 V, T_A = 0 to 70°C for F-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 1 mA	—	—	0.35	V
Low Level Output Voltage, GPIO1–4	V_{OL}	I_O = 10 mA	—	—	0.6	V
Input Leakage Current	I_L		–10	—	10	µA
Pullup Resistance Pins 5, 7, 11, 14	R_{PU}		50	100	200	kΩ
Power Supply Current, Digital	I_D	V_D pin	—	10	15	mA
Power Supply Current, DSP Powerdown	I_D	V_D pin	—	8	12	mA
Power Supply Current, Wake-On-Ring	I_D	V_D pin	—	7	10	mA
Power Supply Current, Total Powerdown	I_D	V_D pin	—	100	—	µA

***Note:** Measurements are taken with inputs at rails and no loads on outputs.

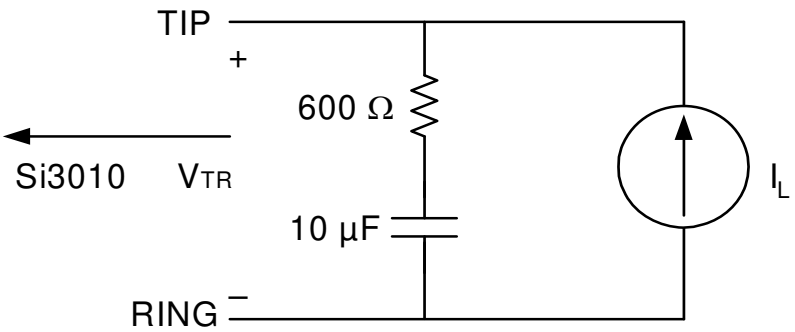


Figure 1. Test Circuit for Loop Characteristics

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, TA = 0 to 70 °C for F-Grade, Fs = 8 kHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		—	8	—	kHz
Clock Input Frequency	F_{XTL}	default	—	4.9152	—	MHz
Clock Input Frequency	F_{XTL}	≤10 kΩ resistor between DCD and GND	—	27	—	MHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	—	200	—	Hz
Transmit Full Scale Level[1]	V_{FS}		—	1.1	—	V_{PEAK}
Receive Full Scale Level[1,2]	V_{FS}		—	1.1	—	V_{PEAK}
Dynamic Range[3]	DR	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I_L = 100 mA	—	80	—	dB
Dynamic Range[3]	DR	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	80	—	dB
Dynamic Range[3]	DR	ILIM = 1, DCV = 11, MINI = 00 DCR = 0, I_L = 50 mA	—	80	—	dB
Transmit Total Harmonic Distortion[4]	THD	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I_L = 100 mA	—	–72	—	dB
Transmit Total Harmonic Distortion[4]	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[4]	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[4]	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I_L = 50 mA	—	–78	—	dB
Dynamic Range (Caller ID Mode)	DR_{CID}	VIN = 1 kHz, –13 dBm	—	50	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 6.
2. Receive full scale level produces –0.9 dBFS at DTX.
3. DR = 20 x log |Vin| + 20 x log (rms signal/rms noise). Applies to both transmit and receive paths. Vin = 1 kHz, –3 dBFS.
4. Vin = 1 kHz, –3 dBFS. THD = 20 x log (rms distortion/rms signal).

Table 5. Absolute Maximum Ratings

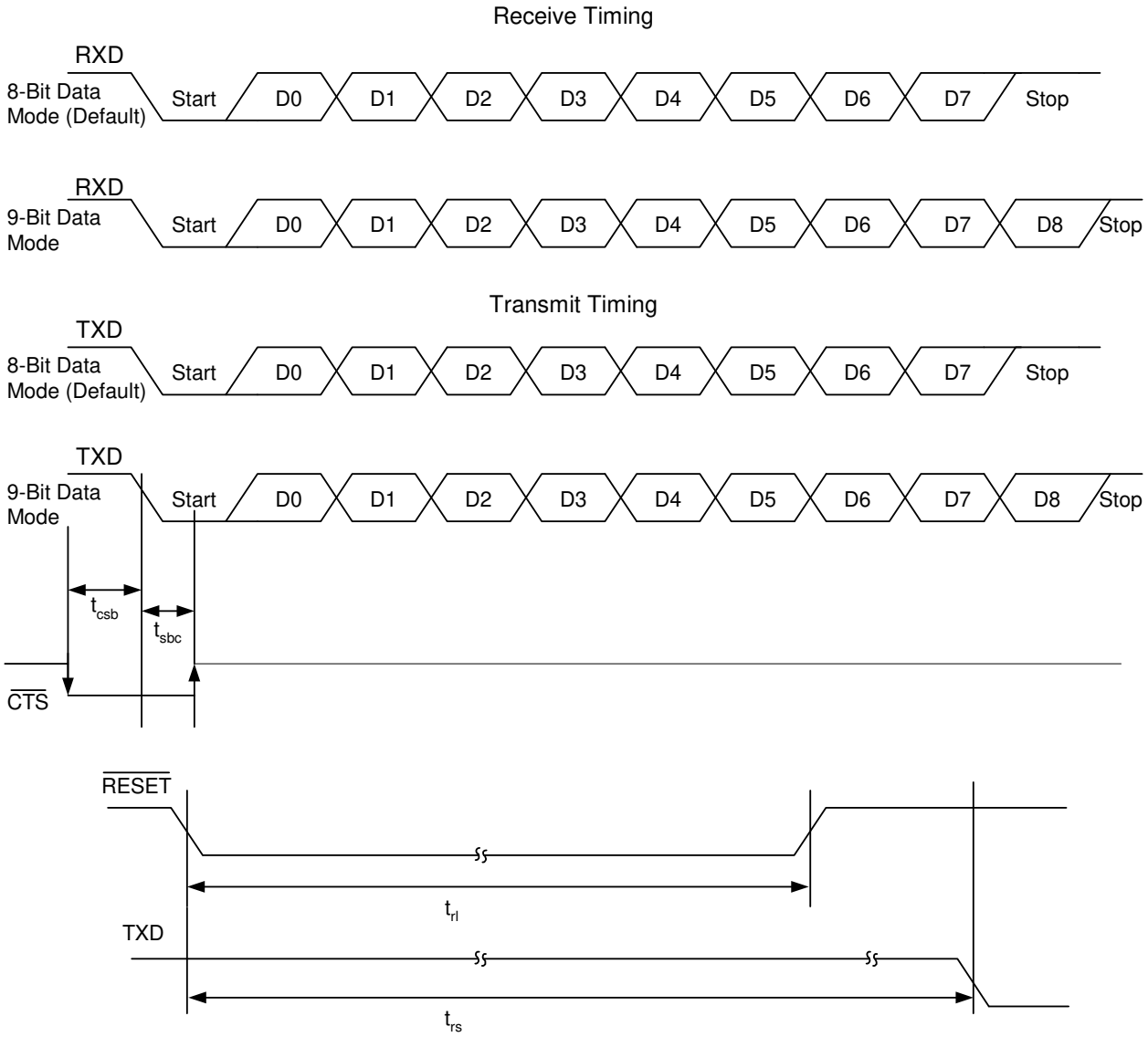
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 4.1	V
Input Current, Si2401 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to 5.3	V
CLKIN/XTALI Input Voltage	V_{XIND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–10 to 100	°C
Storage Temperature Range	T_{STG}	–40 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Switching Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F-Grade)

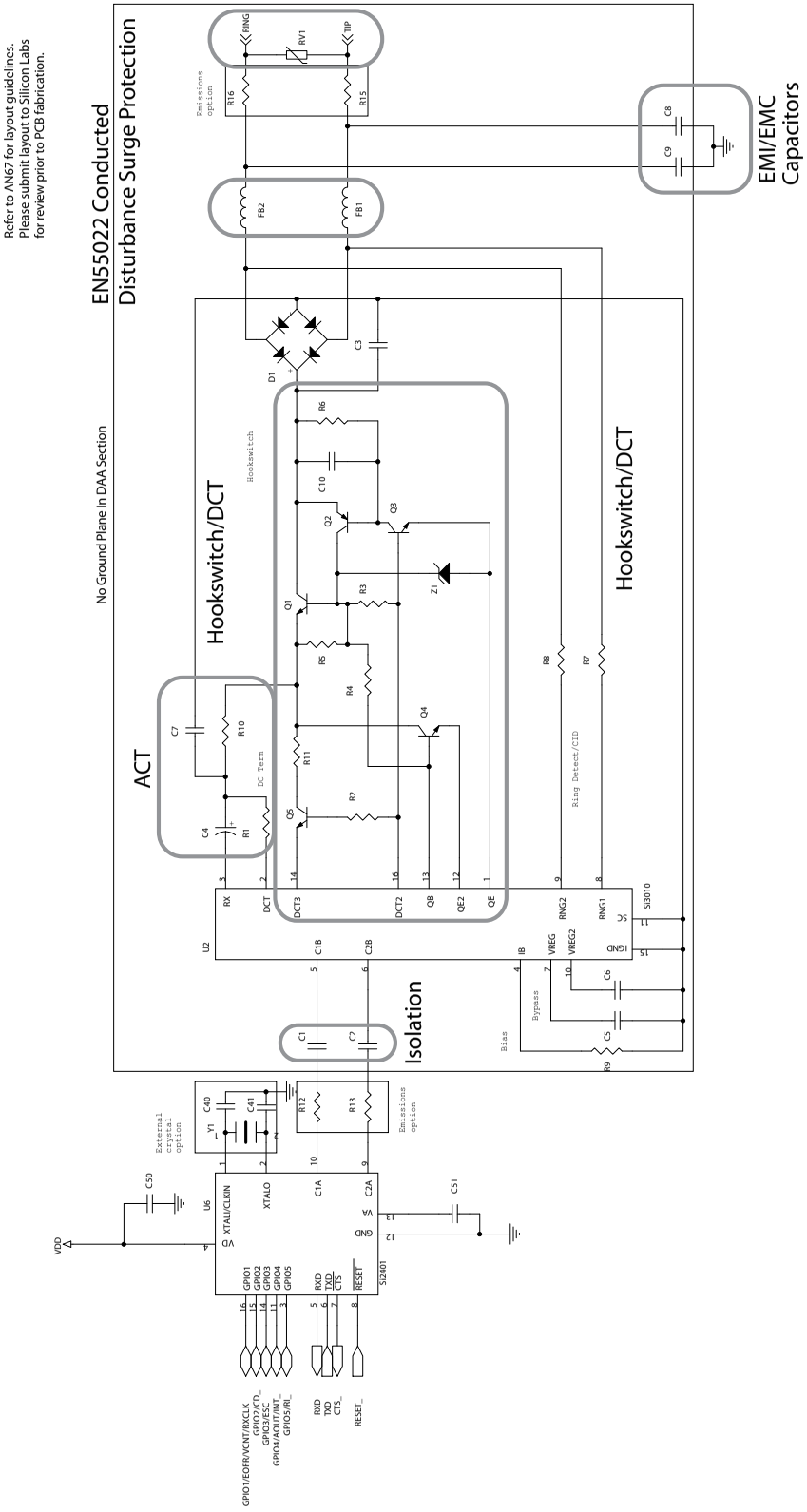
Parameter	Symbol	Min	Typ	Max	Unit
Baud Rate Accuracy		–1	—	1	%
$\overline{CTS}$ ↓ Active to Start Bit↓	t_{csb}	10	—	—	ns
$\overline{RESET}$ Pulse Width	t_{rl}	1	—	—	ms
$\overline{RESET}$ ↑ to TXD ↓	t_{rs}	3	—	—	ms
Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = 2.0 V, V_{IL} = 0.8 V					



Note: Baud rates (programmed through register SE0) are as follows: 300,1200, 2400, 9600, 19200, 38400, 115200, and 307200 Hz.

Figure 2. Asynchronous UART Serial Interface Timing Diagram

2. Typical Application Schematic



3. Bill of Materials: Si2401/10 Chipset

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Tant/Elect, ±20%	Venkel, SMEC
C5, C6, C50	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC
C40, C41[1]	33 pF, 16 V, NP0, ±5%	Venkel, SMEC
C51	0.22 µF, 16 V, X7R, ±20%	Venkel, SMEC
D1[2]	HD04-T (V_{RRM} = 400 V and I_F = 0.8 A)	Diodes, Inc.
FB1, FB2	Ferrite Bead, BLM21AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13	56 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonic
R15, R16[3]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
U1	Si2401	Silicon Labs
U2	Si3010	Silicon Labs
Y1[1,4]	4.9152 MHz, 20 pF, 100 ppm, 150 Ω ESR	ECS Inc., Siward
Z1	Zener Diode, 43 V, 1/2 W, BZT52C43	On Semi

Notes:

1. In STB applications, C40, C41, and Y1 can be removed when using the 27 MHz clock input feature. See "4.10. Clock Generation Subsystem" on page 23.
2. Several diode configurations are acceptable, with the main requirement being $V_{RRM} \geq 350$ and $I_F \geq 225$ mA, e.g., part number HD04-T in a MiniDIP package by Diodes, Inc., two MMBD3004S-7-F diode pairs by Diodes, Inc. in an SOT-23 package, or four 1N4004 diodes.
3. Murata BLM21AG601SN1 may be substituted for R15–R16 (0 Ω) to decrease emissions.
4. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. 50 ppm initial accuracy crystals typically satisfy this requirement.

4. Functional Description

The Si2401 is a complete modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two 16-pin small-outline packages, this solution includes a DSP data pump, modem controller, codec, and DAA.

The modem accepts simple modem AT commands and provides connect rates up to 2400 bps full-duplex over the Public Switched Telephone Network (PSTN) with V.42 hardware support through HDLC framing. To minimize handshake times, the Si2401 can implement a V.22-based fast connect. The modem also supports the V.23 reversing protocol and standard alarm formats including SIA.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2401 solution integrates a silicon DAA using Silicon Laboratories' proprietary third-generation DAA technology. This highly-integrated DAA can be programmed using the Si3010 to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. The DAA can also monitor line status for parallel handset detection and overcurrent conditions.

The Si2401 is designed for rapid assimilation into existing modem applications. The device interfaces directly through a UART to a microcontroller. The Si2401URT-EVB evaluation board connects directly to a standard RS-232 interface. This allows for evaluation of the modem immediately upon powerup via HyperTerminal or any standard terminal software.

The chipset can be fully programmed to meet international telephone line interface requirements with full compliance to FCC, TBR21, JATE, and other country-specific PTT specifications. In addition, the Si2401 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, high-voltage surges, and safety requirements.

Table 7. Selectable Configurations

Configuration	Modulation	Carrier Frequency (Hz)	Data Rate (bps)	Standard Compliance
V.21	FSK	1080/1750	300	Full
V.22*	DPSK	1200/2400	1200	Full
V.22bis*	QAM	1200/2400	2400	No retrain
V.23	FSK	1300/2100	1200/75	Full; plus reversing (Europe)
V.23		1300/1700	600/75	
Bell 103	FSK	1170/2125	300	Full
Bell 212A	DPSK	1200/2400	1200	Full
Security	DTMF	—	40	Full
SIA—Pulse	Pulse	—	Low	Full
SIA Format	FSK	1170/2125	300 half-duplex	300 bps only

***Note:** The Si2401 only adjusts its DCE rate from 2400 bps to 1200 bps if it is connecting to a V.22-only (1200 bps only) modem. Because the V.22bis specification does not outline a fallback procedure, the host should implement a fallback mechanism consisting of hanging up and connecting at a lower baud rate. Retraining to accommodate changes in line conditions that occur during a call must be implemented by terminating the call and redialing.

4.1. Serial Interface

The Si2401 has a universal asynchronous receiver/transmitter (UART) serial interface compatible with standard microcontroller serial interfaces. After powerup or reset, the speed of the serial (Data Terminal Equipment—DTE) interface is set by default to 2400 bps with the 8-bit, no parity, and one-stop bit (8N1) format described below.

The serial interface DTE rate can be modified by writing SE0[2:0] (SD) with the value corresponding to the desired DTE rate. (See Table 8.) This is accomplished with the command, ATSE0=xx, where xx is the hexadecimal value of the SE0 register.

Table 8. DTE Rates

DTE Rate (bps)	SE0[2:0] (SD)
300	000
1200	001
2400	010
9600	011
19200	100
38400	101
115200	110
307200	111

Immediately after the ATSE0=xx string is sent, the host UART must be reprogrammed to the new DTE rate in order to communicate with the Si2401.

The carriage return character following the ATSE0=xx string must be sent at the new DTE rate to observe the “O” response code. See Table 12 on page 24 for the response code summary.

4.2. Configurations and Data Rates

The Si2401 can be configured to any of the Bell and CCITT operation modes listed in Table 9. When configured for V.22bis, the modem connects at 1200 bps if the far end modem is configured for V.22. This device also supports SIA and other protocols for the security industry. Table 7 provides the modulation method, carrier frequencies, data rate, baud rate, and notes on standard compliance for each modem configuration of the Si2401. Table 9 shows example register settings (S07) for some of the modem configurations.

Table 9. Modem Configuration Examples (S07[7] (HDEN) = 0, S07[6] (BD) = 0)

Modem Protocol	Register S07 Values
V.22bis	0x06
V.22	0x02
V.21	0x03
Bell 212A	0x00
Bell 103	0x01
V.23 (1200 tx, 75 rx)	0x16
V.23 (75 tx, 1200 rx)	0x26
V.23 (600 tx, 75 rx)	0x10
V.23 (75 tx, 600 rx)	0x20

As shown in Figure 3, 8-bit and 9-bit data modes refer to the DTE format over the UART. Line data formats are configured through registers S07 (MF1) and S15 (MLC). If the number of bits specified by the format differs from the number of bits specified by the DCE data communications equipment or line (DTE) format, the MSBs are either dropped or bit-stuffed, as appropriate. For example, if the DTE format is 9 data bits (9N1), and the line data format is 8 data bits (8N1), the MSB from the DTE is dropped as the 9-bit word is passed from the DTE side to the DCE (line) side. In this case, the dropped ninth bit can then be used as an escape mechanism. However, if the DTE format is 8N1, and the line data format is 9N1, an MSB equal to 0 is added to the 8-bit word as it is passed from the DTE side to the DCE side.

The Si2401 UART does not continuously check for stop bits on the incoming digital data. Therefore, if the TXD pin is not high, the RXD pin may echo meaningless characters to the host UART. This requires the host UART to flush its receiver FIFO upon initialization.

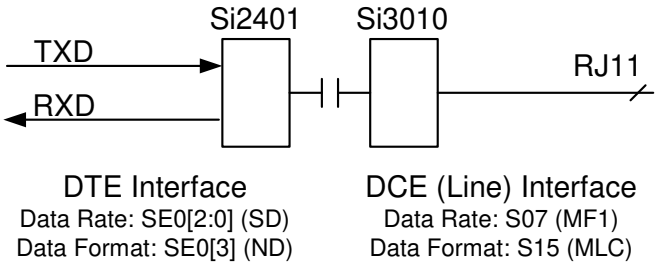


Figure 3. Link and Line Data Formats

4.2.1. Command/Data Mode

Upon reset, the modem is in command mode and accepts AT-style commands. An outgoing modem call can be made using the “ATDT#” (tone dial) or “ATDP#” (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the “c”, “d”, or “v” string and enters data mode. (The byte following the “c”, “d”, or “v” is the first data byte.) At this point, AT-style commands are not accepted. There are three methods that may be used to return the Si2401 to command mode:

- Use the ESC pin—To program the GPIO3 pin to function as an ESCAPE input, set GPIO3 SE2[5:4] = 11. In this setting, a positive edge detected on this pin returns the modem to command mode. The “ATO” string can be used to reenter data mode.
- Use 9-bit data mode—If 9-bit data format with escape is programmed, a 1 detected on bit 9 returns the modem to command mode. (See Figure 2 on page 9.) This is enabled by setting SE0[3] (ND) = 1 and S15[0] (NBE) = 1. The ATO string can be used to reenter data mode. Ninth bit escape does not work in the security modes.
- Use “+++”—The escape sequence is a sequence of three escape characters that are set in S-register S0F (“+” characters by default). If the ISOmodem® chipset detects the “+++” sequence and detects no activity on the UART before or after the “+++” sequence for a time period set by S-register S10, it returns to command mode. To disable this escape sequence, set S-register S10 = FF. To remove the time-dependent behavior, set S-register S10 = 00.

Whether using an escape method or not, when the carrier is lost, the modem automatically returns to command mode and reports “N”.

4.2.2. 8-Bit Data Mode (8N1)

The 8-bit data mode is the default mode after powerup or reset and is set by SE0[3] (ND) = 0_b. It is asynchronous, full duplex, and uses a total of 10 bits including a start bit (logic 0), eight data bits, and a stop bit (logic 1). Data received from the remote modem is transferred from the Si2401 to the host on the RXD pin. Data transfer to the host begins when the Si2401 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2401 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the remote modem is shifted to the Si2401 on TXD beginning with a start bit, LSB, first at the DTE rate determined by the SE0[2:0] setting, and terminates with a stop bit. After the middle of the stop bit time, the Si2401 begins looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

4.2.3. 9-Bit Data Mode (9N1)

The 9-bit data mode is set by SE0[3] (ND) = 1. It is asynchronous, full duplex, and uses a total of 11 bits including a start bit (logic 0), 9 data bits, and a stop bit (logic 1). Data received from the line (remote modem) is transferred from the Si2401 to the host on the RXD pin. Data transfer to the host begins when the Si2401 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2401 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the line (remote modem) is shifted to the Si2401 on TXD beginning with a start bit, LSB, first at the DTE rate determined by the S-Register SE0[2:0] (SD) setting, and terminates with a stop bit. After the middle of the stop bit time, the Si2401 begins looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

The ninth data bit may be used to indicate an escape by setting S15[0] (NBE) = 1. In this mode, the ninth data bit is normally set to 0 when the modem is online. When the ninth data bit is set to 1, the modem goes offline into command mode, and the next frame is interpreted as an AT command. Data mode can be reentered using the ATO command.

4.2.4. Flow Control

No flow control is needed if the DTE rate and DCE rate are the same. If the serial link (DTE) data rate is set higher than the line (DCE) rate of the modem, flow control is required to prevent loss of data to the transmitter.

To control data flow, the clear-to-send (CTS) pin is used. When CTS is asserted, the Si2401 is ready to accept a character. While CTS is negated, no data should be sent to the Si2401 on TXD. To simplify flow control, the Si2401 has an integrated ten character transmit FIFO and allows for two different CTS reporting methods. By default, the CTS pin is negated as soon as a start bit is detected on the TXD pin and remains negated until the modem is ready to accept another character (see Figure 2 on page 9.) By setting SFC7[7] = 1 (CTSM), CTS is negated when the FIFO is 70% full and is reasserted when the FIFO is 30% full.

4.3. Low Power Modes

The Si2401 has three low-power modes:

- DSP Powerdown. The DSP processor can be powered down by setting register SEB[3] (PDDE) = 1.
  In this mode, the serial interface still functions, and the modem detects ringing and intrusion. However, no modem modes or tone detection features function.
- Wake-Up-On-Ring. By issuing the ATz command, the Si2401 goes into a low-power mode where both the microcontroller and DSP are powered down. Only an incoming ring, a low TXD signal, or a total reset will power up the chip again. Return from wake-on-ring triggers the $\overline{INT}$ pin if S09[6] (WOR) = 1 (WOR = 0_b by default).
- Total Powerdown. Setting SF1[5] = 1 and SF1[6] = 1 places the Si2401 into a total powerdown mode. All logic is powered down including the crystal oscillator and clock-out pin. Only a hardware reset can restart the Si2401.

4.4. Global DAA Operation

The Si2401 chipset contains an integrated silicon direct access arrangement (silicon DAA) that provides a programmable line interface to meet international telephone line requirements. Table 10 gives the DAA register settings required to meet various country PTT standards.

Table 10. Country-Specific Register Settings

Si2401 Register	SF5				SF6			
Country	OHS	ILIM	RZ	RT	MINI[1:0]	DCV[1:0]	ACT[3:0]	AT Command String
Algeria	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Argentina	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Armenia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Australia	01	0	0	0	10	01	0011	ATSF5=10SF6=93
Austria (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Bahamas	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Bahrain	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Belarus	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Belgium (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Bermuda	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Brazil	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Brunei	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Bulgaria	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Canada	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Caribbean	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Chile	00	0	0	0	00	10	0000	ATSF5=00SF6=20
China - People's Republic	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Colombia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Costa Rica	00	0	0	0	00	10	0000	ATSF5=00SF6=20

Table 10. Country-Specific Register Settings

Si2401 Register	SF5				SF6			
Country	OHS	ILIM	RZ	RT	MINI[1:0]	DCV[1:0]	ACT[3:0]	AT Command String
Croatia	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Cyprus (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Czech Republic (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Denmark (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Dominican Republic	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Dubai	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Equador	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Egypt	10	1	0	0	00	10	0011	ATSF5=28SF6=23
El Salvador	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Estonia (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Finland (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
France (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Georgia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Germany (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Ghana	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Greece (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Guadeloupe	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Guam	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Hong Kong	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Hungary (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Iceland (CTR-21)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
India	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Indonesia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Ireland (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Israel	10	0	0	0	01	01	0011	ATSF5=20SF6=53
Italy (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Japan	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Jordan	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Kazakhstan	00	0	0	0	00	10	0000	ATSF5=00SF6=20

Table 10. Country-Specific Register Settings

Si2401 Register	SF5				SF6			
Country	OHS	ILIM	RZ	RT	MINI[1:0]	DCV[1:0]	ACT[3:0]	AT Command String
Korea	00	0	1	0	00	10	0000	ATSF5=04SF6=20
Kuwait	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Kyrgyzstan	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Latvia (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Lebanon	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Lesotho	00	0	1	0	00	10	0011	ATSF5=04SF6=23
Liechtenstein (CTR-21)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Lithuania (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Luxembourg (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Macao	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Malaysia	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Malta (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Martinique	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Mexico	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Moldova	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Morocco	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Netherlands (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
New Zealand	00	0	0	0	00	10	0100	ATSF5=00SF6=24
Nigeria	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Norway (CTR-21)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Oman	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Pakistan	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Paraguay	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Peru	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Philippines	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Poland (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Polynesia (French)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Portugal (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Puerto Rico	00	0	0	0	00	10	0000	ATSF5=00SF6=20

Table 10. Country-Specific Register Settings

Si2401 Register	SF5				SF6			
Country	OHS	ILIM	RZ	RT	MINI[1:0]	DCV[1:0]	ACT[3:0]	AT Command String
Qatar	00	0	0	0	10	01	0000	ATSF5=00SF6=90
Reunion	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Romania	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Russia	00	0	0	0	00	01	0000	ATSF5=00SF6=10
Saudi Arabia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Singapore	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Slovakia (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Slovenia (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
South Africa	00	0	1	0	00	10	0011	ATSF5=04SF6=23
Spain (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Sri Lanka	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Sweden (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Switzerland (CTR-21)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Taiwan	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Thailand	00	0	0	0	00	01	0000	ATSF5=00SF6=10
Tunisia	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Turkey	10	1	0	0	00	10	0011	ATSF5=28SF6=23
UAE	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Ukraine	00	0	0	0	00	10	0000	ATSF5=00SF6=20
United Kingdom (EU)	10	1	0	0	00	10	0011	ATSF5=28SF6=23
Uruguay	00	0	0	0	00	10	0000	ATSF5=00SF6=20
USA	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Uzbekistan	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Venezuela	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Yemen	00	0	0	0	00	10	0000	ATSF5=00SF6=20
Zambia	10	1	0	0	00	10	0011	ATSF5=28SF6=23

4.5. Parallel Phone Detection

The ISOmodem® chipset is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem chipset is using the phone line.

4.5.1. On-Hook Intrusion Detection

When the ISOmodem chipset is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect when another device is using the shared telephone line, the host can use the ISOmodem chipset to monitor the TIP-RING dc voltage with the LVS[7:0] bits (SDB). The LVS[7:0] bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed 2s complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING.

When all devices on a particular telephone line are on-hook, there is no loop current flowing through TIP and RING. Therefore, the voltage across TIP and RING is at a maximum. (On most telephone lines, this on-hook voltage is a minimum of 40 V.) Once a device goes off-hook, current flows through TIP and RING on that device, and the TIP-RING voltage drops appreciably. (On most telephone lines, this off-hook voltage is a maximum of 20 V.)

If the host checks the TIP-RING voltage via LVS before causing the ISOmodem chipset to dial out or go off-hook, the host can determine if another device is using the telephone line. One way to do this is to verify that the voltage represented in LVS is above some fixed threshold, such as 30 V.

4.5.2. Off-Hook Intrusion Detection

After it has been determined that it is safe to use the phone line without interrupting a call, the host can instruct the ISOmodem chipset to begin a call or go off-hook. However, once the call has begun and the ISOmodem chipset is in data mode, the serial port is used for modem data making it difficult for the host to monitor registers. Therefore, when the ISOmodem chipset is off-hook, an algorithm is implemented to automatically monitor the TIP-RING loop current via the LCS register (SF3). Because the TIP-RING voltage drops significantly when off-hook, TIP-RING current is a better indicator of another device using the phone line. The LCS[7:0] bits have a resolution of 1.1 mA per bit. An LCS register value of 0x00 indicates less than the required loop current is present, and a value of 0xFF indicates excessive current draw (>120 mA if ILIM = 0 or >60 mA if ILIM = 1). The user can read these bits directly through the LCS register. Upon detecting an intrusion, an "i" result code is sent to the host if it is in the call negotiation stage or command mode. Otherwise, the modem can be programmed to generate an interrupt to notify the host of the intrusion.

The off-hook intrusion algorithm monitors the value of LCS (SF3) at a sample rate determined by the DGSR (SDF, bits 6:0) register (40 ms units). The algorithm compares each LCS sample to the reference value in the ACL register (S12). If LCS is lower than ACL by an amount greater than DCL (S11, bits 4:0), the algorithm waits for another LCS sample, and if the next LCS sample is also lower than ACL by an amount greater than DCL, an interrupt occurs. This helps the ISOmodem chipset avoid a false parallel phone detection (PPD) interrupt due to glitches on the phone line. The ACL is continually updated with the value of LCS as outlined below. The algorithm can be outlined as follows:

If LCS(t) = LCS(t – 40 ms x DGSR)
and
LCS(t) – ACL > DCL
then ACL = LCS(t)
If (ACL – LCS[t – 40 ms x DGSR]) > DCL)
and
(ACL – LCS[t]) > DCL)

Then, an intrusion is sent to the host.

The very first sample of LCS the algorithm uses after going off-hook does not have any previous samples for comparison. If LCS was measured during a previous call, this value of LCS may be used as an initial reference. ACL may be written by the host with this known value of LCS. If ACL is non-zero, the ISOmodem chipset uses ACL as the first valid LCS sample in the off-hook intrusion algorithm. If ACL is 0 (default after reset), the ISOmodem chipset ignores the register and does not begin operating the algorithm until two LCS samples have been received. Additionally, immediately after a modem call, ACL is updated automatically with the last valid LCS value before a parallel phone detection (PPD) intrusion or going back on-hook.

The off-hook intrusion algorithm does not begin to operate immediately after going off-hook. This is to avoid triggering an interrupt due to transients resulting from the ISOmodem chipset itself going from on-hook to off-hook. The time that elapses between the ISOmodem chipset going off-hook and the intrusion algorithm starting defaults to one second and may be adjusted via the IST register (S82, bits 7:4). If ACL is written to a non-zero value before going off-hook, a parallel phone intrusion that occurs during this IST interval and

sustains through the end of the interval triggers an interrupt.

The off-hook intrusion algorithm may additionally be disabled for a period of time after dialing begins via the IB register (S82, bits 2:1). This avoids triggering an interrupt due to pulse dialing, open-switch intervals, or line transients from central office switching. Intrusion may be disabled from the start of dialing to the end of dialing (IB = 01_b), from the start of dialing to the timeout of the IS (S29, bits 7:0) by setting IB = 10_b(IB = 2), or from the start of dialing to carrier detect by setting IB = 11b. The off-hook intrusion algorithm is only suspended (not disabled) during this IB interval. Therefore, any intrusion that occurs during the IB interval and sustains through the end of the interval triggers a PPD interrupt.

4.6. Interrupt Detection

The $\overline{INT}$ interrupt pin can be programmed to alert the host of loss of carrier, loss of phone line voltage/current, parallel phone detection, and other interrupts listed in the interrupt status mask (S08). After the host receives an interrupt via the $\overline{INT}$ pin, the host should issue the AT:I command. This command causes a read-clear of the WOR, PPD, NLD, RI, OCD, and REV bits of the S09 register and raises (deactivates) the $\overline{INT}$ pin. All the interrupt status bits in register S09 remain high after being set until cleared by the AT:I command.

4.6.1. Loop Current Detection

In addition to monitoring parallel phone intrusion, it is possible to monitor the loss of loop current. This feature can be enabled by setting S08[4] (NLDM) = 1. This feature is disabled by default. If the loop current is too low for normal DAA operation, S09[4] (NLD) is set. During this event, if the NLR result code is enabled by setting S62[1](NLR) = 1, the "l" result code is sent. Once the loop current returns to a normal current state, the "L" result code is sent. The $\overline{INT}$ pin is also asserted if enabled.

4.6.2. Loss-of-Carrier Detection

The Si2401 has two methods of implementing a loss-of-carrier function. If GPIO4 is programmed as $\overline{INT}$, and if S08[7](CDM) = 1, $\overline{INT}$ asserts in data mode when a loss-of-carrier is detected. The carrier detect function may also be implemented on GPIO2 by setting SE2[3:2] (GPIO2) = 01 and SOC[7](CDE) = 1.

4.6.3. Overcurrent Detection

The Si2401 has an integrated overcurrent detection feature. The Si2401 begins monitoring for an overcurrent condition at a programmable time set by S32 (OCDT) after going off-hook (default = 20 ms). If an overcurrent condition is detected, the Si2401 sets S09[1] interrupt status. As long as GPIO4 is programmed as INT and the overcurrent mask bit is enabled by setting S08[1](OCDM) = 1, $\overline{INT}$ asserts during an overcurrent situation. The host may then check S09[1] (OCD) via the AT:I command to confirm that an overcurrent condition occurred.

4.6.4. Caller ID Decoding Operation

The Si2401 supports full caller ID detection and decode for US Bellcore and UK standards. To use the caller ID decoding feature, the following configuration is necessary:

1. Set SE0[3] (ND) = 0_b (set modem to 8N1 configuration).
2. Set S0C[6:5] (CIDM) = 01 (set modem to Bellcore type caller ID) or S13[2] (CIDB) = 1 (set modem to UK type caller ID).

4.6.5. Caller ID Monitor/Bellcore Caller ID

The Si2401 continuously monitors the phone line for the caller ID mark signals. This can be useful in systems that require detection of caller ID data before the ring signal, voice mail indicator signals, and Type II caller ID monitor support. To force the Si2401 into caller ID monitor mode, set SOC[6:5] (CIDM) = 11.

Note: CIDM should be disabled before going off-hook.

4.6.6. UK Caller ID Operation

The Si2401 starts searching for the Idle State Tone Alert Signal. When this signal has been detected, the Si2401 transmits an "a" to the host. After the Idle State Tone Alert Signal is completed, the Si2401 applies the wetting pulse for the required 15 ms by quickly going off-hook and on-hook. From this point on, the algorithm is identical to that of Bellcore in that it searches for the channel seizure signal and the marks before echoing an "m" and then reports the decoded caller ID data.

4.7. V.23 Operation/V.23 Reversing

The Si2401 supports full V.23 operation including the V.23 reversing procedure. V.23 operation is enabled by setting S07 (MF1) = $xx10x110_b$ or $xx01x110_b$. If S07[5] (V23R) = 1_b, the Si2401 transmits data at 75 bps and receives data at 600 or 1200 bps. If S07[4] (V23T) = 1_b, the Si2401 receives data at 75 bps and transmits data at 600 or 1200 bps. S07[2] (BAUD) is the 1200 or 600 bps indicator. BAUD = 1_b enables the 1200/600 V.23 channel to run at 1200 bps, while BAUD = 0_b enables 600 bps operation.

When a V.23 connection is successfully established, the modem responds with a "c" character if the connection is made with the modem transmitting at 1200/600 bps and receiving at 75 bps. The modem responds with a "v" character if a V.23 connection is established with the

modem transmitting at 75 bps and receiving at 1200/600 bps.

The Si2401 supports the V.23 turnaround procedure. This allows a modem that is transmitting at 75 bps to initiate a "turnaround" procedure so that it can begin transmitting data at 1200/600 bps and receiving data at 75 bps. The modem is defined as being in V.23 master mode if it is transmitting at 75 bps, and it is defined as being in slave mode if the modem is transmitting at 1200/600 bps. The following paragraphs give a detailed description of the V.23 turnaround procedure.

4.7.1. Modem in Master Mode

To perform a direct turnaround once a modem connection is established, the master host goes into online-command-mode by sending an escape command (Escape pin activation, TIES, or ninth bit escape) to the master modem.

Note: The host can initiate a turnaround only if the Si2401 is the master.

The host then sends the ATRO command to the Si2401 to initiate a V.23 turnaround and return to the online (data) mode.

The Si2401 then changes its carrier frequency (from 390 Hz to 1300 Hz) and waits to detect a 390 Hz carrier for 440 ms. If the modem detects more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it echoes the "c" response character. If the modem does not detect more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it hangs up and echoes the "N" (no carrier) character as a response.

4.7.2. Modem in Slave Mode

Configure GPIO4 as $\overline{\text{INT}}$ (SE2[7:6] [GPIO4] = 11_b). The Si2401 performs a reverse turnaround when it detects a carrier drop longer than 20 ms. The Si2401 then reverses (changes its carrier from 1300 Hz to 390 Hz) and waits to detect a 1300 Hz carrier for 400 ms. If the Si2401 detects more than 40 ms of a 1300 Hz carrier in a time window of 400 ms, it sets the S09[7] bit, and the next character echoed by the Si2401 is a "v".

If the Si2401 does not detect more than 40 ms of the 1300 Hz carrier in a time window of 400 ms, it reverses again and waits to detect a 390 Hz carrier for 440 ms. Then, if the Si2401 detects more than 40 ms of a 390 Hz carrier in a time window of 220 ms, it sets the S09[7] bit, and the next character echoed by the Si2401 is a "c".

At this point, if the Si2401 does not detect more than 40 ms of the 390 Hz carrier in a time window of 440 ms, it hangs up, sets the S09[7] bit, and the next character echoed by the Si2401 is an "N" (no carrier).

Successful completion of a turnaround procedure in master or slave mode automatically updates S07[4] (V23T) and S07[5] (V23R) to indicate the new status of the V.23 connection.

To avoid using the $\overline{\text{INT}}$ pin, the host may also be notified of the $\overline{\text{INT}}$ condition by using 9-bit data mode. Setting S15[0] (NBE) = 1_b and S0C[3] (9BF) = 0_b configures the ninth bit on the Si2401 TXD path to function exactly as the $\overline{\text{INT}}$ pin has been described.

4.8. V.42 HDLC Mode

The Si2401 supports V.42 through hardware HDLC framing in all modem data modes. Frame packing and unpacking including opening and closing flag generation and detection, CRC computation and checking, zero insertion and deletion, and modem data transmission and reception are all performed by the Si2401. V.42 error correction and V.42bis data compression must be performed by the host.

The digital link interface in this mode uses the same UART interface (8-bit data and 9-bit data formats) as in the asynchronous modes, and the ninth data bit may be used as an escape by setting S15[0] (NBE) = 1_b. When using HDLC in 9-bit data mode, if the ninth bit is not used as an escape, it is ignored.

To use the HDLC feature on the Si2401, the host must enable HDLC operation by setting S13[1] (HDEN) = 1_b. The host may initiate the call or answer the call using either the "ATDT#", the "ATA" command or the auto-answer mode. (The auto-answer mode is implemented by setting register S00 (NR) to a non-zero value.) When the call is connected, a "c", "d", or "v" is echoed to the host controller. The host may now send/receive data across the UART using either the 8-bit data or 9-bit data formats with flow control.

At this point, the Si2401 begins framing data into the HDLC format. On the transmit side, if no data is available from the host, the HDLC flag pattern is sent repeatedly. When data is available, the Si2401 computes the CRC code throughout the frame, and the data is sent with the HDLC zero-bit insertion algorithm.

HDLC flow control operates in a similar manner to normal asynchronous flow control across the UART and is shown in Figure 4. To operate flow control (using the $\overline{\text{CTS}}$ pin to indicate when the Si2401 is ready to accept a character), a DTE rate higher than the line rate should be selected.

The method of transmitting HDLC frames is as follows:

1. After the call is connected, the host should begin sending the frame data to the Si2401 using the $\overline{CTS}$ flow control to ensure data synchronicity.
2. When the frame is complete, the host should simply stop sending data to the Si2401. Since the Si2401 does not yet recognize the end-of-frame, it expects an extra byte and asserts $\overline{CTS}$ as shown in Figure 4A. If $\overline{CTS}$ is used to cause a host interrupt, this final interrupt should be ignored by the host.
3. When the Si2401 is ready to send the next byte, if it has not yet received any data from the host, it recognizes this as an end-of-frame, raises $\overline{CTS}$, calculates the final CRC code, transmits the code, and begins transmitting stop flags.
4. After transmitting the first stop flag, the Si2401 lowers $\overline{CTS}$ indicating that it is ready to receive the next frame from the host. At this point, the process repeats as in Step 1.

The method of receiving HDLC frames is as follows:

1. After the call is connected, the Si2401 searches for flag data. Then, once the first non-flag word is detected, the CRC is continuously computed, and the data is sent across the UART (8-bit data or 9-bit data mode) to the host after removing the HDLC zero-bit insertion. The DTE rate of the host must be at least as high as that of data transmission. HDLC mode only works with 8-bit data words; the ninth bit is used only for escape on TXD and end-of-frame received (EOFR) on RXD.
2. When the Si2401 detects the stop flag, it sends the last data word in the frame as well as the two CRC bytes and determines if the CRC checksum matches. Thus, the last two bytes are not frame data but are the CRC bytes, which can be discarded by the host. If the checksum matches, the Si2401 echoes “G” (good). If the checksum does not match, the Si2401 echoes “e” (error). Additionally, if the Si2401 detects an abort (seven or more contiguous ones), it echoes an “A”.
   When the “G”, “e”, or “A” (referred to as a frame result word) is sent, the Si2401 raises the EOFR (end of frame receive) pin (see Figure 4B). The GPIO1 pin must be configured as EOFR by setting SE4[3] (GPE) = 1_b. In addition to using the EOFR pin to indicate that the byte is a frame result word, if in 9-bit data mode (set S15[0] (NBE) = 1_b), the ninth bit is raised if the byte is a frame result word. To program this mode, set S0C[3] (9BF) = 1_b and SE0[3] (ND) = 1.
3. When the next frame of data is detected, EOFR is lowered, and the process repeats at Step 1_b.

To summarize, when receiving HDLC frames, the host begins receiving data asynchronously from the Si2401. When each byte is received, the host should check the EOFR pin (or the ninth bit). If the EOFR pin (or the ninth bit) is low, the data is valid frame data. If the EOFR pin (or the ninth bit) is high, the data is a frame result word.

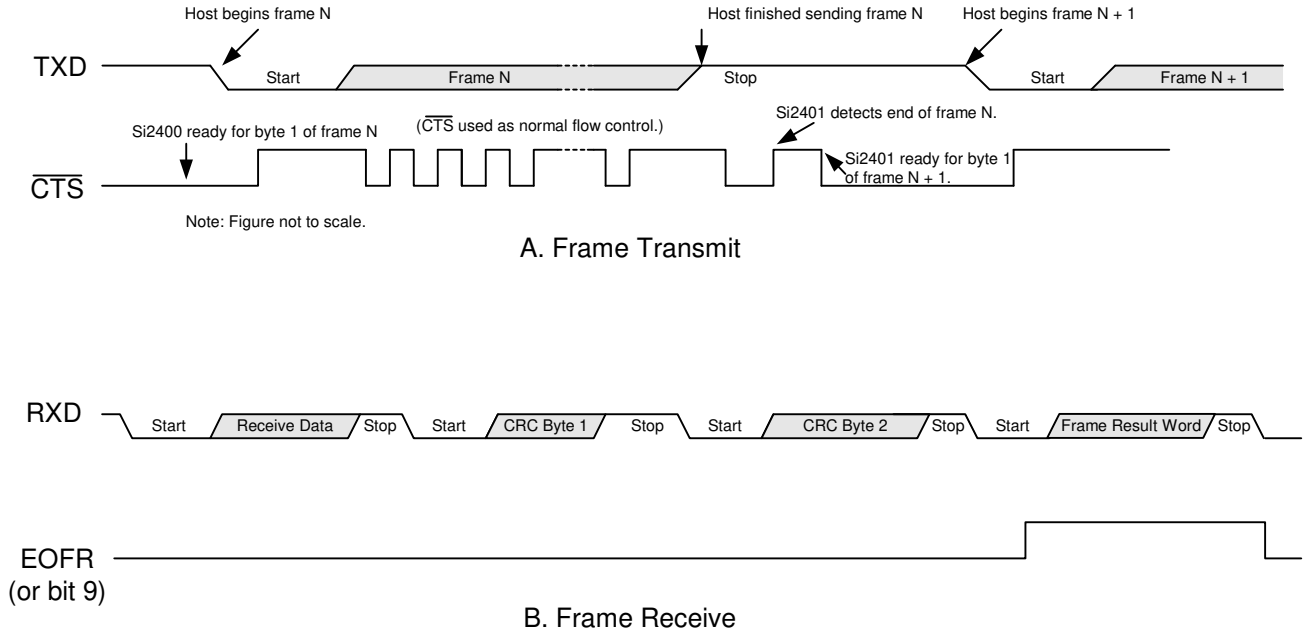


Figure 4. HDLC Timing

4.9. Fast Connect

In modem applications that require fast connection times, it is possible to reduce the length of the handshake.

Additional modem handshaking control can be adjusted through the registers shown in Table 11. These registers are most useful if the user has control of both the originating and answering modems.

When the fast connect settings are used, there may be unintended data received initially. The host must tolerate these bytes.

4.10. Clock Generation Subsystem

The Si2401 contains an on-chip clock generator. Using a single master clock input, the Si2401 can generate all modem sample rates necessary to support V.22bis, V.22/Bell212A, and V.21/Bell103 standards and a 9.6 kHz rate for audio playback. Either a 27 MHz or 4.9152 MHz clock on XTALI or a 4.9152 MHz crystal across XTALI and XTALO form the master clock for the Si2401. This clock source is sent to an internal phase-locked loop (PLL) that generates all necessary internal system clocks. The PLL has a settling time of ~1 ms. Data on RXD should not be sent to the device prior to settling of the PLL. By default, the Si2401 assumes a 4.9152 MHz clock input. If a 27 MHz clock on XTALI is used, a pulldown resistor $\leq$10 kΩ must be placed between GPIO4 (Si2401, pin 11) and GND.

Table 11. V.22/Bell212 Handshaking Control Registers

Register	Name	Function	Units	Default	Fast Connect
S1E	TATL	Transmit Answer Tone Length	1 s	0x03	00
S1F	ATTD	Answer Tone to Transmit Delay	5/3 ms	0x2D	00
S20	UNL	Unscrambled Ones Length—V.22	5/3 ms	0x5D	00
S21	TSOD	Transmit Scrambled Ones Delay—V.22	53.3 ms	0x09	00
S22	TSOL	Transmit Scrambled Ones Length—V.22	5/3 ms	0xA2	00
S23	VDDL	V.22/22b Data Delay Low	5/3 ms	0xCB	00
S24	VDDH	V.22/22b Data Delay High	(256) 5/3 ms	0x08	00
S34	TASL	Answer Tone Length (only used in S1E [TATL] = 0x00)	5/3 ms	0x5A	F0
S35	RSOL	Receive V.22 Scrambled Ones Length	5/3 ms	0xA2	00

5. AT Command Set

The controller provides several vital functions including AT command parsing, DAA control, connect sequence control, DCE protocol control, intrusion detection, parallel phone off-hook detection, escape control, caller ID control and formatting, ring detect, DTMF control, call progress monitoring, and HDLC framing. The controller also writes to the control registers that configure the modem. Virtually all interaction between the host and the modem is done via the controller. The controller uses AT (ATtention) commands and S-Registers to configure and control the modem.

The modem has two modes of operation: command mode and data mode. The Si2401 is asynchronous in both command mode and data mode. The modem is in command mode at powerup, after a reset, before a connection is made, after a connection is dropped, and during a connection after successfully "Escaping" from the data mode back to the command mode using one of the methods previously described. The following section describes the AT command set available in command mode.

The Si2401 supports a subset of the typical modem AT command set since it is intended for use with a dedicated microcontroller instead of general terminal applications. AT commands begin with the letters AT and are followed directly (no space) by the command. (These commands are also case-sensitive.) All AT commands *must* be entered in upper case including AT, except w##, r#, m#, q#, and z (wakeup-on-ring).

AT commands can be divided into two groups: control commands and configuration commands. Control commands, such as ATD, cause the modem to perform an action (going off-hook and dialing). The value of this type of command is changed at a particular time to perform a particular action. For example, the ATDT1234<CR> command causes the modem to go off-hook and dial the number, 1234, via DTMF. This action exists only during a connection attempt. No enduring change in the modem configuration exists after the connection or connection attempt has ended.

Configuration commands change modem characteristics until they are modified or reversed by a subsequent configuration command or the modem is reset. Modem configuration status can be determined with the use of "ATSR?<CR>" where "R" is the two-character hexadecimal address of an S-register.

A command line is defined as a string of characters starting with AT and ending with an end-of-line character, <CR> (13 decimal). Command lines may contain several commands, one after another. If there are no characters between AT and <CR>, the modem responds with "O" after the carriage return.

5.1. Command Line Execution

The characters in a command line are executed one at a time. Unexpected command characters are ignored, but unexpected data characters may be interpreted incorrectly.

After the modem has executed a command line, the result code corresponding to the last command executed is returned to the terminal or host. In addition to the "ATH" and "ATZ" commands, the commands that warrant a response (e.g., "ATSR?" or "ATI") must be the last in the string and followed by a <CR>. All other commands may be concatenated on a single line. To echo command line characters, set the Si2401 to echo mode using the E1 command.

All numeric arguments, including the address and value of an S-register, are in hexidecimal format, and two digits must always be entered.

5.2. <CR> End-Of-Line Character

This character is typed to end a command line. The value of the <CR> character is 13 in decimal, the ASCII carriage return character. When the <CR> character is entered, the modem executes the commands in the command line.

Note: Commands that do not require a response are executed immediately and do not need a <CR>.

Table 12. AT Command Set Summary

Command	Function
A	Answer line immediately with modem
DT#	Tone dial number
DP#	Pulse dial number
E	Local echo on/off
H0	Go on-hook (hang up modem)
H1	Go off-hook
I	Chip revision
:I	Interrupt read and clear
M	Speaker control options
O	Return online
RO	V.23 reverse
S	Read/write S-Registers
w##	Write S-Register in binary
r#	Read S-Register in binary
m#	Monitor S-Register in binary

Table 12. AT Command Set Summary

q#	Read S-Register in binary
V0	Result code with no carriage return
V1	Result code with added carriage returns
Z	Software reset
z	Wakeup on ring

5.3. AT Command Set Description

A Answer

The "A" command makes the modem go off-hook and respond to an incoming call. This command is to be executed after the Si2401 has indicated a ring has occurred. (The Si2401 indicates an incoming ring by echoing an "R".)

This command is aborted if any other character is transmitted to the Si2401 before the answer process is completed.

Auto answer mode is entered by setting S00 (NR) to a non-zero value. NR indicates the number of rings before answering the line.

Upon answering, the modem communicates by whatever protocol has been determined via the modem control registers in S07 (MF1).

If no transmit carrier signal is received from the calling modem within the time specified in S39 (CDT), the modem hangs up and enters the idle state.

D Dial

DT# Tone Dial Number.

DP# Pulse Dial Number.

The D commands make the modem dial a telephone call according to the digits and dial modifiers in the dial string following the command. A maximum of 64 digits is allowed. A DT command performs tone dialing, and a DP command performs pulse dialing.

The ATH1 command can be used to go off-hook without detecting a dial tone or dialing.

The dial string must contain only the digits "0–9", "*", "#", "A", "B", "C", "D", or the modifiers "**;**", "/", or "**,**". Other characters are interpreted incorrectly. The modifier "**,**" causes a two-second delay (added to the spacing value in S04) in dialing. The modifier "/" causes a 125 ms delay (added to the spacing value in S04) in dialing. The modifier "**;**" returns the device to command mode after dialing and must be the last character.

If any character is received by the Si2401 between the ATDT#<CR> (or ATDP#<CR>) command and when the connection is made ("c" or "d" is echoed), the extra character is interpreted as an abort, and the Si2401 returns to command mode ready to accept AT commands. A line feed character immediately following the <CR> is treated as an "extra character" and aborts the call.

If the modem does not have to dial (i.e., "ATDT<CR>" or "ATDP<CR>" with no dial string), the Si2401 assumes the call was manually established and attempts to make a connection.

5.3.1. Automatic Tone/Pulse Dialing

The Si2401 can be configured to attempt DTMF dialing and automatically revert to pulse dialing if it determines that the line is not DTMF-capable. This feature is best explained by the following example.

If it is desired that the telephone number, 12345, be dialed, it is normally accomplished through either the ATDT12345 or the ATDP12345 command. In the force pulse dialing mode of operation, the following string should be issued instead: ATDT1,p12345

If the result code returned is "t,", this indicates that the dialing was accomplished using DTMF dialing. If the result code returned is "tt,", it indicates that the dialing was accomplished using pulse dialing.

In the above example, the Si2401 dials the first digit "1" using DTMF dialing. The "," is used to pause in order to ensure that the central office has had time to accept the DTMF digit "1". When the Si2401 processes the "p" command, it attempts to detect a dial tone. If a dial tone is detected, the DTMF digit "1" was not effective; hence, the line does not support DTMF dialing. Conversely, if the dial tone is not detected, the DTMF digit "1" was effective, and the line supports DTMF dialing. The character after the "p" may or may not be dialed depending on whether the DTMF digit "1" was effective. If the "1" was effective (DTMF mode), the character after the "p" is skipped. The next DTMF digit to be dialed is "2". Subsequent digits are all DTMF. If the "1" was not effective, the first character after the "p" (the "1") is pulse-dialed, and subsequent digits are all pulse-dialed.

E Command Mode Echo

Tells the Si2401 whether or not to echo characters sent from the terminal.

EO

Does not echo characters sent from the terminal.

E1

Echoes characters sent from the terminal.

H0 Hangup

Hang up and go into command mode (go offline).

H1 Off-hook

Go off-hook and remain in command mode.