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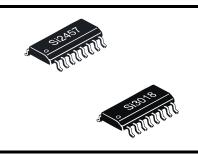


V.90, V.34, V.32BIS, V.22BIS ISOMODEM® WITH GLOBAL DAA

Features

- This data sheet applies to Si2457/34/ Integrated DAA 15/04 Revision D
- Data modem formats
 - ITU-T. Bell
 - 300 bps up to 56 kbps
 - V.21,V.22, V.29 Fast Connect
 - V.44, V.42, V.42bis, MNP2-5
 - Automatic rate negotiation
- Type I and II caller ID decode
- No external ROM or RAM required
- UART, SPI, or parallel interface
- Flexible clock options
 - Low-cost 32.768 kHz oscillator
 - 4.915 MHz oscillator
 - 27 MHz clock input

- - Over 6000 V capacitive isolation
 - Parallel phone detect
 - · Globally-compliant line interface
 - Overcurrent detection
- AT command set support
- SMS / MMS support
- Firmware upgradeable
- **EEPROM** interface
- Lead-free, RoHS-compliant packages
- Commercial or industrial temperature range
- DTMF detection/generation



Ordering Information

This data sheet is valid only for those chipset combinations listed on page 50.

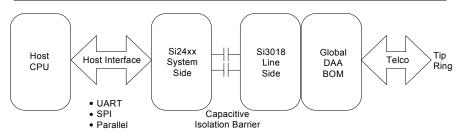
Applications

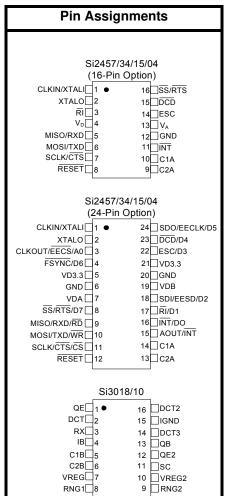
- Set-top boxes
- Point-of-sale terminals
- Text / video telephones
- Digital video recorder
- Digital televisions
- Remote monitoring

Description

The ISOmodem[®] family of products is a complete modem ranging in speed from 56.000 bps to 2400 bps. Offered as a chipset with the Si2457, Si2434. Si2415, or Si2404 system-side device and the Si3018/10 line-side device, the ISOmodem utilizes Silicon Laboratories' patented direct access arrangement (DAA) technology to provide a programmable telephone line interface with an unparalleled level of integration. These compact solutions eliminate the need for a separate DSP, modem controller, codec, transformer, relay, opto-isolators, clocking crystal, and 2-4 wire hybrid. Available with a system-side packaging option of either a 16-pin SOIC or a 24-pin TSSOP, these devices are ideal for embedded modem applications due to their flexibility, small footprint, and minimal external component count.

System Block Diagram







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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter ¹	Symbol	Test Condition	Min ²	Тур	Max ²	Unit
Ambient Temperature	T _A	F-grade G-grade	0 -40	25 25	70 85	°C
Si2457/34/15/04 Supply Voltage, Digital ³	V _D		3.0	3.3	3.6	V

Notes:

- **1.** The Si2457/34/15/04 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2457/34/15/04 and any Si3018 are used. See "2. Typical Application Schematic" on page 11.
- **2.** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
- 3. The digital supply, VD, operates from 3.0 to 3.6 V.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F-grade, T_A = -40 to 85 °C for G-grade)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
DC Termination Voltage	V _{TR}	I _L = 20 mA, ILIM ¹ = 0 DCV = 00, MINI = 11, DCR = 0	_		6.0	V
DC Termination Voltage	V _{TR}	I _L = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9		_	V
DC Termination Voltage	V _{TR}	I _L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	_	_	7.5	V
DC Termination Voltage	V _{TR}	I _L = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	_	_	V
DC Termination Voltage	V _{TR}	I _L = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	_		7.5	V
DC Termination Voltage	V _{TR}	I _L = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40		_	V
DC Termination Voltage	V _{TR}	I _L = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	_	_	40	V
On-Hook Leakage Current	I_{LK}	V _{TR} = -48 V	_		5	μA
Operating Loop Current	I _{LP}	MINI = 00, ILIM = 0	10	_	120	mA
Operating Loop Current	I _{LP}	MINI = 00, ILIM = 1	10	_	60	mA
DC Ring Current		DC current flowing through ring detection circuitry	_	1.5	3	μA
Ring Detect Voltage ²	V_{RD}	RT = 0	12	15	18	V _{RMS}
Ring Detect Voltage ²	V_{RD}	RT = 1	18	21	25	V_{RMS}
Ring Frequency	F_R		15	_	68	Hz
Ringer Equivalence Number	REN		_		0.2	

Notes:

- 1. ILIM = U67, bit 9; DCV = U67, bits 3:2; MINI = U67, bits 13:12; DCR = U67, bit 7; RT = U67, bit 0.
- 2. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.



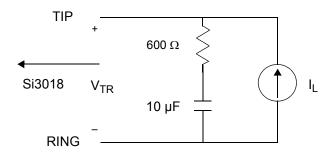


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, $V_D = 3.0$ to 3.6 V

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \text{ °C for F-grade}, T_A = -40 \text{ to } 85 \text{ °C for G-grade})$

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
High Level Input Voltage	V _{IH}		2.0	_	_	V
Low Level Input Voltage	V _{IL}		_	_	0.8	V
High Level Output Voltage	V _{OH}	I _O = -2 mA	2.4	_	_	V
Low Level Output Voltage	V _{OL}	I _O = 2 mA	_	_	0.35	V
Input Leakage Current	ΙL		-10	_	10	μA
Pullup Resistance Pins	R _{PU}		50	125	200	kΩ
Total Supply Current [*]	I _D		_	17	35	mA
Total Supply Current, Wake on Ring [*]	I _D		_	4.4	_	mA
Total Supply Current, Powerdown*	I _D	PDN = 1	_	80	_	μA
*Note: All inputs at 0 or V _D . All inputs held	static except	clock and all outputs un	loaded (Sta	tic I _{OUT} = 0	mA).	1



Si2457/34/15/04

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, TA = 0 to 70 °C for F-grade, Fs = 8 kHz, T_A = -40 to 85 °C for G-grade)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Sample Rate	Fs		_	8	_	kHz
Clock Input Frequency	F _{XTL}	default	_	4.9152	_	MHz
Clock Input Frequency	F _{XTL}	27 MHz Mode ¹	_	27	_	MHz
Clock Input Frequency	F _{XTL}	32 kHz Mode ¹	_	32.768		kHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	_	5	_	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	_	200		Hz
Transmit Full Scale Level ²	V _{FS}		_	1.1	_	V _{PEAK}
Receive Full Scale Level ^{2,3}	V _{FS}		_	1.1	_	V _{PEAK}
Dynamic Range ⁴	DR	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I _L = 100 mA	_	80	_	dB
Dynamic Range ⁴	DR	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I _L = 20 mA	_	80	_	dB
Dynamic Range ⁴	DR	ILIM = 1, DCV = 11, MINI = 00 DCR = 0, I _L = 50 mA	_	80		dB
Transmit Total Harmonic Distortion ⁵	THD	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I _L = 100 mA	_	-72		dB
Transmit Total Harmonic Distortion ⁵	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I _L = 20 mA	_	–78		dB
Receive Total Harmonic Distortion ⁵	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I _L = 20 mA	_	–78		dB
Receive Total Harmonic Distortion ⁵	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I _L = 50 mA	_	–78		dB
Dynamic Range (Caller ID Mode)	DR _{CID}	VIN = 1 kHz, –13 dBm	_	50	_	dB

Notes:

- 1. Refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for configuring clock input reset strapping.
- 2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 5.
- 3. Receive full scale level produces –0.9 dBFS at DTX.
- **4.** DR = $20 \times \log |Vin| + 20 \times \log (rms signal/rms noise)$. Applies to both transmit and receive paths. Vin = 1 kHz, -3 dBFS.
- **5.** Vin = 1 kHz, -3 dBFS. THD = 20 x log (rms distortion/rms signal).

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _D	4.1	V
Input Current, Si2457/34/15/04 Digital Input Pins	I _{IN}	±10	mA
Digital Input Voltage	V_{IND}	-0.3 to (V _D + 0.3)	V
CLKIN/XTALI Input Voltage	V _{XIND}	-0.3 to (V _D + 0.3)	V
Operating Temperature Range	T _A	-10 to 100	°C
Storage Temperature Range	T _{STG}	-40 to 150	°C

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Switching Characteristics¹

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \text{ °C for F-grade}, T_A = -40 \text{ to } 85 \text{ °C for G-grade})$

Parameter	Symbol	Min	Тур	Max	Unit
UART Timing Parameters			-1		
Baud Rate Accuracy	t _{BD}	– 1	_	1	%
Reset Timing Parameters			-1		
RESET ↓ to RESET ↑	t _{RS}	5.0 ²	_	_	ms
RESET ↑ to 1st AT Command	t _{AT}	300	_	_	ms
Parallel Timing Parameters			1		
Address Setup	t _{AS}	15	_		ns
Address Hold	t _{AH}	0	_	_	ns
WR Low Pulse Width	t _{WL}	50	_	_	ns
Write Data Setup Time	t _{WDSU}	20	_	_	ns
Write Cycle Time	t _{WC}	120	_	_	ns
Chip Select Setup	t _{css}	10	_	_	ns
Chip Select Hold	t _{CSH}	0	_	_	ns
RD Low Pulse Width	t _{RL}	50	_	_	ns
RD Low to Data Driven Time	t _{RLDD}	_	_	20	ns
Data Hold	t _{DH}	10	_	_	ns
RD High to Hi-Z Time	t _{DZ}	_	_	30	ns

Notes:

- 1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D 0.4 V, V_{IL} = 0.4 V.
- 2. With 32.768 kHz clocking, allow 500 ms for the reset low-to-high minimum pulse on power-up and wake-from-power-down conditions.



Table 6. Switching Characteristics (Continued) (V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F-grade, T_A = -40 to 85 °C for G-grade)

Parameter	Symbol	Min	Тур	Max	Unit
Read Cycle Time	t _{RC}	120	_	_	ns
Write to Read Cycle Time	t _{WRC}	120	_	_	ns
Serial Peripheral Interface (SPI) Timing Pa	rameters				
SS Falling to First SCLK Edge	t _{SE}	41	_	_	ns
Last SCLK Edge to SS Rising	t _{SD}	41	_	_	ns
SS Rising to MISO High-Z	t _{SDZ}	_	_	93	ns
SCLK High Time	t _{CKH}	102	_	_	ns
SCLK Low Time	t _{CKL}	102	_	_	ns
MOSI Valid to SCLK Sample Edge	t _{SIS}	41	_	_	ns
SCLK Sample Edge to MOSI Change	t _{SIH}	41	_	_	ns
SCLK Shift Edge to MISO Change	t _{SOH}	_	_	93	ns
SCLK cycle time	t _{SCK}	224	_	_	ns
Inactive time between SS actives	t _{NSS_INACT}	81	_		ns

Notes:

- All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D 0.4 V, V_{IL} = 0.4 V.
 With 32.768 kHz clocking, allow 500 ms for the reset low-to-high minimum pulse on power-up and wake-from-powerdown conditions.

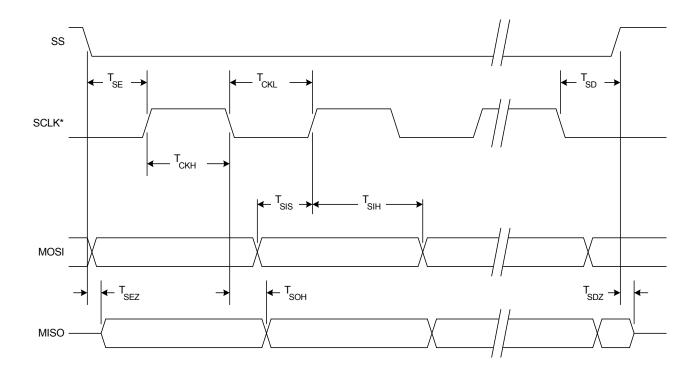


Figure 2. SPI Slave Timing

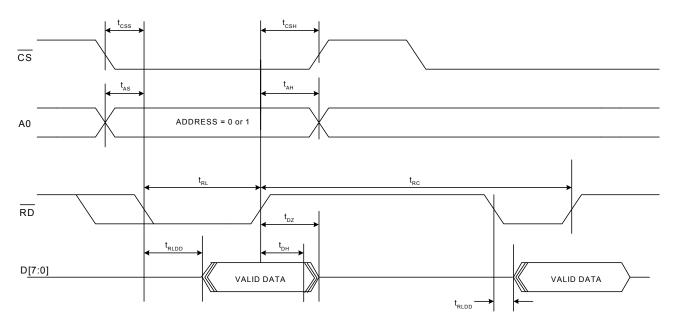


Figure 3. Parallel Interface Read Timing

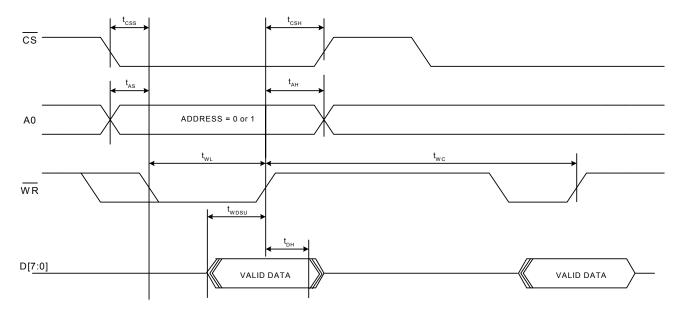


Figure 4. Parallel Interface Write Timing



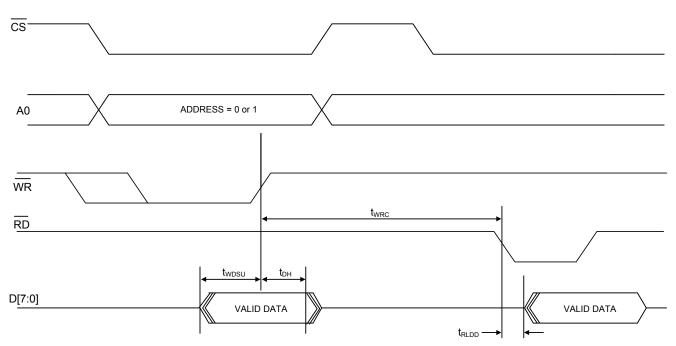


Figure 5. Parallel Interface Write Followed by Read Timing

Typical Application Schematic

Refer to ANS3 Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication. Refer to ANS3 Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication. Refer to ANS3 Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication. REFERENCE SILICON ANS Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication. REFERENCE SILICON ANS Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication. REFERENCE SILICON ANS Appendix A for layout guidelines. Please submit layout to Silicon Labs for review prior to PCB flabrication.

Figure 6. Typical Si2457/34/15/04 Schematic with 16-pin System-Side Option

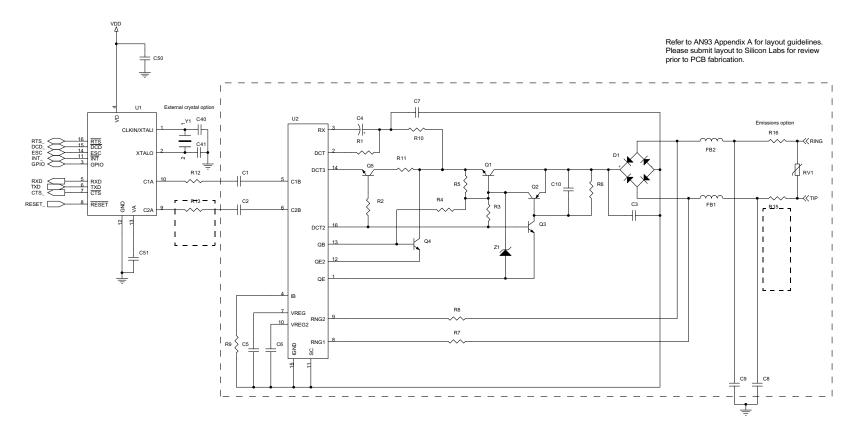


Figure 7. Typical Si2457/34/15/04 Schematic with 24-pin System-Side Option



3. Bill of Materials: Si2457/34/15/04 Chipset

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C52 ¹	0.1 μF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 μF, 16 V, X7R, ±20%	Venkel, SMEC
040	32.768 kHz: 18 pF, 16 V, NPO, ±5%	Venkel, SMEC
C40 C41	4.9152 MHz: 33 pF, 16 V, NPO, ±5%	Veriker, Siviec
041	27 MHz: Not Populated	
C51, C53 ¹	0.22 μF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2 ²	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM21AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13	56 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonio
R15, R16 ³	0 Ω, 1/16 W	Venkel, SMEC, Panasonio
U1	Si2457/34/15/04	Silicon Labs
U2	Si3018/10	Silicon Labs
	32.768 kHz, 12 pF, 100 ppm, 35 kΩ max ESR	FOO Inc. Observed
Y1 ⁴	4.9152 MHz, 20 pF, 100 ppm, 150 Ω ESR	ECS Inc., Siward
	27 MHz (from external clock)	
Z1	Zener Diode, 43 V, 1/2 W, BZT84C43	On Semi

Notes:

- 1. C52 and C53 should not be populated with the Si2457/34/15/04 16-pin package option.
- 2. Several diode bridge configurations are acceptable. For example, a single DF04S or four 1N4004 diodes may be used.
- 3. Murata BLM21AG601SN1 may be substituted for R15–R16 (0 Ω) to decrease emissions.
- **4.** To ensure compliance with ITÚ specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading.



Table 7. Protocol Characteristics

Item	Specification		
Data Rate			
56 kbps ¹	ITU-T V.90 ¹		
54.666 kbps ¹	ITU-T V.90 ¹		
53.333 kbps ¹	ITU-T V.90 ¹		
52 kbps ¹	ITU-T V.90 ¹		
50.666 kbps ¹	ITU-T V.90 ¹		
49.333 kbps ¹	ITU-T V.90 ¹		
48 kbps ¹	ITU-T V.90 ¹		
46.666 kbps ¹	ITU-T V.90 ¹		
45.333 kbps ¹	ITU-T V.90 ¹		
44 kbps ¹	ITU-T V.90 ¹		
42.666 kbps ¹	ITU-T V.90 ¹		
41.333 kbps ¹	ITU-T V.90 ¹		
40 kbps ¹	ITU-T V.90 ¹		
38.666 kbps ¹	ITU-T V.90 ¹		
37.333 kbps ¹	ITU-T V.90 ¹		
36 kbps ¹	ITU-T V.90 ¹		
34.666 kbps ¹	ITU-T V.90 ¹		
33.333 kbps ¹	ITU-T V.90 ¹		
32 kbps ¹	ITU-T V.90 ¹		
30.666 kbps ¹	ITU-T V.90 ¹		
29.333 kbps ¹	ITU-T V.90 ¹		
28 kbps ¹	ITU-T V.90 ¹		
33.6 kbps ²	ITU-T V.34 ²		
31.2 kbps ²	ITU-T V.34 ²		
28.8 kbps ²	ITU-T V.34 ²		
26.4 kbps ²	ITU-T V.34 ²		
24.0 kbps ²	ITU-T V.34 ²		
21.6 kbps ²	ITU-T V.34 ²		
19.2 kbps ²	ITU-T V.34 ²		
16.8 kbps ²	ITU-T V.34 ²		
14.4 kbps ³	ITU-T V.34 or V.32bis ³		
12.0 kbps ³	ITU-T V.34 or V.32bis ³		
9600 bps ³	ITU-T V.34, V.32bis, or V.29 ³		
7200 bps ³	ITU-T V.34 or V.32bis ³		
4800 bps ³	ITU-T V.34 or V.32bis ³		
2400 bps	ITU-T V.34 or V.22bis ³		
1200 bps	ITU-T V.22bis, V.23, or Bell 212A		
300 bps	ITU-T V.22515, V.23, OF BEIL 21274		
300 bps	Bell 103		
Notes:	23.1.100		

Notes:

- 1. Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- 3. Supported on Si2457, Si2434, and Si2415 only.



Table 7. Protocol Characteristics (Continued)

Item	Specification
Data Format	
Bit asynchronous	Selectable 8, 9, 10, or 11 bits per character, which includes the start, stop, and parity bits
Compatibility	ITU-T V.90 ¹ , V.34 ² , V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103
Operating Mode	
Switched network	Two-wire full duplex
Data Modulation	
28 to 56 kbps ¹	V.90 as specified by ITU-T
2.4 to 33.6 kbps ²	V.34 as specified by ITU-T
14.4 kbps ³	128-level TCM/2400 Baud ±0.01%
12.0 kbps ³	64-level TCM/2400 Baud ±0.01%
9600 bps ³	32-level TCM/2400 Baud ±0.01%
9600 bps ³	16-level QAM/2400 Baud ±0.01%
9600 bps ³	V.29 QAM as specified by ITU-T
7200 bps ³	16-level TCM/2400 Baud ±0.01%
4800 bps ³	4-level QAM/2400 Baud ±0.01%
2400 bps	16-level QAM/600 Baud ±0.01%
1200 bps	4-level PSK/600 Baud ±0.01%
300 bps	FSK 300 Baud ±0.01%
Answer Tone	
ITU-T V.32bis, V.32, V.22bis, V.22, and V.21	2100 Hz ±3 Hz
modes	
Bell 212A and 103 modes	2225 Hz ±3 Hz
Transmit Carrier	
V.90 ¹	As specified by ITU-T
V.34 ²	As specified by ITU-T
ITU-T V.32bis ³	1800 Hz ±0.01%
ITU-T V.32 ³	1800 Hz ±0.01%
ITU-T V.29 ³	1700 Hz±1 Hz
ITU-T V.22, V.22bis/Bell 212A	1200 Hz ±0.5 Hz
Originate mode	2400 Hz ±1 Hz
Answer mode	
ITU-T V.21	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)
Originate mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)
Answer mode	, -, -, -, -, -, -, -, -, -, -, -, -, -,
Bell 103	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)
Originate mode	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)
Answer mode	, , , , , , , , , , , , , , , , , , , ,
Output Level	
Permissive—Switched network	–9 dBm maximum
Notes:	

Notes:

- 1. Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- **3.** Supported on Si2457, Si2434, and Si2415 only.



Table 7. Protocol Characteristics (Continued)

Item	Specification
Receive Carrier	
ITU-T V.90 ¹	As specified by ITU-T
ITU-T V.34 ²	As specified by ITU-T
ITU-T V.32bis ³	1800 Hz ±7 Hz
ITU-T V.32 ³	1800 Hz ±7 Hz
ITU-T V.29 ³	1700 Hz ±7 Hz
ITU-T V.22, V.22bis/Bell 212A	2400 Hz ±7 Hz
Originate mode	1200 Hz ±7 Hz
Answer mode	M 1 (200 He 140 He) 0 (4400 He 140 He)
ITU-T V.21	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)
Originate mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)
Answer mode	Mark (2225 Uz ±42 Uz) Space (2025 Uz ±42 Uz)
Bell 103	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz) Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)
Originate mode Answer mode	Walk (12/0 HZ 112 HZ) Space (10/0 HZ 112 HZ)
Carrier Detect (level for ITU-T V.22bis, V.22, V.21,	Acquisition (-43 dBm)
212, 103) in Switched Network	Release (–48 dBm)
Hysteresis	2 dBm minimum
Note: ITU-T V.90 ¹ , V.34 ² , V.32/V.32bis ³ are echo cancel connection. They also provide for self-training dete	ection to force disconnect.
DTE Interface	EIA/TIA-232-E (ITU-T V.24/V.28/ISO 2110)
Line Equalization	Automatic Adaptive
Connection Options	Loss of Carrier in ITU-T V.22bis and lower
Phone Types	500 (rotary dial), 2500 (DTMF dial)
Dialing	Pulse and Tone
DTMF Output Level	Per TIA-968-B
Pulse Dial Ratio	Make/Break: 39/61%
Ring Cadence	Per T1.401.02-2000
Call Progress Monitor	BUSY
	CONNECT (rate)
	NO ANSWER
	NO CARRIER
	NO DIALTONE
	OK
	RING
	RINGING
Notes:	

- **1.** Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- **3.** Supported on Si2457, Si2434, and Si2415 only.



4. Functional Description

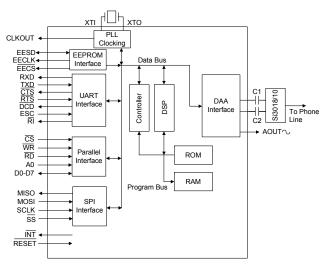


Figure 8. Functional Block Diagram

The Si2457/34/15/04 ISOmodem[®] is a complete embedded modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two small packages, this solution includes a DSP data pump, modem controller, on-chip RAM and ROM, codec, DAA, analog output, and 27 MHz clock input.

The Si2457/34/15/04 accepts standard modem AT commands and provides connect rates up to 56/33.6/14.4/2.4 kbps full-duplex over the Public Switched Telephone Network (PSTN). The Si2457/34/15/04 features a complete set of modem protocols including all ITU-T standard formats up to V.90.

To provide the most flexibility, the Si2457/34/15/04 ISOmodem system-side device is offered in either a 24-pin TSSOP or a 16-pin SOIC package. The 16-pin version is footprint-compatible with the Si2401 ISOmodem and is recommended for most applications. The 16-pin version does not support the parallel, EEPROM or voice codec interface. If these features are required, customers should use the 24-pin version.

The ISOmodem provides numerous additional features for embedded modem applications. The modem includes full type I and type II caller ID detection and decoding for global standards. Call progress monitoring is supported through standard result codes. The modem is also programmable to meet global settings. Because the Si2457/34/15/04 ISOmodem integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2457/34/15/04 solution includes a silicon DAA using Silicon Laboratories' proprietary third-generation DAA technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2457/34/15/04 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, surge immunity, and safety requirements.

The Si2457/34/15/04 allows for rapid integration into existing modem applications by providing a serial interface that can directly communicate to either a microcontroller via a UART interface or a PC via an RS-232 port. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software.

4.1. Host Interface

The Si2457/34/15/04 interfaces to the host processor through either an asynchronous serial interface, a synchronous Serial Peripheral Interface (SPI), or a parallel interface. The default is asynchronous serial communication. Selection of either SPI or parallel interface is done on power-up with reset strapping. Please refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

4.1.1. Asynchronous Serial Interface

The Si2457/34/15/04 supports asynchronous serial communication with data terminal equipment (DTE) at rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART baud rate is automatically detected using the autobaud feature.

4.1.2. Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) provides a flexible, full-duplex synchronous serial bus for host processor and Si2457/34/15/04 ISOmodem communication. When the Si2457/34/15/04 is powered up with SPI mode enabled the modem becomes an SPI slave, and the pins are configured to SS (slave select input, active low), MOSI (serial data input to modem), MISO (serial data output from modem) and SCLK (serial data clock input). Each SPI operation consists of a control-and-address byte and a data byte.

4.1.3. Parallel Interface (24-Pin Version Only)

The Si2457/34/15/04 can also communicate via a parallel interface when using the 24-pin version. The parallel interface is an 8-bit data bus with a single bit address to memory mapped registers.



4.2. Command Mode

Upon reset, the ISOmodem[®] is in command mode and accepts "AT" commands. An outgoing modem call can be made using the "ATDT#" (tone dial) or "ATDP#" (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 12 on page 38 and enters data mode.

4.3. Data Mode

The Si2457/34/15/04 ISOmodem is in data mode while it has a telephone line connection to another modem or is in the process of establishing a connection.

Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4) and data compression to increase throughput (V.44, V.42bis and MNP5).

Each connection between two modems in data mode begins with a handshaking sequence. During this sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

4.4. Fast Connect

The Si2457/34/15/04 supports a fast connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, Bell103, and V.29 modulations. See AN93 for details.

4.5. V.80 Synchronous Access Mode

The Si2457/34/15/04 supports a V.80 synchronous access mode of operation, which operates with an asynchronous DTE and a synchronous DCE. See "AN93: ISOmodem® Chipset Family Designer's Guide".

4.6. Clocking

The Si2457/34/15/04 contains an on-chip phase-locked loop (PLL) and clock generator to derive all necessary internal system clocks from a single clock input. A 32.768 kHz or 4.9152 MHz crystal can be used across XTALI and XTALO pins to form the master clock (±100 ppm max, ±25 ppm recommended) for the ISOmodem. The 32.768 kHz option can provide lower BOM costs and smaller footprint. Alternatively, a clock input of 27 MHz, 4.9152 MHz, or 32.768 kHz can be provided to XTALI if that clock source is available in the system. A 4.9152 MHz clock input is the default clock option. Other clock options are selected at power-up through reset strapping. Refer to AN93 for details.

4.7. Low-Power Modes

The Si2457/34/15/04 provides multiple low power modes. Using the S24 S-register, the Si2457/34/15/04 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the last DTE activity, after the transmit FIFO is empty, and after the last data are received from the remote modem.

Additionally, the Si2457/34/15/04 can be placed in wake-on-ring-mode using the command, AT&Z. In either mode, the ISOmodem remains in the sleep state until one of the following occurs:

- A 1-to-0 transition on TXD (UART mode).
- A 1-to-0 transition on SS (SPI mode).
- A 1-to-0 transition on CS (parallel mode).
- An incoming ring is detected.
- A parallel telephone is picked up.
- Line polarity reversal

The Si2457/34/15/04 may also be placed in a complete powerdown mode. Once the Si2457/34/15/04 completely powers down, it can only be powered back on via the RESET pin.

4.8. Data Compression

The modem can achieve DTE (host-to-ISOmodem) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T V.42bis and MNP5 protocols. Data compression attempts to increase throughput by compressing the data before actually sending it. Thus, the modem is able to transmit more data in a given period of time.

4.9. Error Correction

The Si2457/34/15/04 ISOmodem can employ error correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The Si2457/34/15/04 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

4.10. Wire Mode

Wire mode is used to communicate with standard nonerror correcting modems. When optioned with \N3, the Si2457/34/15/04 falls back to wire mode if it fails in an attempt to negotiate a V.42 link with the remote modem. Error correction and data compression are not active in wire mode.



4.11. Caller ID Operation

The Si2457/34/15/04 supports full type I and type II caller ID detection and decode. Caller ID is supported for the US Bellcore, European ETSI, UK, and Japanese protocols and is enabled via the +VCID, +VCDT, and +PCW commands.

4.12. Parallel Phone Detection

The ISOmodem[®] is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem is using the phone line.

4.12.1. On-Hook Line-in-use Detection

When the ISOmodem is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the ISOmodem to monitor the TIP-RING dc voltage with the line voltage sense (LVS) register (U6C, bits 15:8).

The LVS bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed twos complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING. The ISOmodem can also monitor the TIP-RING dc voltage using the LVCS register (U79, bits 4:0). See Figure 9 on page 19. See also the %Vn commands for automatic line-in-use detection.

4.12.2. Off-Hook Intrusion Detection

When the ISOmodem is off-hook, an algorithm is implemented in the ISOmodem to automatically monitor the TIP-RING loop current via the LVCS register. During the off-hook state, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. See Figure 10 on page 20. Upon detecting an intrusion, the ISOmodem alerts the host of the condition via the INT pin.

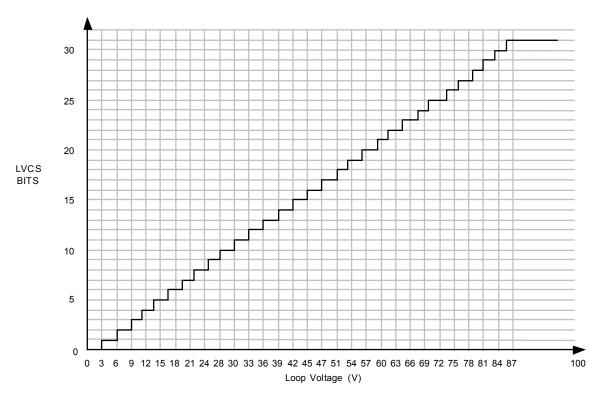


Figure 9. Loop Voltage



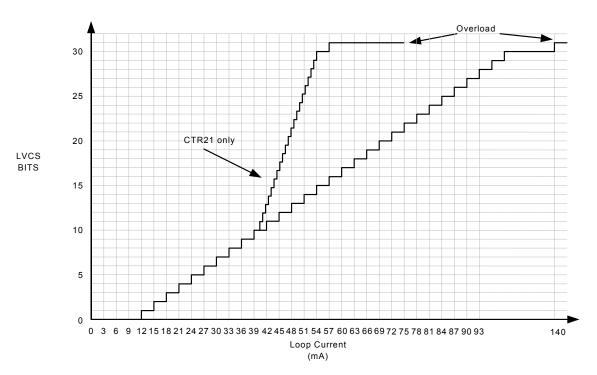


Figure 10. Loop Current



4.13. Overcurrent Detection

The Si2457/34/15/04 includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2457/34/15/04 goes off-hook. This allows the Si2457/34/15/04 to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured. See "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

4.14. Global Operation

The Si2457/34/15/04 chipset contains an integrated silicon direct access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. "AN93: Modem Designer's Guide" gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. See AN93 for complete details.

4.15. Firmware Upgrades

The Si2457/34/15/04 contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2457/34/15/04 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field. See AN93 for complete details.

4.16. DTMF Detection / Generation

The Si2457/34/15/04 provides comprehensive DTMF tone generation and detection. The ISOmodem can generate single tones or DTMF tones using the +VTS command. DTMF tones may also be generated during dialing using the "ATDT" command. DTMF detection is only available in voice mode (+FCLASS = 8). DTMF digits are reported from the modem to the host using <DLE> shielding.

4.17. SMS/MMS Support

Short Message Service (SMS) is a service that allows text messages to be sent and received from one telephone to another via an SMS service center. Multimedia Messaging Service (MMS) extends the core SMS capability to send messages that include multimedia content. The Fax ISOmodem provides an interface that offers a great deal of flexibility in handling multiple SMS standards. This flexibility is possible because most of the differences between standards are handled by the host using the raw data itself. The Si2457/34/15/04 performs the necessary modulation/demodulation of the data and provides two options for message packet structure (Protocol 1 and Protocol 2, as defined in ETSI ES 201 912). The rest of the data link layer and transfer layer are defined by the host system.

The content of the message is entirely up to the host including any checksum or CRC. ETSI ES 201 912 describes two standard data and transfer layers that are commonly used. SMS typically relies on caller identification information to determine if the call should be answered using an SMS device or not.

See "6.4. SMS Support" in AN93 for more information on how to configure the modem for SMS support.

4.18. Codec Interface (24-Pin Version Only)

In order to support a full range of voice and data applications, the Si2457/34/15/04 includes an optional serial interface that connects to an external voice codec (Si3000). See AN93 for complete details.

4.19. EEPROM Interface (24-Pin Version Only)

The Si2457/34/15/04 supports an optional serial peripheral interface (SPI) bus serial EEPROM Mode 3 with a 16-bit (8–64 kbit range) address. Upon powerup, if a pulldown resistor $\leq\!10~k\Omega$ is placed between D6 and GND, the ISOmodem attempts to detect an EEPROM. The EEPROM is intended first for setting custom defaults, second for automatically loading firmware upgrades, and third to allow for user-defined AT command macros for use in custom AT commands or country codes. See AN93 for complete details.

4.20. AT Commands

At powerup, the Si2457/34/15/04 is in the AT command mode. In command mode, the modem monitors the input (serial or parallel) checking constantly for a valid command (AT commands are described in Table 8.)



Table 8. Basic AT Command Set (Command Defaults in Bold)

Command		Action
\$	Display AT command mode settings.	
Α	Answer incoming call	
A/	Re-execute last command. This is the only command not preceded by "AT" or followed by a <cr>.</cr>	
Dn	Dial The dial command, followed by number: Modifier ! or & , or < ; @	Function Flash hook switch for FHT (U4F) ms (default: 500 ms) Pause before continuing for S8 seconds (default: 2 seconds) Return to AT command mode Wait for silence. Polarity reversal detect. By placing the "G" character in the dial string (i.e. ATDTG1), the Si2457/34/15/04 will monitor the telephone line for polarity reversals. If a busy tone is detected, the Si2457/34/15/04 will report "POLARITY REVERSAL" if a polarity reversal was detected or "NO POLARITY REVERSAL" if a polarity reversal was not detected. In each case, the result code is followed by "OK". If the S7 timeout occurs before a busy tone is detected, the Si2457/34/15/04 will report "NO CARRIER". Polarity reversal monitoring begins after the last digit is dialed and ends when the busy tone is detected or S7 timeout occurs. Note: It is not possible to establish a modem connection when using this command.
	L	Redial last number. Pulse (rotary) dialing—pulse digits: 0, 1, 2, 3, 4, 5, 6, 7,
	Р	8, 9
	Т	Tone (DTMF) dialing—DTMF digits: *, #, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
	W	Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1 and X3 do not affect the W command. If the DOP bit (U7A, bit 7) is set, the "ATDTW" command will cause the ISOmodem® to pause dialing and either report an "OK" if a dialtone is detected or "NO DIALTONE" if a dial tone is not detected.
En	Local DTE echo	
E0	Disable	
E1	Enable	
Hn	Hook switch.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
H0	Go on-hook (hang up modem).	
H1	Go off-hook.	
In	Identification and checksum.	
10	Display Si2457/34/15/04 revision code. B: Revision B C: Revision C, etc.	
I1	Display Si2457/34/15/04 firmware revision code (numeric).	
13	Display line-side revision code. 18C = Si3018 revision C	
16	Display the ISOmodem [®] model number. "2404" = Si2404 "2415" = Si2415 "2434" = Si2434 "2457" = Si2457	
17	Diagnostic results 1. See "AN93: ISOModem® Chipset Family Designer's Guide" for details.	
18	Diagnostic results 2. See AN93 for details.	
Ln	Speaker volume operation	
L1	Low speaker volume	
L2	Medium speaker volume	
L3	High speaker volume	
Mn	Speaker operation (via AOUT).	
МО	Speaker is always off.	
M1	Speaker is on while dialing and handshaking; off in data mode.	
M2	Speaker is always on.	
M3	Speaker is off while dialing, on during handshaking and retraining.	
On	Return to data mode from Command mode operation.	
00	Return to data mode.	
01	Return to data mode and perform a full retrain (at any speed except 300 bps).	
O2	Return to data mode and perform rate renegotiation.	
Qn	Response mode.	
Q0	Enable result codes (see Table 12 on page 38)	
Q1	Disable result codes (enable quiet mode).	
R	Initiate V.23 reversal.	
Sn	S-register operation (see Table 13 on page 41).	
S\$	List contents of all S registers.	
Sn?	Display contents of S-register n.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
Sn=x	Set S-register n to value x (where n and x are decimal values).	
Vn	Result code type (see Table 12 on page 38).	
V0	Numeric result codes.	
V1	Verbal result codes	
Xn	Call Progress Monitor (CPM)—This command controls which CPM signals are monitored and reported to the host from the Si2457/34/15/04. (See Table 12 on page 38.)	
X0	Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.	
X1	Extended results; disable CPM—Blind dial. CONNECT message includes speed.	
X2	Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.	
X3	Extended results and detect busy only—Add busy tone detection to X1 mode.	
X4	Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.	
X5	Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.	
Yn	Long space disconnect—Modem hangs up after 1.5 seconds or more of continuous space while on-line.	
Y0	Disable.	
Y1	Enable.	
Z	Hard Reset—This command is functionally equivalent to pulsing the RESET pin low. (See t _{AT} in Table 6 on page 7.)	
:E	Read from serial EEPROM.	
:1	Interrupt Read—This command causes the ISOmodem [®] to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits also are cleared, and the INT pin (INT bit in parallel mode) is deactivated on this read.	
:M	Write to serial EEPROM.	
:P	Program RAM Write—This command is used to upload firmware supplied by Silicon Labs to the Si2457/34/15/04. The format for this command is AT:Paaaa,xxxx,yyyy, where aaaa is the first address in hexadecimal and xxxx,yyyy, is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is <i>only</i> for use with special files provided by Silicon Laboratories. Do not attempt to use this command for any other purpose.	
:R	User-Access Register Read—This command allows the user to read from the user-access registers (see "6. User-Access Registers (U-Registers)" on page 44). The format is "AT:Raa", where: aa = user-access address in hexadecimal. The "AT:R" command causes all the U- registers to be displayed.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action		
:U	User-Access Register Write—This command allows the user to write to the 16-bit user-access registers. (See page page 44.) The format is "AT:Uaa,xxxx,yyyy,zzzz," where aa = user-access address in hexadecimal. xxxx = Data in hexadecimal to be written to location aa. yyyy = Data in hexadecimal to be written to location (aa + 1). zzzz = Data in hexadecimal to be written to location (aa + 2). etc.		
+DR=X	Data compression reporting. X		
+DS Options +DS = A +DS = A,B +DS = A,B,C +DS = A,B,C,D	Controls V.42bis data compression function. A Direction 0 No compression 1 Transmit only 2 Receive only 3 Both Directions B Compression_negotiation 0 Do not disconnect if V.42 is not negotiated. 1 Disconnect is V.42 is not negotiated. C Maximum dictionary size 512 D Maximum string size 6 to 250 (28 default)		
+ES Options +ES = A +ES = A,,C	Enable synchronous access mode. A Specifies the mode of operation when initiating a modem connection. D Disable synchronous assess mode. 6 Enable synchronous access mode when connection is completed and data state is entered. B Specifies fallback mode of operation. This parameter should not be used. C Specifies the mode of operation when answer a modem connection. D Disable synchronous assess mode. 8 Enable synchronous access mode when connection is completed and data state is entered.		

