

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



### Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China







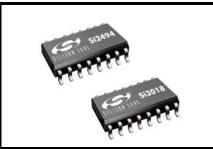


## V.92 AND V.34 ISOMODEM® WITH GLOBAL DAA

#### **Features**

- Data modem formats
  - ITU-T, Bell
  - 300 bps up to 56 kbps
  - V.21, V.22, V.29 Fast Connect
  - V.44, V.42, V.42bis, MNP2-5
  - Automatic rate negotiation
  - V.92 PCM upstream
  - V.92 Quick connect
  - V.92 Modem on hold
- Type I and II caller ID decode
- No external ROM or RAM required
- UART, SPI, or parallel interface
- Flexible clock options
  - Low-cost 32.768 kHz oscillator
  - 4.915 MHz oscillator
  - 27 MHz clock input
- Integrated DAA
  - Over 6000 V capacitive isolation
  - Parallel phone detect
  - Globally-compliant line interface
  - Overcurrent detection
- AT command set support
- SMS / MMS support
- Firmware upgradeable

- **EEPROM** interface
- Commercial or industrial temperature range
- DTMF detection/generation
- Si3000 Voice Codec Interface
  - Hardware support for mic, speaker, and/or handset
  - Programmable voice filters. limiters, and sidetone
  - Supports TBR-38, TIA/EIA-4790 and other voice standards
- Voice pass through with compression
  - Supports telephone answering machine, music on hold, voice menus, etc
- Full-duplex speakerphone support
  - Line echo cancellation
  - Acoustic echo cancellation



#### **Ordering Information**

This data sheet is valid only for those chipset combinations listed on page 59.

#### **Applications**

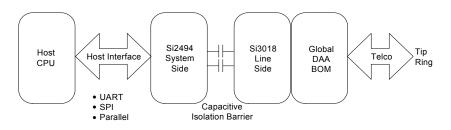
- Point-of-sale terminals
- Security

- Medical
- Remote monitoring

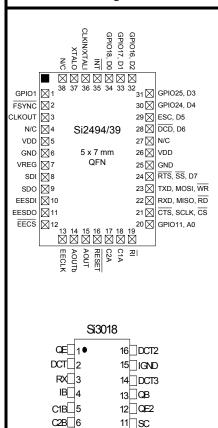
#### Description

The Si2494/39 ISOmodem is a full-featured ITU V.92/V.34-compliant modem that provides connect rates of up to 56 kbps, full-duplex, over the public switched telephone network (PSTN). Offered as a chipset with the Si2494/39 system-side device and the Si3018 line-side device, the ISOModem utilizes Silicon Laboratories' patented direct access arrangment (DAA) technology to provide a programmable telephone line interface with an unparalleled level of integration. This compact solution eliminates the need for a separate DSP, modem controller, codec, transformer, relay, opto-isolators, clocking crystal, and 2-4 wire hybrid. The addition of the Si3000 voice codec supports a voice handset and/or full-duplex speakerphone. Voice pass-through with optional compression supports tapeless answering machine, music-on-hold, voice menus, etc. The Si2494/39 is ideal for embedded modem applications due to its flexibility, small footprint, and minimal external component count.

#### System Block Diagram



## Pin Assignments



VREG□7

RNG1∐8

10 VREG2

9 RNG2



2

## TABLE OF CONTENTS

Section P	<u>age</u>
1. Electrical Specifications	5
2. Typical Application Schematic	
3. Bill of Materials: Si2494/39 Chipset	
4. Functional Description	
4.1. Host Interface	19
4.2. Command Mode	20
4.3. Data Mode	20
4.4. Fast Connect	
4.5. V.80 Synchronous Access Mode	20
4.6. Voice Mode (+FCLASS=8)	
4.7. Clocking	
4.8. Low-Power Modes	
4.9. Data Compression	
4.10. Error Correction	
4.11. Wire Mode	
4.12. V.92 PCM Upstream	
4.13. V.92 Quick Connect	
4.14. V.92 Modem-on-Hold	
4.15. Caller ID Operation	
4.16. Parallel Phone Detection	
4.17. Overcurrent Detection	
4.18. Global Operation	
4.19. Firmware Upgrades	
4.20. DTMF Detection / Generation	
4.21. SMS/MMS Support	
4.22. Codec Interface	
4.23. Answering Machine Support	
4.24. Voice Pass-Through (Speakerphone)	
4.25. General-Purpose Tone Detectors	
4.20. EEPROW Interface	
4.28. Extended AT Commands	
5. S-Registers	
6. User-Access Registers (U-Registers)	
7. Pin Descriptions: Si2494/39	
8. Pin Descriptions: Si3018	
9. Ordering Guide	
10. Package Markings (Top Markings)	
10.1. Si2494 Top Marking	
10.2. Si2439 Top Marking	
10.3. Si2494/39 Top Markings Explanation	
10.4. Si3018 Top Markings	
10.5. Si3018 Top Markings Explanation	62



## Si2494/39

11. Package Outline: 38-Pin QFN	.63
12. 38-Pin QFN Land Pattern	.65
13. Package Outline: 16-Pin SOIC	
14. 16-Pin SOIC Land Pattern	
Contact Information	



### 1. Electrical Specifications

**Table 1. Recommended Operating Conditions** 

Parameter <sup>1</sup>	Symbol	Test Condition	Min <sup>2</sup>	Тур	Max <sup>2</sup>	Unit
Ambient Temperature	T <sub>A</sub>	F-grade G-grade	0 -40	25 25	70 85	°C
Si2494/39 Supply Voltage, Digital <sup>3</sup>	$V_D$		3.0	3.3	3.6	V

#### Notes:

- **1.** The Si2494/39 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2494/39 and any Si3018 are used. See "2. Typical Application Schematic" on page 12.
- **2.** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
- 3. The digital supply, VD, operates from 3.0 to 3.6 V.

Figure 1. Test Circuit for Loop Characteristics

Table 2. DC Characteristics,  $V_D = 3.0$  to 3.6 V

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \,^{\circ}\text{C} \text{ for F-grade}, T_A = -40 \text{ to } 85 \,^{\circ}\text{C} \text{ for G-grade})$ 

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
High Level Input Voltage	V <sub>IH</sub>		2.0	_	_	V
Low Level Input Voltage	V <sub>IL</sub>		_	_	0.8	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>O</sub> = -2 mA	2.4	_	_	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>O</sub> = 2 mA	_	_	0.35	V
Input Leakage Current	ΙL		-10	_	10	μΑ
Pullup Resistance Pins	R <sub>PU</sub>		50	125	200	kΩ
Total Supply Current <sup>*</sup>	I <sub>D</sub>		_	17	35	mA
Total Supply Current, Wake-On-Ring*	I <sub>D</sub>		_	4.4	_	mA
Total Supply Current, Powerdown*	I <sub>D</sub>	PDN = 1	_	80	_	μA
*Note: All inputs at 0 or V <sub>D</sub> . All inputs held	static except	clock and all outputs unl	oaded (Sta	tic I <sub>OUT</sub> = 0	mA).	



#### **Table 3. AC Characteristics**

( $V_D$  = 3.0 to 3.6 V, TA = 0 to 70 °C for F-grade, Fs = 8 kHz,  $T_A$  = -40 to 85 °C for G-grade)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Sample Rate	Fs		_	8	_	kHz
Clock Input Frequency	F <sub>XTL</sub>	default	_	4.9152	_	MHz
Clock Input Frequency	F <sub>XTL</sub>	27 MHz Mode <sup>1</sup>	_	27	_	MHz
Clock Input Frequency	F <sub>XTL</sub>	32 kHz Mode <sup>1</sup>	_	32.768	_	kHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	_	5	_	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	_	200	_	Hz
Transmit Full Scale Level <sup>2</sup>	V <sub>FS</sub>		_	1.1	_	V <sub>PEAK</sub>
Receive Full Scale Level <sup>2,3</sup>	V <sub>FS</sub>		_	1.1	_	V <sub>PEAK</sub>
Dynamic Range <sup>4</sup>	DR	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 100 mA	_	80		dB
Dynamic Range <sup>4</sup>	DR	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	80	_	dB
Dynamic Range <sup>4</sup>	DR	ILIM = 1, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 50 mA	_	80		dB
Transmit Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 100 mA	_	<b>-72</b>		dB
Transmit Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	<b>–78</b>		dB
Receive Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	<b>–78</b>		dB
Receive Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I <sub>L</sub> = 50 mA	_	<b>–78</b>		dB
Dynamic Range (Caller ID Mode)	DR <sub>CID</sub>	VIN = 1 kHz, –13 dBm	_	50		dB

#### **Notes**

- 1. Refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for configuring clock input reset strapping.
- 2. Measured at TIP and RING with 600  $\Omega$  termination at 1 kHz, as shown in Figure 1 on page 5.
- 3. Receive full scale level produces –0.9 dBFS at DTX.
- **4.** DR =  $20 \times \log |Vin| + 20 \times \log (rms signal/rms noise)$ . Applies to both transmit and receive paths. Vin = 1 kHz, -3 dBFS.
- **5.** Vin = 1 kHz, -3 dBFS. THD = 20 x log (rms distortion/rms signal).

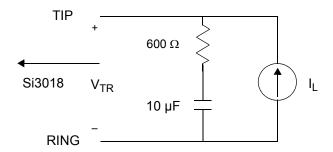
#### **Table 4. Loop Characteristics**

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \text{ °C for F-grade}, T_A = -40 \text{ to } 85 \text{ °C for G-grade})$ 

Symbol	Test Condition	Min	Тур	Max	Unit
$V_{TR}$	I <sub>L</sub> = 20 mA, ILIM <sup>1</sup> = 0 DCV = 00, MINI = 11, DCR = 0	_	_	6.0	V
V <sub>TR</sub>	I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	_	_	V
V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	_	_	7.5	V
V <sub>TR</sub>	I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	_	_	V
V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	_	_	7.5	V
V <sub>TR</sub>	I <sub>L</sub> = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	_	_	V
V <sub>TR</sub>	I <sub>L</sub> = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	_	_	40	V
I <sub>LK</sub>	V <sub>TR</sub> = -48 V	_		5	μA
I <sub>LP</sub>	MINI = 00, ILIM = 0	10	_	120	mA
I <sub>LP</sub>	MINI = 00, ILIM = 1	10	_	60	mA
	DC current flowing through ring detection circuitry	_	1.5	3	μA
$V_{RD}$	RT = 0	12	15	18	$V_{RMS}$
$V_{RD}$	RT = 1	18	21	25	V <sub>RMS</sub>
F <sub>R</sub>		15	_	68	Hz
REN				0.2	
	V <sub>TR</sub> F <sub>R</sub>	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM¹ = 0         —           DCV = 00, MINI = 11, DCR = 0         —           V <sub>TR</sub> I <sub>L</sub> = 120 mA, ILIM = 0         9           DCV = 00, MINI = 11, DCR = 0         —           V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 0         —           DCV = 11, MINI = 00, DCR = 0         9           V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 1         —           DCV = 11, MINI = 00, DCR = 0         —           V <sub>TR</sub> I <sub>L</sub> = 60 mA, ILIM = 1         40           DCV = 11, MINI = 00, DCR = 0         —           V <sub>TR</sub> I <sub>L</sub> = 50 mA, ILIM = 1         —           DCV = 11, MINI = 00, DCR = 0         —           I <sub>L</sub> V <sub>TR</sub> = -48 V         —           I <sub>L</sub> MINI = 00, ILIM = 0         10           I <sub>L</sub> MINI = 00, ILIM = 0         10           I <sub>L</sub> MINI = 00, ILIM = 1         10           DC current flowing through ring detection circuitry         —           V <sub>RD</sub> RT = 0         12           V <sub>RD</sub> RT = 1         18           F <sub>R</sub> 15	V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM¹ = 0 DCV = 00, MINI = 11, DCR = 0       —         V <sub>TR</sub> I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0       9 —         V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0       —         V <sub>TR</sub> I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0       9 —         V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —         V <sub>TR</sub> I <sub>L</sub> = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —         V <sub>TR</sub> I <sub>L</sub> = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —         I <sub>L</sub> V <sub>TR</sub> = -48 V DCV = 11, MINI = 00, ILIM = 1       —         I <sub>L</sub> MINI = 00, ILIM = 0       10 DCV = 10         I <sub>L</sub> MINI = 00, ILIM = 1       —         I <sub>L</sub> MINI = 00, ILIM = 1       —         I <sub>L</sub> MINI = 00, ILIM = 1       —         I <sub>L</sub> MINI = 00, ILIM = 1       —         I <sub>L</sub> MINI = 00, ILIM = 1       10 DCV = 11.5         M <sub>R</sub> M <sub>R</sub> M <sub>R</sub> 1.5         M <sub>R</sub> R <sub>R</sub> 15 DCV = 15.5	V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM¹ = 0 DCV = 00, MINI = 11, DCR = 0       —       —       6.0         V <sub>TR</sub> I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0       9       —       —         V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0       9       —       —         V <sub>TR</sub> I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0       9       —       —         V <sub>TR</sub> I <sub>L</sub> = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —       —       7.5         V <sub>TR</sub> I <sub>L</sub> = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —       —       —         V <sub>TR</sub> I <sub>L</sub> = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —       —       40         I <sub>L</sub> = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0       —       —       5         I <sub>L</sub> = MINI = 00, ILIM = 1 DCV = 11, MINI = 00, ILIM = 1       —       —       5         I <sub>L</sub> = N MINI = 00, ILIM = 0       10       —       120         I <sub>L</sub> = N MINI = 00, ILIM = 1       10       —       60         DC current flowing through ring detection circuitry       —       1.5       3         V <sub>RD</sub> RT = 0       12       15       18         V <sub>RD</sub> RT = 1       18       21       25         F <sub>R</sub> <

#### Notes:

- 1. ILIM = U67, bit 9; DCV = U67, bits 3:2; MINI = U67, bits 13:12; DCR = U67, bit 7; RT = U67, bit 0.
- 2. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.





7

Table 5. Switching Characteristics<sup>1</sup>

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \text{ °C for F-grade}, T_A = -40 \text{ to } 85 \text{ °C for G-grade})$ 

Parameter	Symbol	Min	Тур	Max	Unit			
UART Timing Parameters	UART Timing Parameters							
CLKOUT Output Clock Frequency		2.048	_	49.152	MHz			
Baud Rate Accuracy	t <sub>BD</sub>	<b>–</b> 1	_	1	%			
Reset Timing Parameters				1				
RESET ↓ to RESET ↑	t <sub>RS</sub>	5.0 <sup>2</sup>	_	_	ms			
RESET ↑ to 1st AT Command	t <sub>AT</sub>	300	_	_	ms			
Parallel Timing Parameters					1			
Address Setup	t <sub>AS</sub>	15	_	_	ns			
Address Hold	t <sub>AH</sub>	0	_	_	ns			
WR Low Pulse Width	$t_{WL}$	50	_	_	ns			
Write Data Setup Time	t <sub>WDSU</sub>	20	_	_	ns			
Write Cycle Time	t <sub>WC</sub>	120	_	_	ns			
Chip Select Setup	t <sub>CSS</sub>	10	_	_	ns			
Chip Select Hold	t <sub>CSH</sub>	0	_	_	ns			
RD Low Pulse Width	t <sub>RL</sub>	50	_	_	ns			
RD Low to Data Driven Time	t <sub>RLDD</sub>		_	20	ns			
Data Hold	t <sub>DH</sub>	10	_	_	ns			
RD High to Hi-Z Time	t <sub>DZ</sub>	_	_	30	ns			
Read Cycle Time	t <sub>RC</sub>	120	_	_	ns			
Write to Read Cycle Time	t <sub>WRC</sub>	120	_	_	ns			
Serial Peripheral Interface (SPI) Timing P	arameters							
SS Falling to First SCLK Edge	t <sub>SE</sub>	41	_	_	ns			
Last SCLK Edge to SS Rising	t <sub>SD</sub>	41	_	_	ns			
SS Rising to MISO High-Z	t <sub>SDZ</sub>	_	_	93	ns			
SCLK High Time	t <sub>CKH</sub>	102	_	_	ns			
SCLK Low Time	t <sub>CKL</sub>	102	_	_	ns			
MOSI Valid to SCLK Sample Edge	t <sub>SIS</sub>	41	_	_	ns			
SCLK Sample Edge to MOSI Change	t <sub>SIH</sub>	41	_	_	ns			
SCLK Shift Edge to MISO Change	t <sub>SOH</sub>	<del></del>	_	93	ns			

#### Notes:

8

- All timing is referenced to the 50% level of the waveform. Input test levels are V<sub>IH</sub> = V<sub>D</sub> 0.4 V, V<sub>IL</sub> = 0.4 V.
   With 32.768 kHz clocking, allow 500 to the reset low-to-high minimum pulse on power-up and wake-from-power-down conditions.

# Table 5. Switching Characteristics (Continued) ( $V_D$ = 3.0 to 3.6 V, $T_A$ = 0 to 70 °C for F-grade, $T_A$ = -40 to 85 °C for G-grade)

Parameter	Symbol	Min	Тур	Max	Unit
SCLK cycle time	t <sub>SCK</sub>	224	_	_	ns
Inactive time between SS actives	t <sub>NSS_INACT</sub>	81	_	_	ns

- All timing is referenced to the 50% level of the waveform. Input test levels are V<sub>IH</sub> = V<sub>D</sub> 0.4 V, V<sub>IL</sub> = 0.4 V.
   With 32.768 kHz clocking, allow 500 to the reset low-to-high minimum pulse on power-up and wake-from-power-down conditions.

#### **Table 6. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Thermal Resistance (Si2494/39)	$\theta_{\sf JA}$	QFN-38	_	35	_	°C/W
Thermal Resistance (Si3018)	$\theta_{\sf JA}$	SOIC-16	_	77	_	°C/W
Maximum Junction Temperature (Si2494/39)	Τ <sub>θ</sub>	QFN-38	_	_	105	°C
Maximum Junction Temperature (Si3018)	$T_{\theta}$	SOIC-16	_	_	110	°C

#### **Table 7. Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
DC Supply Voltage	V <sub>D</sub>	4.1	V
Input Current, Si2494/39 Digital Input Pins	I <sub>IN</sub>	±10	mA
Digital Input Voltage	V <sub>IND</sub>	-0.3 to (V <sub>D</sub> + 0.3)	V
CLKIN/XTALI Input Voltage	V <sub>XIND</sub>	-0.3 to (V <sub>D</sub> + 0.3)	V
Operating Temperature Range	T <sub>A</sub>	-10 to 100	°C
Storage Temperature Range	T <sub>STG</sub>	-40 to 150	°C

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



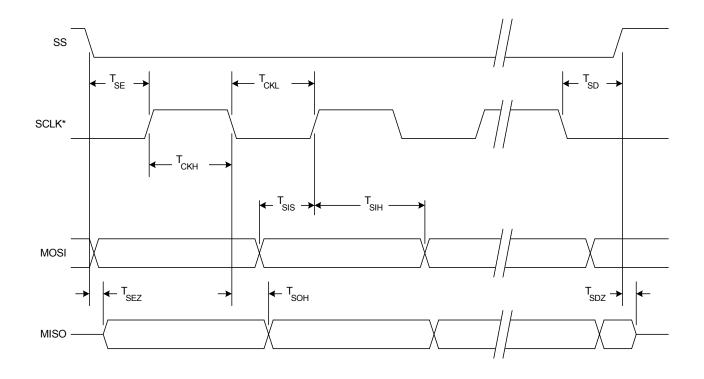
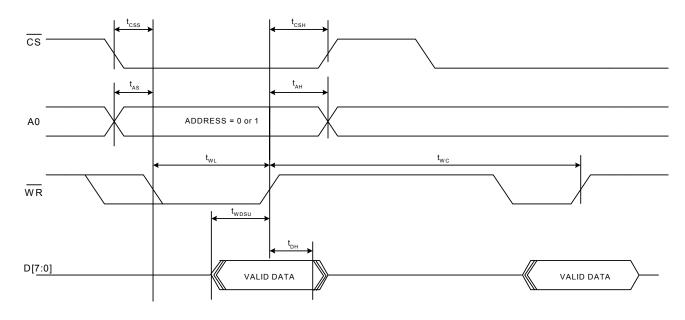


Figure 2. SPI Slave Timing





**Figure 3. Parallel Interface Write Timing** 

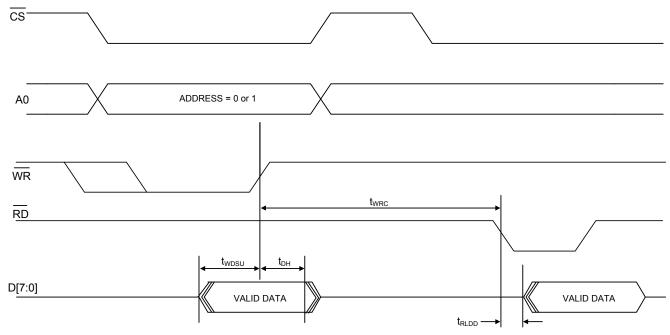


Figure 4. Parallel Interface Write Followed by Read Timing



Rev. 1.0

11



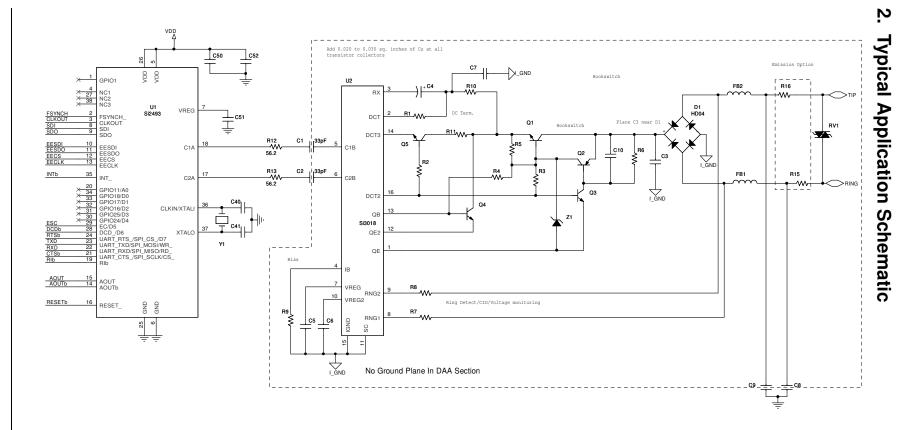


Figure 5. Typical Si2494/39 Schematic

#### 3. Bill of Materials: Si2494/39 Chipset

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C52	0.1 μF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 μF, 16 V, X7R, ±20%	Venkel, SMEC
040	32.768 kHz: 18 pF, 16 V, NPO, ±5%	Venkel, SMEC
C40 C41	4.9152 MHz: 33 pF, 16 V, NPO, ±5%	Veriker, SivieC
041	27 MHz: Not Populated	
C51	0.22 μF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2 <sup>1</sup>	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM21AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonio
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonio
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonio
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonio
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonio
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonio
R12, R13	56 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonio
R15, R16 <sup>2</sup>	0 Ω, 1/16 W	Venkel, SMEC, Panasonio
U1	Si2494/39	Silicon Labs
U2	Si3018	Silicon Labs
	32.768 kHz, 12 pF, 100 ppm, 35 kΩ max ESR	ECC Inc. Chuard
Y1 <sup>3</sup>	4.9152 MHz, 20 pF, 100 ppm, 150 Ω ESR	ECS Inc., Siward
	27 MHz (from external clock)	
Z1	Zener Diode, 43 V, 1/2 W, BZT84C43	On Semi

#### Notes:

- 1. Several diode bridge configurations are acceptable. For example, a single DF04S or four 1N4004 diodes may be used.
- 2. Murata BLM21AG601SN1 may be substituted for R15–R16 (0  $\Omega$ ) to decrease emissions.
- **3.** To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. For optimal V.92 PCM upstream performance, the recommended crystal accuracy is ±25 ppm.



**Table 8. Protocol Characteristics** 

Item	Specification
Data Rate (downstream)	
56 kbps	ITU-T V.90
54.666 kbps	ITU-T V.90
53.333 kbps	ITU-T V.90
52 kbps	ITU-T V.90
50.666 kbps	ITU-T V.90
49.333 kbps	ITU-T V.90
48 kbps	ITU-T V.90
46.666 kbps	ITU-T V.90
45.333 kbps	ITU-T V.90
44 kbps	ITU-T V.90
42.666 kbps	ITU-T V.90
41.333 kbps	ITU-T V.90
40 kbps	ITU-T V.90
38.666 kbps	ITU-T V.90
37.333 kbps	ITU-T V.90
36 kbps	ITU-T V.90
34.666 kbps	ITU-T V.90
33.333 kbps	ITU-T V.90
32 kbps	ITU-T V.90
30.666 kbps	ITU-T V.90
29.333 kbps	ITU-T V.90
28 kbps	ITU-T V.90
Data Rate (upstream)	
48 kbps	ITU-T V.92
46.666 kbps	ITU-T V.92
45.333 kbps	ITU-T V.92
44 kbps	ITU-T V.92
42.666 kbps	ITU-T V.92
41.333 kbps	ITU-T V.92
40 kbps	ITU-T V.92
38.666 kbps	ITU-T V.92
37.333 kbps	ITU-T V.92
36 kbps	ITU-T V.92
34.666 kbps	ITU-T V.92
33.333 kbps	ITU-T V.92
32 kbps	ITU-T V.92
30.666 kbps	ITU-T V.92
29.333 kbps	ITU-T V.92
28 kbps	ITU-T V.92
26.666 kbps	ITU-T V.92
25.333 kbps	ITU-T V.92
24 kbps	ITU-T V.92

**Table 8. Protocol Characteristics (Continued)** 

Item	Specification	
Data Rate		
33.6 kbps	ITU-T V.34	
31.2 kbps	ITU-T V.34	
28.8 kbps	ITU-T V.34	
26.4 kbps	ITU-T V.34	
24.0 kbps	ITU-T V.34	
21.6 kbps	ITU-T V.34	
19.2 kbps	ITU-T V.34	
16.8 kbps	ITU-T V.34	
14.4 kbps	ITU-T V.34 or V.32bis	
12.0 kbps	ITU-T V.34 or V.32bis	
9600 bps	ITU-T V.34 or V.32bis	
7200 bps	ITU-T V.34 or V.32bis	
4800 bps	ITU-T V.34 or V.32bis	
2400 bps	ITU-T V.34, IV.32 bis, or V.22bis	
1200 bps	ITU-T V.22bis, V.23, or Bell 212A	
300 bps	ITU-T V.21	
300 bps	Bell 103	
·		
Data Format	Selectable 8, 9, 10, or 11 bits per character, which includes	
Bit asynchronous	the start, stop, and parity bits.	
Compatibility	ITU-T V.92, V.90, V.34, V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103	
Operating Mode		
Switched network	Two-wire full duplex	
Data Modulation		
28 to 56 kbps (downstream)	V.90 as specified by ITU-T	
24 to 48 kbps (upstream)	V.92 as specified by ITU-T	
2.4 to 33.6 kbps	V.34 as specified by ITU-T	
14.4 kbps	128-level TCM/2400 Baud ±0.01%	
12.0 kbps	64-level TCM/2400 Baud ±0.01%	
9600 kbps	32-level TCM/2400 Baud ±0.01%	
9600 kbps	16-level QAM/2400 Baud ±0.01%	
7200 kbps	16-level TCM/2400 Baud ±0.01%	
4800 kbps	4-level QAM/2400 Baud ±0.01%	
2400 kbps	16-level QAM/600 Baud ±0.01%	
1200 kbps	4-level PSK/600 Baud ±0.01%	
0 to 300 kbps	FSK 0-300 Baud ±0.01%	
Answer Tone		
ITU-T V.32bis, V.32, V.22bis, V.22, and V.21	2100 Hz ±3 Hz	
modes	2100112 10112	
Bell 212A and 103 modes	2225 Hz ±3 Hz	



**Table 8. Protocol Characteristics (Continued)** 

Item	Specification	
Transmit Carrier		
V.92	As specified by ITU-T	
V.90	As specified by ITU-T	
V.34	As specified by ITU-T	
ITU-T V.32bis	1800 Hz ±0.01%	
ITU-T V.32	1800 Hz ±0.01%	
ITU-T V.29	1700 Hz ±1 Hz	
ITU-T V.22, V.22bis/Bell 212A		
Originate mode	1200 Hz ±0.5 Hz	
Answer mode	2400 Hz ±1 Hz	
ITU-T V.21		
Originate mode	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)	
Answer mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)	
Bell 103		
Originate mode	Mark (1070 Hz ±12 Hz) Space (1270 Hz ±12 Hz)	
Answer mode	Mark (2025 Hz ±12 Hz) Space (2225 Hz ±12 Hz)	
Output Level		
Permissive—Switched network	−9 dBm maximum	
Receive Carrier		
ITU-T V.90	As specified by ITU-T	
ITU-T V.34	As specified by ITU-T	
ITU-T V.32bis	1800 Hz ±7 Hz	
ITU-T V.32	1800 Hz ±7 Hz	
ITU-T V.29	1800 Hz ±7 Hz	
ITU-T V.22, V.22bis/Bell 212A		
Originate mode	2400 Hz ±7 Hz	
Answer mode	1200 Hz ±7 Hz	
ITU-T V.21		
Originate mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)	
Answer mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)	
Bell 103		
Originate mode	Mark (2025 Hz ±12 Hz) Space (2225 Hz ±12 Hz)	
Answer mode	Mark (1070 Hz ±12 Hz) Space (1270 Hz ±12 Hz)	
Carrier Detect (level for ITU-T V.22bis, V.22, V.21,	Acquisition (–43 dBm)	
212, 103) in Switched Network	Release (–48 dBm)	
Hysteresis	2 dBm minimum	
·		
ITU-T V.90, V.34, V.32/V.32bis are echo canceling protocols that use signal quality as criteria for maintaining connection. They also provide for self-training detection to force disconnect.		
DTE Interface	EIA/TIA-232-E (ITU-T V.24/V.28/ISO 2110)	
Line Equalization	Automatic Adaptive	
Connection Options	Loss of Carrier in ITU-T V.22bis and lower	



**Table 8. Protocol Characteristics (Continued)** 

Item	Specification	
Phone Types	500 (rotary dial), 2500 (DTMF dial)	
Dialing	Pulse and Tone	
DTMF Output Level	Per Part 68	
Pulse Dial Ratio	Make/Break: 39/61%	
Ring Cadence	On 2 seconds; Off 4 seconds	
Call Progress Monitor	BUSY CONNECT (rate) NO ANSWER NO CARRIER NO DIALTONE OK RING RINGING	



#### 4. Functional Description

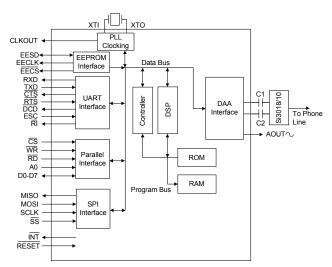


Figure 6. Functional Block Diagram

The Si2494/39 ISOmodem<sup>®</sup> is a complete embedded modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. This solution includes a DSP data pump, modem controller, on-chip RAM and ROM, codec, DAA, analog output, and a PLL clocking generator.

The Si2494/39 accepts standard modem AT commands and provides connect rates up to 56/33.6/14.4/2.4 kbps full-duplex over the Public Switched Telephone Network (PSTN). The Si2494/39 features a complete set of modem protocols including all ITU-T standard formats up to V.92.

The Si2494/39 features a direct interface to the Si3000 voice codec. Itself a highly integrated device, the Si3000 provides a codec, mixer, digital gain control, microphone preamp, microphone bias generator, speaker driver, and line in/out ports for use with external amplifiers. The Si3000 codec combined with the features of the on-chip DSP supports a voice handset and/or full-duplex speakerphone including programmable levels, frequency response, limiting/soft-clipping and sidetone generation. Voice pass-through with optional compression supports implementation of a tapeless answering machine (TAM), music-on-hold, voice menus, etc.

The ISOmodem provides numerous additional features for embedded modem applications. The modem includes full type I and type II caller ID detection and decoding for global standards, DTMF tone generation and detection, Short Message Service (SMS), distinctive ring detection, and call progress monitoring via a PWM audio output. Call progress monitoring is supported through standard result codes. The modem is also programmable to meet global settings. Because the Si2494/39 ISOmodem integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.



This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2494/39 solution includes a silicon DAA using Silicon Laboratories' proprietary third-generation DAA technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2494/39 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, surge immunity, and safety requirements.

The Si2494/39 allows for rapid integration into existing modem applications by providing a serial interface that can directly communicate to either a microcontroller via a UART interface or a PC via an RS-232 port. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software.

#### 4.1. Host Interface

The Si2494/39 interfaces to the host processor through either an asynchronous serial interface, a synchronous Serial Peripheral Interface (SPI), or a parallel interface. The default is asynchronous serial communication. Selection of either SPI or parallel interface is done on power-up with reset strapping. Please refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

#### 4.1.1. Asynchronous Serial Interface

The Si2494/39 supports asynchronous serial communication with data terminal equipment (DTE) at rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART baud rate is automatically detected using the autobaud feature.

#### 4.1.2. Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) provides a flexible synchronous serial bus for host processor and Si2494/39 ISOmodem communication. When the Si2494/39 is powered up with SPI mode enabled the modem becomes an SPI slave, and the pins are configured to SS (slave select input, active low), MOSI (serial data input to modem), MISO (serial data output from modem) and SCLK (serial data clock input). Each SPI operation consists of a control-and-address byte and a data byte.

#### 4.1.3. Parallel Interface

The Si2494/39 can also communicate via a parallel interface. The parallel interface is an 8-bit data bus with a single bit address to memory mapped registers.



#### 4.2. Command Mode

Upon reset, the ISOmodem<sup>®</sup> is in command mode and accepts "AT" commands. An outgoing modem call can be made using the "ATDT#" (tone dial) or "ATDP#" (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 14 on page 49 and enters data mode.

#### 4.3. Data Mode

The Si2494/39 ISOmodem is in data mode while it has a telephone line connection to another modem or is in the process of establishing a connection.

Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4) and data compression to increase throughput (V.44, V.42bis and MNP5).

Each connection between two modems in data mode begins with a handshaking sequence. During this sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

#### 4.4. Fast Connect

The Si2494/39 supports a fast connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, Bell103, and V.29 modulations. See AN93 for details.

#### 4.5. V.80 Synchronous Access Mode

The Si2494/39 supports a V.80 synchronous access mode of operation, which operates with an asynchronous DTE and a synchronous DCE. See "AN93: ISOmodem<sup>®</sup> Chipset Family Designer's Guide".

#### 4.6. Voice Mode (+FCLASS=8)

The Si2494/39 supports the implementation of voice handset, tapeless answering machine (TAM), and speakerphone functions when used with the Si3000 voice codec. The Si3000 provides a direct interface to most handsets, including a variable gain microphone preamplifier, microphone bias for an electret (condenser) microphone, digital volume control, and a speaker driver. Additional Line In/Out ports can be used with external amplifiers to support other audio sources/destinations, such as a microphone and speaker for hands-free operation. Very few external components are required between the handset and the Si3000. See the Si3000 Voiceband Codec with Microphone/Speaker Drive data sheet and AN93 Modem Designer's Guide for more details ITU-T V.253 commands are used to control operation in voice mode. Voice mode is enabled by the AT command +FCLASS=8. The Si2494 /39 DSP provides programmable soft transmit level limiters, programmable transmit and receive gains, sidetone gain, and programmable transmit and receive filters for frequency shaping. These features provide a completely programmable voice implementation capable of compliance with the international standards including TBR 38 and EIA/TIA-470.

Voice mode is typically the system's idle state. While in this state, the ISOmodem monitors the telephone line for various events, such as DTMF detection, caller ID, or ringing (including distinctive ring). Once an event is detected, the ISOModem sends the host either a simple event code (a single character) or a complex event code (multiple characters) preceded by a <DLE> character to the host. For a full list of event reports, see Table 9 on page 22. In voice mode, the ISOmodem can generate DTMF and single tones using the +VTS command; the +VLS command is used to enable event reporting and tone generation and to control the on/off hook state. Table 9 on page 22 lists the events that are supported based on the +VLS state.

#### 4.7. Clocking

The Si2494/39 contains an on-chip phase-locked loop (PLL) and clock generator to derive all necessary internal system clocks from a single clock input. A 32.768 kHz or 4.9152 MHz crystal can be used across XTALI and XTALO pins to form the master clock (±100 ppm max, ±25 ppm recommended) for the ISOmodem. The 32.768 kHz option can provide lower BOM costs and smaller footprint. Alternatively, a clock input of 27 MHz or 4.9152 MHz can be provided to XTALI if that clock source is available in the system. A 4.9152 MHz clock input is the default clock option. Other clock options are selected at power-up through reset strapping. Refer to AN93 for details.



#### 4.8. Low-Power Modes

The Si2494/39 provides multiple low power modes. Using the S24 S-register, the Si2494/39 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the last DTE activity, after the transmit FIFO is empty, and after the last data are received from the remote modem.

Additionally, the Si2494/39 can be placed in wake-on-ring-mode using the command, AT&Z. In either mode, the ISOmodem remains in the sleep state until one of the following occurs:

- A 1-to-0 transition on TXD (UART mode).
- A 1-to-0 transition on SS (SPI mode).
- A 1-to-0 transition on CS (parallel mode).
- An incoming ring is detected.
- A parallel telephone is picked up.
- Line polarity reversal

The Si2494/39 may also be placed in a complete powerdown mode. Once the Si2494/39 completely powers down, it can only be powered back on via the RESET pin.

#### 4.9. Data Compression

The modem can achieve DTE (host-to-ISOmodem) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T V.44, V.42bis, and MNP5 protocols. Data compression attempts to increase throughput by compressing the data before actually sending it. Thus, the modem is able to transmit more data in a given period of time.

#### 4.10. Error Correction

The Si2494/39 ISOmodem can employ error correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The Si2494/39 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

#### 4.11. Wire Mode

Wire mode is used to communicate with standard non-error correcting modems. When optioned with \N3, the Si2494/39 falls back to wire mode if it fails in an attempt to negotiate a V.42 link with the remote modem. Error correction and data compression are not active in wire mode.



Table 9. V.253 Event Reporting in Voice Mode

Event Description	Reporting	+VLS
Caller Id Report	Complex	0,4,20,21
Distinctive Ringing	Complex	0,4,20,21
RING	R	0,4,20,21
DTMF Received	1-9,A-D,*,#	1,5,20,21
Facsimile Calling (e.g. 1100 Hz)	С	1,5,20,21
Data Calling (e.g. 1300 Hz)	е	1,5,20,21
Presumed End of Message (QUIET) Time-out	q	1,5,20,21
Loop Current Interruption	I	1,5,20,21
Ringing Tone	r	1,5,20,21
BUSY	b	1,5,20,21
DIALTONE	d	1,5,20,21
Extension Phone On-hook	р	0,1,4,5,20,21
Extension Phone Off-hook	Р	0,1,4,5,20,21
Facsimile or Data Answer (e.g. 2100 Hz)	а	1,5,20,21
Data Answer (e.g. 2225 Hz)	f	1,5,20,21

#### 4.12. V.92 PCM Upstream

The Si2494/39 supports the ITU-V.92 PCM upstream data protocol. This protocol allows the ISOmodem to connect at speed up to 48 kbps upstream. Previously the upstream connection rate was limited to 33.6 kbps. The PCM upstream mode is enabled by default; to disable, issue the AT command +PIG = 1 (see Table 10 on page 27). To view both downstream and upstream connect speeds in the connect result message, issue the command "AT \V4" or "AT+MR".

#### 4.13. V.92 Quick Connect

The Si2494/39 supports the ITU-V.92 quick connect protocol. Quick connect enables the modem to save and reuse line condition parameters to reduce startup negotiation time.

The quick connect feature is enabled by default in the Si2494/39. For information on changing the quick connect settings, see the +PSS and +PQC commands shown in Table 10 on page 27.

#### 4.14. V.92 Modem-on-Hold

The modem-on-hold (MOH) feature allows the modem user to answer an incoming call while connected online without dropping the internet connection. The modem will remain "on hold" for a period of time determined by the host and the ISP. There are four AT commands that control the operation of MOH. The commands are as follows: +PCW, +PMHT, +PMHT. By changing these parameters, the user can enable/disable call waiting and MOH, set the MOH request timeout, and set the MOH initiate timeout. For further details and syntax on these commands see Table 10 on page 27. The MOH feature is most useful when the Si2494/39 is connected to a central office that allows call waiting.



#### 4.15. Caller ID Operation

The Si2494/39 supports full type I and type II caller ID detection and decode. Caller ID is supported for the US Bellcore, European ETSI, UK, and Japanese protocols and is enabled via the +VCID, +VCDT, and +PCW commands.

#### 4.16. Parallel Phone Detection

The ISOmodem<sup>®</sup> is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem is using the phone line.

#### 4.16.1. On-Hook Line-in-use Detection

When the ISOmodem is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the ISOmodem to monitor the TIP-RING dc voltage with the line voltage sense (LVS) register (U6C, bits 15:8). The LVS bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed twos complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING. The ISOmodem can also monitor the TIP-RING dc voltage using the LVCS register (U79, bits 4:0). See Figure 7 on page 23. See also the %Vn commands for automatic line-in-use detection.

#### 4.16.2. Off-Hook Intrusion Detection

When the ISOmodem is off-hook, an algorithm is implemented in the ISOmodem to automatically monitor the TIP-RING loop current via the LVCS register. During the off-hook state, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. See Figure 8 on page 24. Upon detecting an intrusion, the ISOmodem alerts the host of the condition via the INT pin.

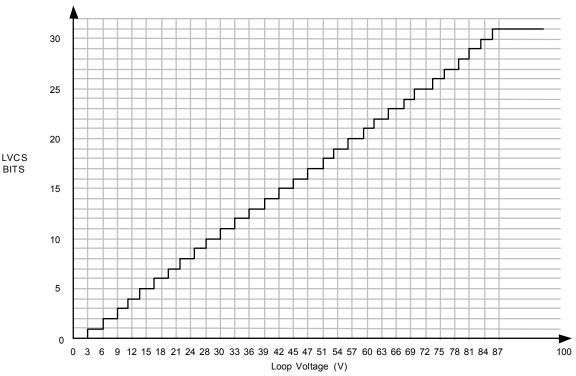


Figure 7. Loop Voltage



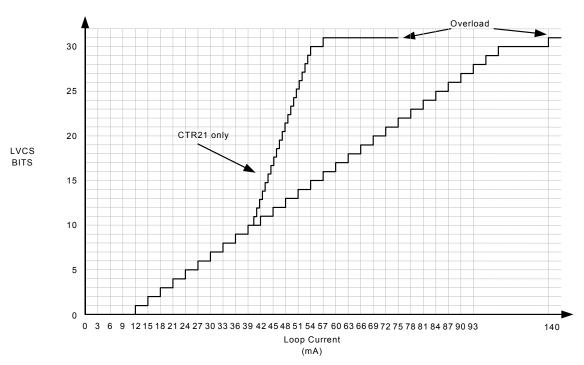


Figure 8. Loop Current

#### 4.17. Overcurrent Detection

The Si2494/39 includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2494/39 goes off-hook. This allows the Si2494/39 to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured. See "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

#### 4.18. Global Operation

The Si2494/39 chipset contains an integrated silicon direct access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. "AN93: Modem Designer's Guide" gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. See AN93 for complete details.

#### 4.19. Firmware Upgrades

24

The Si2494/39 contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2494/39 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field. See AN93 for complete details.

#### 4.20. DTMF Detection / Generation

The Si2494/39 provides comprehensive DTMF tone generation and detection. The ISOmodem can generate single tones or DTMF tones using the +VTS command. DTMF tones may also be generated during dialing using the "ATDT" command. DTMF detection is only available in voice mode (FCLASS = 8). DTMF digits are reported from the modem to the host using <DLE> shielding.



#### 4.21. SMS/MMS Support

Short Message Service (SMS) is a service that allows text messages to be sent and received from one telephone to another via an SMS service center. Multimedia Messaging Service (MMS) extends the core SMS capability to send messages that include multimedia content. The Fax ISOmodem provides an interface that offers a great deal of flexibility in handling multiple SMS standards. This flexibility is possible because most of the differences between standards are handled by the host using the raw data itself. The Si2494/39 performs the necessary modulation/demodulation of the data and provides two options for message packet structure (Protocol 1 and Protocol 2, as defined in ETSI ES 201 912). The rest of the data link layer and transfer layer are defined by the host system.

The content of the message is entirely up to the host including any checksum or CRC. ETSI ES 201 912 describes two standard data and transfer layers that are commonly used. SMS typically relies on caller identification information to determine if the call should be answered using an SMS device or not.

See "6.4. SMS Support" in AN93 for more information on how to configure the modem for SMS support.

#### 4.22. Codec Interface

In order to support a full range of voice and data applications, the Si2494/39 includes an optional serial interface that connects to an external voice codec (Si3000). See AN93 for complete details.

#### 4.23. Answering Machine Support

The TAM voice compression support includes the following formats:

- Signed linear 8-bit, 64 kbps
- Unsigned linear 8-bit, 64 kbps
- G.711 μ-law 8-bit, 64 kbps
- G.711 A-law 8-bit, 64 kbps
- G.726 ADPCM 2-bit, 16 kbps
- G.726 ADPCM 4-bit, 32 kbps

All formats use a fixed 8 kHz sampling rate. For most applications, the user wants a high-quality message format (64 kbps) for the Outgoing Message (OGM) and is less concerned about the Incoming Message (ICM) quality. Higher compression results in less memory use. Less compression results in higher speech quality. See AN 93 for details. This section covers the functional operation of handset, TAM, and speakerphone modes and includes use cases with the programming examples.

#### 4.24. Voice Pass-Through (Speakerphone)

Voice pass-through operation employs an acoustical echo canceller (AEC), acoustical echo suppressor (AES), double-talk detector (DTD), and line echo canceller (LEC). They provide the following performance:

- Programmable echo tail filter length: up to 64 ms
- Convergence speed (white noise): < 1.6 s</p>
- Single-talk echo suppression: > 48 dB
- Double-talk echo suppresion: > 30 dB

See Appendix of AN93 for details. This section covers the functional operation of handset, TAM, and speakerphone modes and includes use cases with programming examples.

#### 4.25. General-Purpose Tone Detectors

Two general-purpose tone detectors based on 4th-order I-quad filters are provided in addition to the other dedicated tone detectors described in this document. These tone detectors are referred to as the Tone A detector and the Tone B detector. They can operate independently or Tone B can receive the output of Tone A to implement a higher-order tone detector. All filter coefficients and detector functions are controlled through U-Registers.

These tone detectors are available for use in any operational mode. Whenever an enabled tone detector output transitions, a message will be generated. The messages follow the DLE shielded format for complex reporting. Refer to AN93 for more details.

