Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Si2704/05/06/07-A10

EMI MITIGATING 2.1x 5 W CLASS D AUDIO AMPLIFIER

Features

- Digital input Delta-Sigma PWM
- Patent-pending EMI mitigation
- AM radio band noise-free notch
- GSM/iPhone friendly
- Wideband PWM carrier spreading
- Power stage slew rate control
- Power stage feedback for PSR/THD
- 2x 5 W @ 3 Ω BTL; 2x 3 W @ 8 Ω BTL
- 88% efficiency with >50 dB PSRR
- 95 dB dynamic range and <0.1% THD
- Stereo PWM DAC line analog outputs
- Master/slave I²S w/ 3 inputs & 1 output
- Automatic digital audio rate detection
- Standard audio rates from 32–192 kHz
- Audio activity detector w/ auto-standby
- Operates from external XTAL or clock
- Buffered master/regulator clock output
- Programmable 7 band parametric EQ, dynamic range compressor, tone control
- Crossbar input mixer with scaling
- Digital tone and alert generation
- 128 dB volume control in 0.5 dB steps
- Multiple low power operating modes
- Over-current and over-temperature detection w/ auto recovery
- Pop and click free operation
- Standard 2-wire control w/ 2 addresses
- System flexibility w/ 3 multi-function pins
- Dual supply voltage: 2.7–3.6 V main and 4.0–6.6 V power stage
- Available in 4x4 24-pin Power QFN and 7x7 48-pin Power eTQFP package
  - Both Pb-free/RoHS compliant

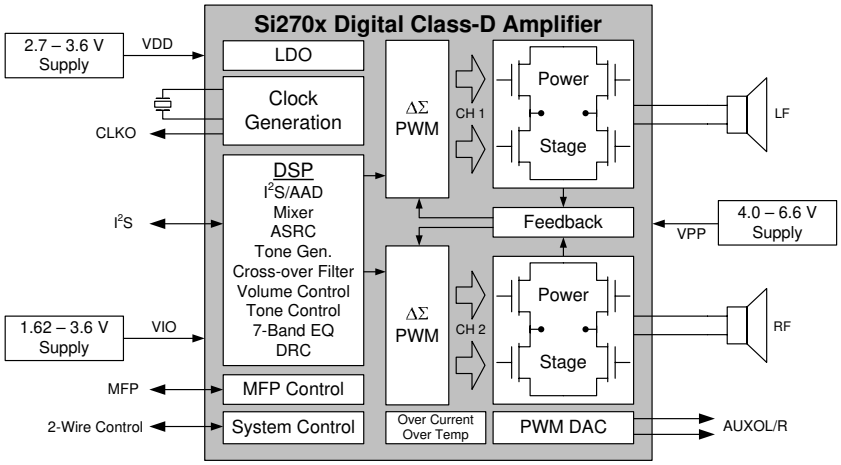
Applications

- PMP/MP3 docking stations
- Portable consumer audio electronics
- Table top and portable radios
- Active/wireless speakers
- TVs and monitors
- TV sound bars

Description

The Si2704/05/06/07 EMI mitigating 2.1 digital audio processing Class D amplifier integrates a power stage, PWM DAC, and digital audio processing (DAP) for simplified, low cost, power efficient system designs in consumer audio electronics. The digital input amplifier features delta-sigma PWM and innovative EMI mitigation technology for producing high-quality audio while effectively managing PWM switching noise for enhanced EMI compliance and AM/FM radio co-existence, while also being GSM/iPhone friendly.

Functional Block Diagram

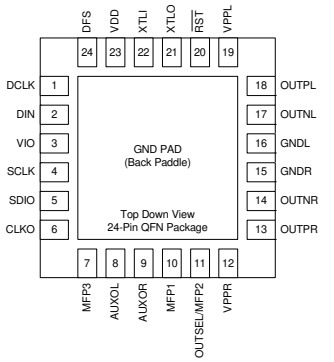


Ordering Information:

See page 37.

Pin Assignments

Si2704/05/06/07



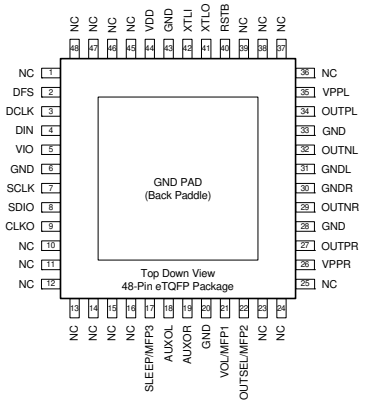


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Output Supply Voltage	V_{PP}		4.0[2]	—	6.6	V
Main Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Interface (I/O) Supply Voltage	V_{IO}		1.62	—	3.6	V
Load Impedance	R_L		—	3–8	—	Ω
Ambient Temperature	T_A		–20	25	85	°C
Junction Temperature	T_J		—	—	135	°C
Case Delta from Junction	θ_{JC}	Temperature delta between junction and top center of package	—	—	5	°C/W
Delta from Junction to Ambient[3]	θ_{JA}	QFN package	—	25	—	°C/W
		eTQFP	—	30	—	°C/W

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
2. Operation with V_{PP} as low as 3 V is possible at reduced performance.
3. The θ_{JA} is layout-dependent; therefore, PCB layout must provide adequate heat-sink capability. The.θ_{JA} is specified, assuming adequate ground plane as in “AN470: 270x Layout Guidelines.”

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Power Output Supply Voltage	V_{PP}	–0.5 to 7.0	V
Main Supply Voltage	V_{DD}	–0.5 to 3.9	V
Interface (I/O) Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[2]	I_{IN}	10	mA
Input Voltage[2]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_A	–20 to +85	°C
Junction Temperature	T_J	150	°C
Storage Temperature	T_A	–55 to +150	°C

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins SCLK, SDIO, DCLK, DFS, DIN, $\overline{\text{RST}}$, OUTSEL, MFPx.

Table 3. DC Characteristics—Supplies and Interfaces

(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 4 to 6.6 V, T_A = –20 to +85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start Up Time	T_{ONSB}	From Standby Mode with CLKO enabled	—	—	2	ms
		From Standby Mode with CLKO disabled	—	—	20	ms
	T_{ON_SLP}	From Sleep Mode	—	—	20	ms
	T_{ON_PD}	From Power Down Mode	—	—	200	ms
Active Mode Quiescent Supply Current	I_{PQ}	From V_{PP}, No load, Both Channels Active, Spread Mode PWM	—	50	—	mA
		From V_{PP}, No load, Both Channels Active, Normal Mode PWM	—	45	—	mA
	I_{DQ}	From V_{DD}	—	54	—	mA
	I_{IOQ}	From V_{IO}, I^2S Slave Mode, CLKO Disabled	—	1.3	—	mA
Standby Mode Supply Current	I_{PSTB}	Standby Mode	—	0.1	—	mA
	I_{DSTB}	Standby Mode with CLKO enabled	—	8	—	mA
		Standby Mode with CLKO disabled	—	4	—	mA
	I_{IOSTB}	Standby Mode	—	2	—	mA
Sleep Mode Supply Current	I_{PSLP}	SLEEP asserted	—	0.1	—	mA
	I_{DSLP}	SLEEP asserted	—	2	—	mA
	I_{IOSLP}	SLEEP asserted	—	1.5	—	mA
Power Down Mode Supply Current	I_{PPD}		—	0.1	—	mA
	I_{DPD}		—	2	—	mA
	I_{IOPD}		—	0.3	—	mA
Input pins SCLK, SDIO, DCLK, DFS, DIN, $\overline{RST}$, OUTSEL, MFPx						
High Level Input Voltage	V_{IH}		0.7 x V_{IO}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{IO}	V
High Level Input Current	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
Output pins MFPx, CLKO*						
High Level Output Voltage	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V
High Level Output Current	I_{OH}	0.8 x V_{IO}	—	6	—	mA
Low Level Output Current	I_{OL}	0.2 x V_{IO}	—	6	—	mA

***Note:** Valid for the configuration where MFPx is configured as an output or general purpose output.

Table 4. DC Characteristics—Class D Amplifier

(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 4 to 6.6 V, T_A = –20 to +85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage Offset	V_{OS}	Differential Output	—	±10	—	mV
Total Drain-Source On-State Resistance (Total Bridge)*	R_{DSON}	V_{PP} = 6.6 V, I_O= 1A	—	648	—	mΩ
***Note:** Excludes package bond wire resistance.						

Table 5. AC Characteristics—Class D Amplifier

(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 6.6 V, R_L = 8 Ω, VOL = 0 dBFS, T_A = –20 to +85 °C, unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Continuous Output Power[1]	P_O	THD+N = 10%, f = 1 kHz, R_L = 8 Ω	—	2.7	—	W
		THD+N = 1%, f= 1 kHz, R_L = 8 Ω	—	1.9	—	W
		THD+N = 10%, f = 1 kHz, R_L = 4 Ω	—	4.7	—	W
		THD+N = 1%, f= 1 kHz, R_L = 4 Ω	—	3.4	—	W
		THD+N = 10%, f = 1 kHz, RL = 3 Ω	—	5.0	—	W
Total Harmonic Distortion + Noise	THD+N	P_O=1 W, f = 1 kHz	—	0.1	—	%
Signal to Noise Ratio/Dynamic Range	SNR	Normal mode PWM, f = 1 kHz, A-weighted	—	95	—	dB
		Normal mode PWM, f = 1 kHz, Unweighted	—	92	—	dB
		Spread mode PWM, f = 1 kHz, A-weighted	—	90	—	dB
		Spread mode PWM, f = 1 kHz, Unweighted	—	87	—	dB
Spread Mode Common Mode PWM Carrier Peak Attenuation[2]		f = 1 kHz, Relative to Normal Mode	—	24	—	dB
Common Mode AM Band Noise Notch Attenuation[3]		f = 1 kHz, Measured in ±10 kHz band around selected frequency	—	35	—	dB

Notes:
1. Measured at filter output. Power measured at the chip output is greater.
2. Guaranteed by characterization.
3. Measured relative to the integrated noise floor in Spread mode. Guaranteed by characterization.
4. Does not include filter efficiency losses.

Table 5. AC Characteristics—Class D Amplifier (Continued)
(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, V_{PP} = 6.6 V, R_L = 8 Ω, VOL = 0 dBFS, T_A = –20 to +85 °C, unless otherwise noted.)

Power Supply Rejection Ratio	PSRR	P_O = –3 dBFS, f = 1 kHz; 200 mV_{PP}, f_r = 400 Hz supply ripple	—	50	—	dB
Crosstalk		f = 1 kHz	—	–92	—	dB
Efficiency[4]	η	f = 1 kHz, half rate PWM and 10 ns slew rate	—	88	—	%
Output Pulse Repetition Frequency	PRF	Half Rate PWM	—	480	—	kHz
		Full Rate PWM	—	960	—	kHz

Notes:
1. Measured at filter output. Power measured at the chip output is greater.
2. Guaranteed by characterization.
3. Measured relative to the integrated noise floor in Spread mode. Guaranteed by characterization.
4. Does not include filter efficiency losses.

Table 6. AC Characteristics—PWM Digital to Analog Converter
(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, VOL = 0 dBFS, T_A = -20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	f = 1 kHz	—	0.02	—	%
Signal to Noise Ratio/Dynamic Range	SNR	f = 1 kHz, A-weighted	—	88	—	dB
		f = 1 kHz, Unweighted	—	85	—	dB
Output Voltage Swing	Vout		—	1	—	V_{P-P}
Output Voltage Common Mode Bias	Voutcm		—	0.8	—	V
Output Load— Resistance	R_{load}	AC coupled	5	—	50	kΩ
Output Load— Capacitance	C_{load}	AC coupling capacitor	0.1	—	1	µF

Table 7. I^2S Digital Audio Interface Characteristics
(V_{IO} = 1.62 to 3.6 V, T_A = –20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Input Cycle Time	$t_{CYC:DCLK}$		70	—	—	ns
DCLK Input Pulse Width High	$t_{HI:DCLK}$		0.4 x $t_{CYC:DCLK}$	—	0.6 x $t_{CYC:DCLK}$	ns
DCLK Input Pulse Width Low	$t_{LO:DCLK}$		0.4 x $t_{CYC:DCLK}$	—	0.6 x $t_{CYC:DCLK}$	ns
DFS Setup Time to DCLK↑	$t_{SU:DCLK}$		10	—	—	ns
DFS Hold Time after DCLK↑	$t_{HD:DCLK}$		5	—	—	ns
DOUT Output Delay	$T_{PD:DCLK}$		0	—	35	ns
Capacitive Loading	C_B		—	—	15	pF

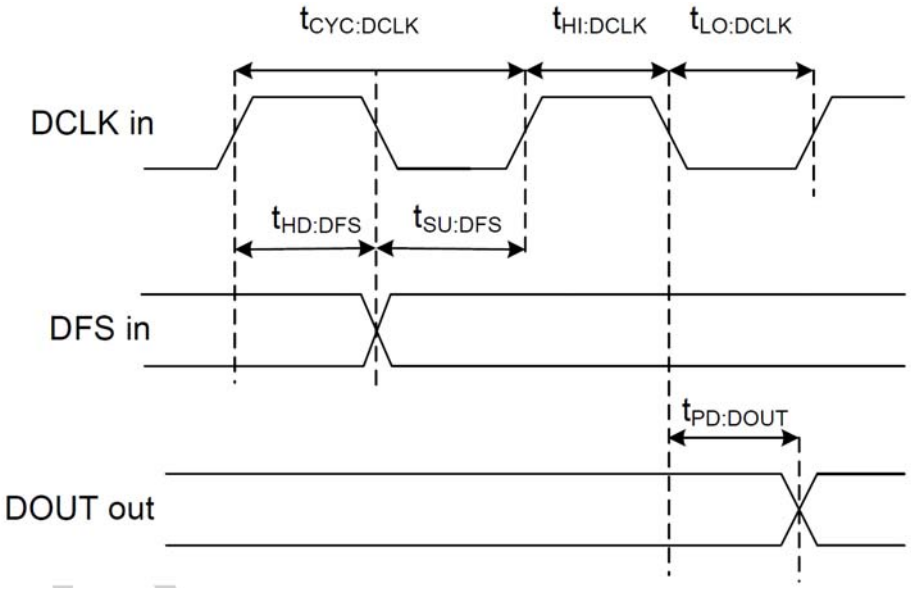


Figure 1. Digital Audio Timing Parameters

Table 8. 2-Wire Control Interface Characteristics

(V_{IO} = 1.62 to 3.6 V, T_A = –20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input from SDIO Setup ↓ (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold	$t_{HD:DAT}$		0	—	900	ns
SDIO output delay	$T_{PD:DAT}$		300	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		—	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		—	—	300	ns
Capacitive Loading	C_b		—	—	50	pF
Pulse Width Rejected by Input Filter	t_{SP}		—	—	50	ns

Table 9. 2-Wire Control Interface Address Selection

CLKO Startup Voltage (Pin Connection)	2-Wire Device Address
GND	1001010 (0x94)
V_{IO} (Default)	0011011 (0x36)

Table 10. Reset Timing Characteristics

(V_{IO} = 1.62 to 3.6 V, T_A = -20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKO Setup Time to $\overline{RST}$↑	t_{SRST}		100	—	—	µs
CLKO Hold Time after $\overline{RST}$↑	T_{HRST}		30	—	—	ns

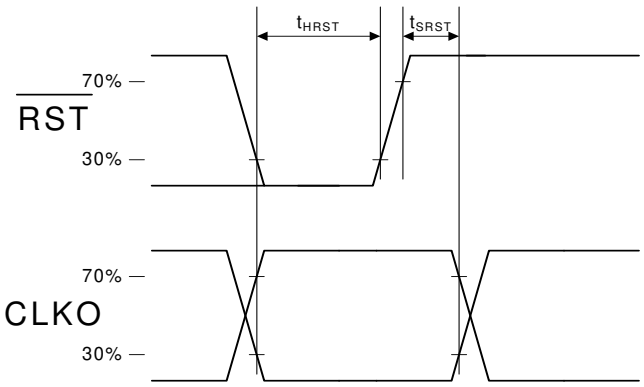


Figure 2. Reset Timing Parameters for Configuration Mode Select

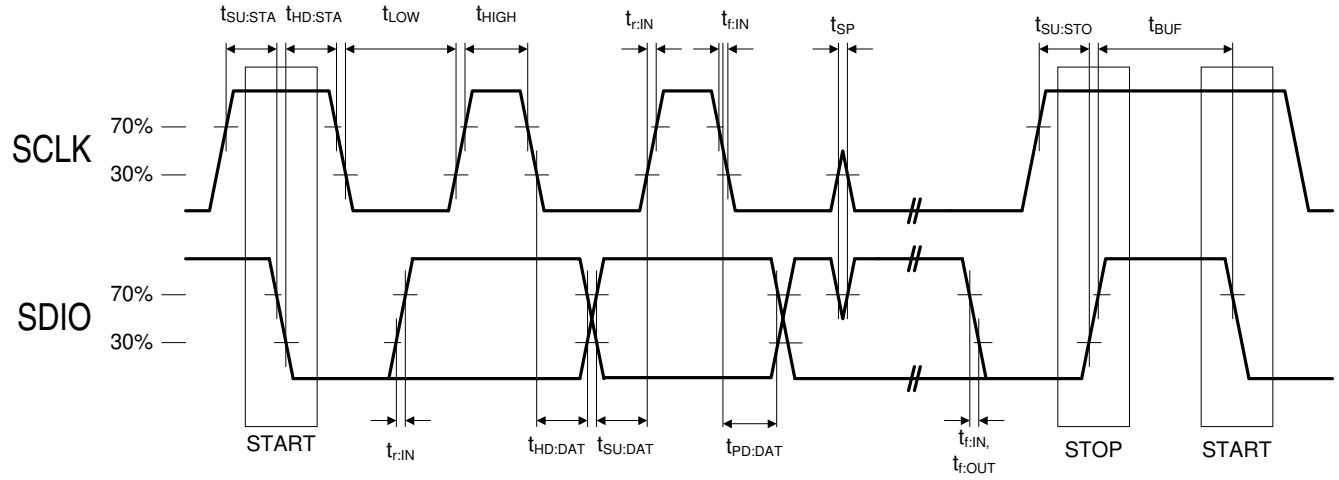


Figure 3. 2-Wire Control Interface Read and Write Timing Parameters

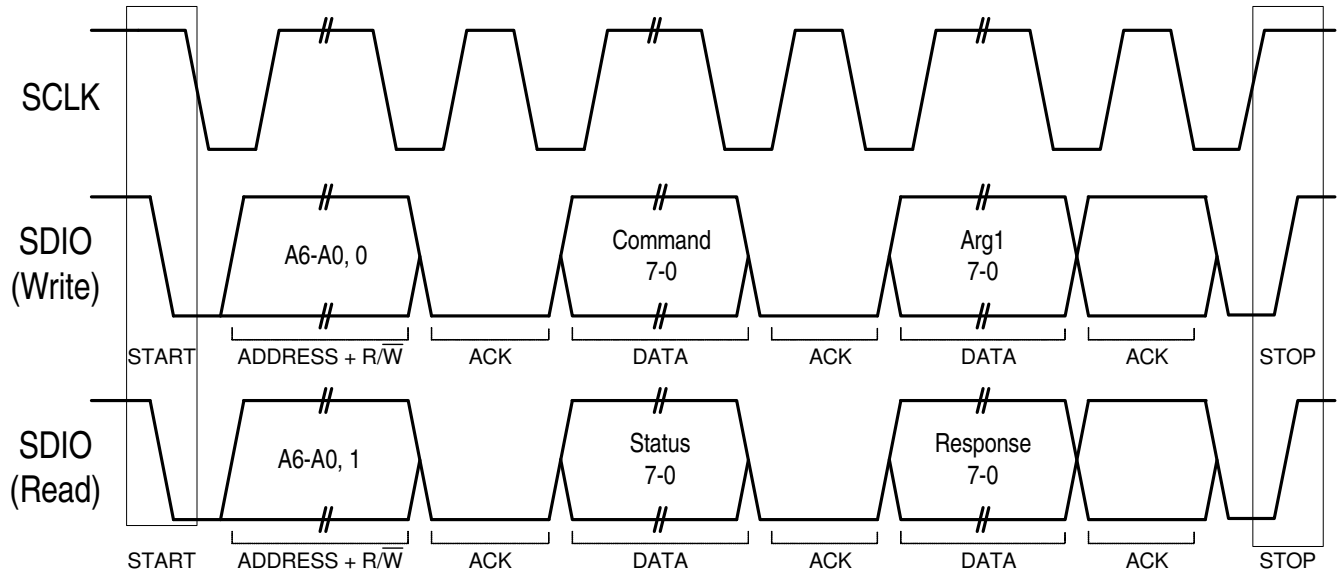


Figure 4. 2-Wire Control Interface Read and Write Timing Diagram

Table 11. Reference Clock and Crystal Characteristics

(V_{DD} = 2.7 to 3.6 V, V_{IO} = 1.62 to 3.6 V, T_A = –20 to +85 °C, unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock, Pin XTLI						
Supported Frequencies[1]			2	—	49	MHz
Frequency Tolerance			–1000	—	1000	ppm
Jitter Tolerance[2]		Integrated from 20 Hz to 1 MHz	—	—	50	psrms
High Level Input Voltage	V_{IH}		0.7xV_{IO}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3xV_{IO}	V
High Level Input Current	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V V_{IO} = 3.6 V	–10	—	10	µA
Crystal oscillator, Pins XTLI, XTLO						
Crystal Oscillator Frequency[3]			12.288	—	24.576	MHz
Crystal Frequency Tolerance			–1000	—	1000	ppm
Internal Crystal Load Capacitance			4	—	20	pF
Crystal Motion Resistance		for 24.576 MHz Crystal	—	—	100	Ω
Reference Clock Output, Pin CLKO						
Frequency Range[4]			120	—	24576	kHz
Load Capacitance			—	—	10	pF

Notes:

1. Supported reference clock frequencies at XTLI include 2.048, 2.822, 3.072, 4.096, 4.234, 4.608, 5.645, 6.144, 8.192, 8.467, 9.216, 11.290, 11.2896, 12, 12.288, 16.368, 16.934, 18.432, 22.579, 24.576, 32.768, 32.869, 36.864, 45.158, and 49.152 MHz.
2. Required to achieve specified performance.
3. Supported crystal frequencies at XTLI include 12.288, 18.432, and 24.576 MHz.
4. 120 kHz, 240 kHz, 480 kHz, 960 kHz, 1.92 MHz, 4.096 MHz, 6.144 MHz, 8.192 MHz, 12.288 MHz, 16.384 MHz, and 24.576 MHz are available at CLKO.

2. Typical Application Schematic

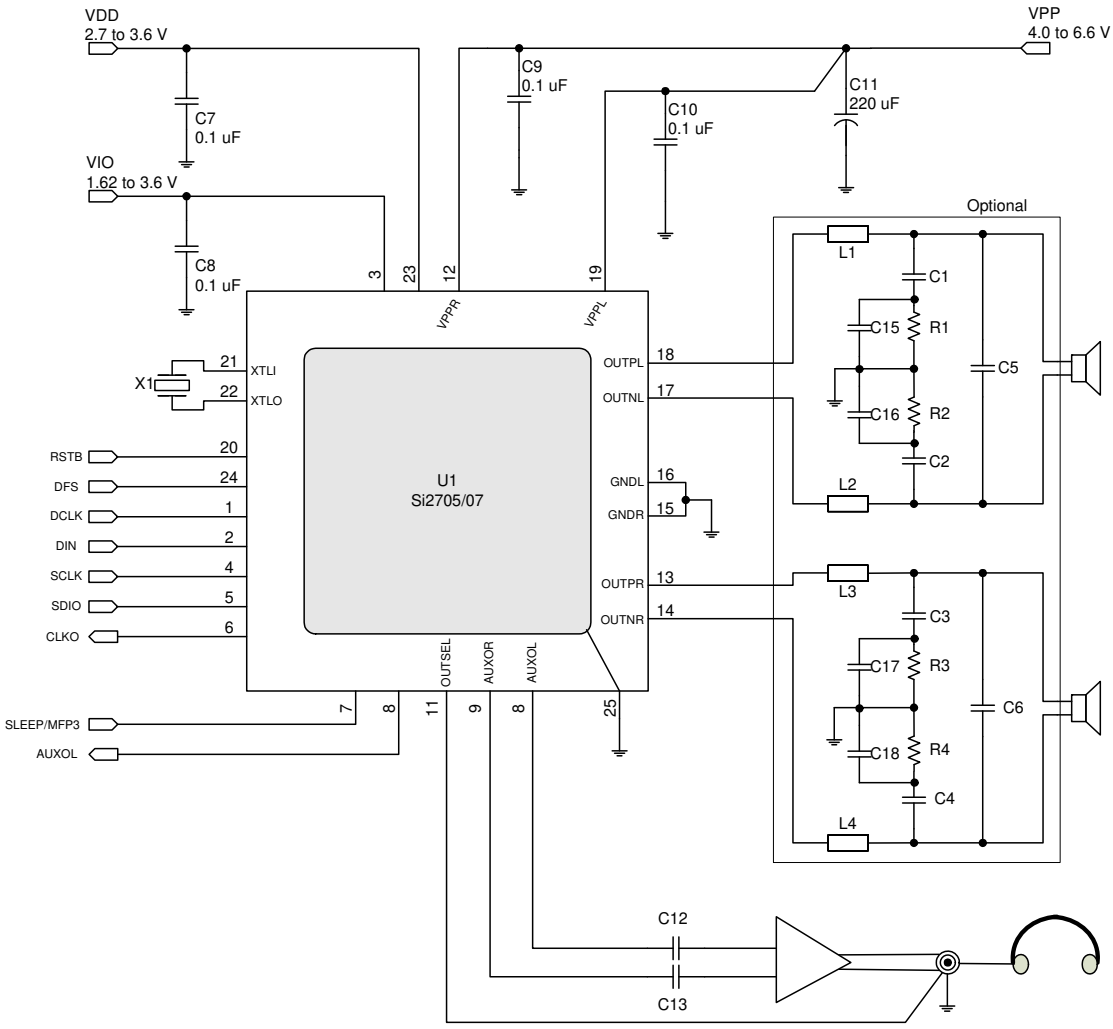


Figure 5. Typical Application Schematic

Table 12. Typical Application Schematic Bill of Materials

Component	Inductor Filter	Ferrite Bead Filter
C1, C2, C3, C4	0.68 µF, ceramic	1000 pF, ceramic
C15, C16, C17, C18	0.33 µF, ceramic	1000 pF, ceramic
C5, C6	0.47 µF, Film	100 pF, ceramic
L1, L2, L3, L4	10 µH, 1.5 A, inductor	TDK MPZ2012S601A, ferrite bead
Note: When using the ferrite bead output filter with AM radio, shielded cable is recommended.		

3. Typical System Configurations

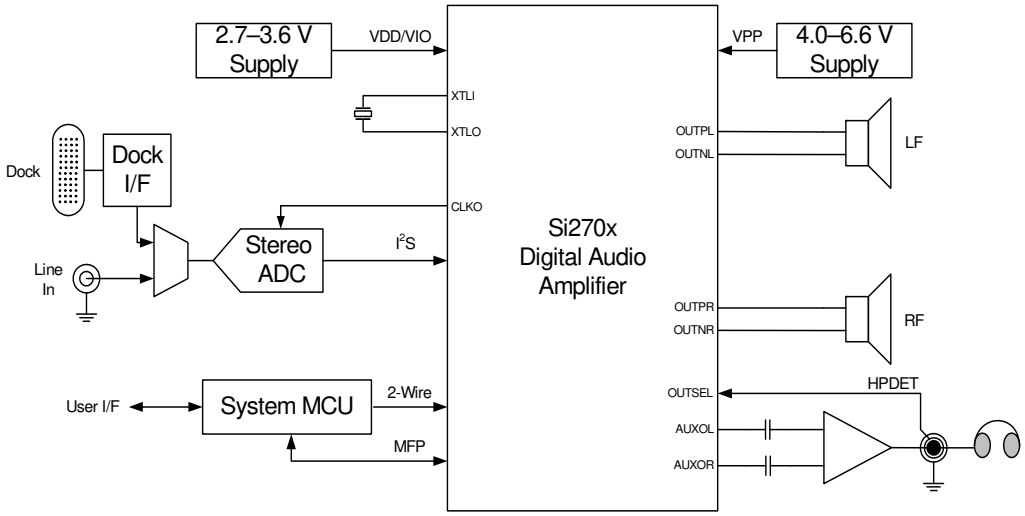


Figure 6. Basic PMP Dock System Configuration

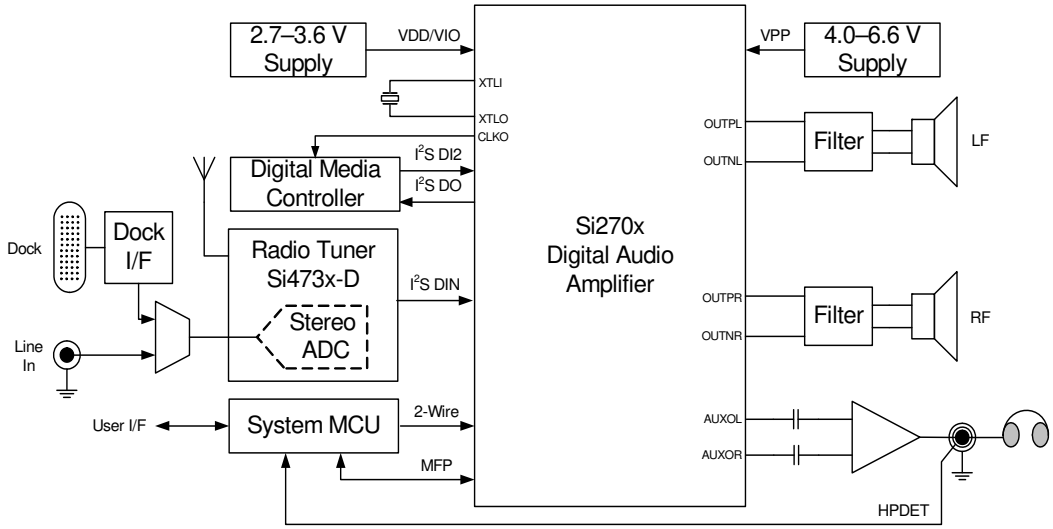


Figure 7. PMP Dock with Radio and Digital Media Controller System Configuration

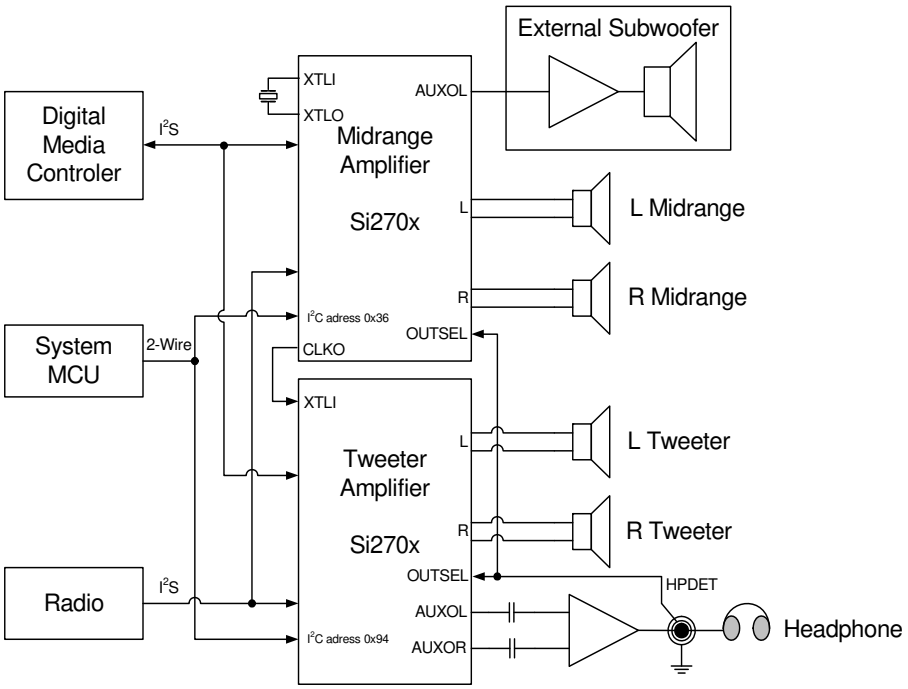


Figure 8. Stereo 2-Way Speaker System Configuration

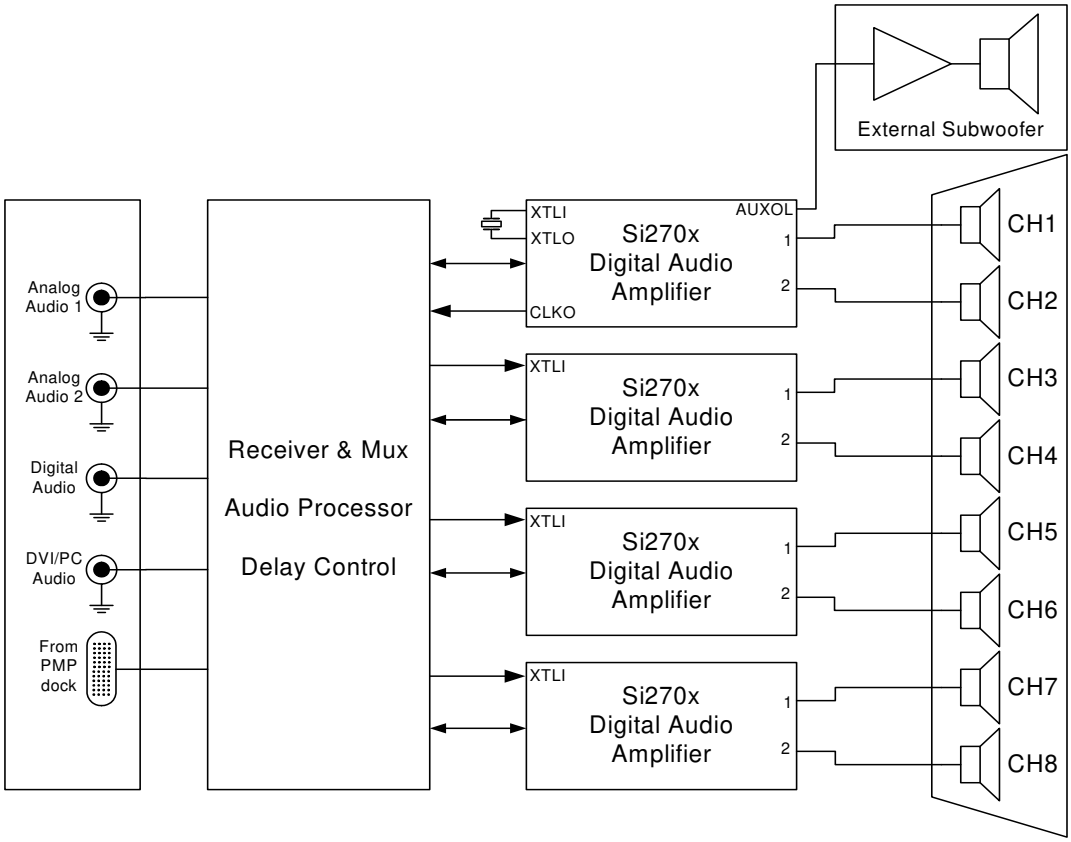


Figure 9. TV Sound Bar System Configuration

4. Functional Description

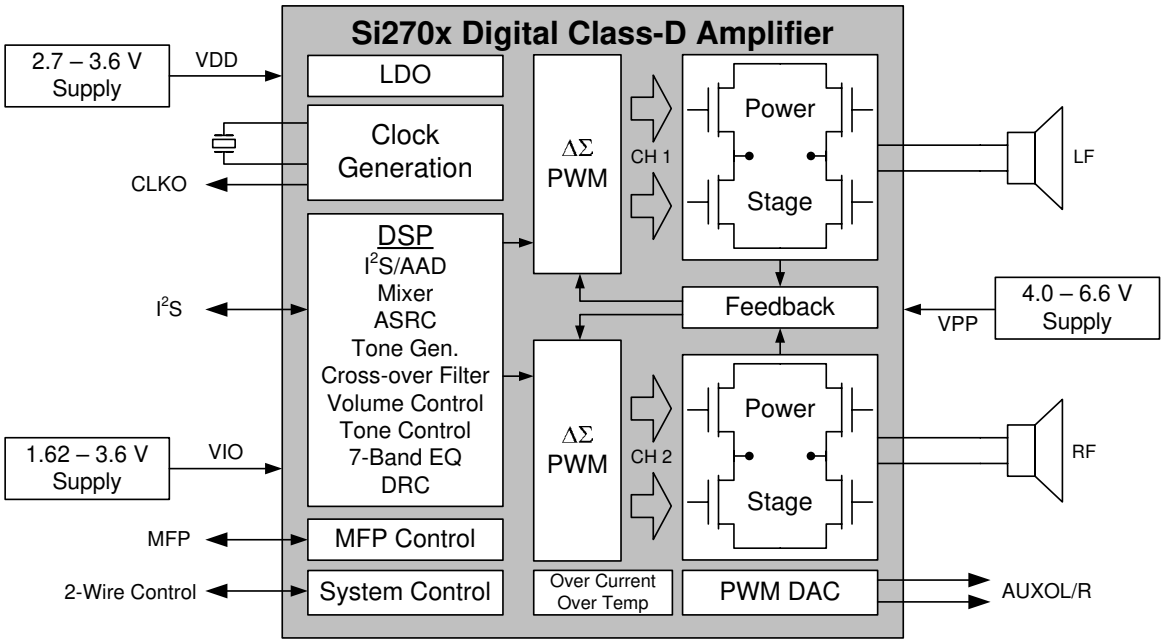


Figure 10. Functional Block Diagram

The Si2704/05/06/07 EMI mitigating 2.1 x 5 W Class D audio amplifier integrates a stereo power stage, PWM DAC, and digital signal processor (DSP) to enable simplified, low cost, power efficient system designs in consumer audio electronics. The digital input amplifier features delta-sigma PWM for high quality audio while innovative EMI mitigation technology manages PWM switching noise to suppress peak emissions more than 20 dB while providing co-existence with AM/FM radio tuners.

The power stage is capable of driving two 3 Ω bridge-tied speakers with 5 W per channel at 10% THD+N from 6.6 V power supplies. It can also drive 8 Ω bridge-tied speakers at 3 W per channel with 88% efficiency. The power stage feedback systems improve power supply rejection and harmonic distortion performance.

The Si270x connects up to three synchronous I^2S digital sources as either master or slave, two of which can be configured as input or output. The I^2S input is converted to a common sample rate for digital audio processing using an asynchronous sample rate converter (ASRC) and a digital crossbar mixer linearly combines any of the six inputs into the three audio processing channels

Integrated digital audio processing enables the amplifier to compensate for speaker and enclosure acoustic characteristics. A programmable 7-biquad parametric equalizer for each main channel allows notching out of mechanical resonances and pre-compensation of the speaker frequency response, while programmable dynamic range compression protects from overdriving speakers and increases the average output power without increasing apparent distortion. Tone control enables ±18 dB of treble and bass boost/cut, while output volume is digitally controlled in 0.5 dB steps from –100 to +28 dB via the I^2C-Compliant 2-Wire interface or an analog potentiometer connected to the integrated ADC. Two independent tone generators enable mixing of multi-tone alarms and alerts into the audio channels.

The auxiliary audio processing channel (Aux Channel) with optional sub-mixing and low pass filtering generates mono line level analog audio output for driving an external active subwoofer or center speaker. The main channel L/R outputs may also be connected to the PWM DAC for driving a headphone amplifier.

A low jitter PLL generates internal system clocks referenced in master mode to an external crystal, or alternatively, in slave mode to either the I^2S data clock (DCLK) or the audio master clock (MCLK). A buffered clock (CLKO) can be output by the device to synchronously drive companion audio devices, additional amplifiers, and switching regulators.

4.1. PWM Processing

The Si270x is designed to operate using a bridge-tied-load (BTL) output configuration where both sides of the speaker are actively driven by the amplifier.

4.1.1. PWM Switching Rate Control

The output PWM switching frequency can be programmed via 2-wire control to be half rate (480 kHz) or full rate (960 kHz). The different rates can be configured by setting property PWM_FREQ.

Full Rate PWM provides better audio performance and AM radio co-existence, while Half Rate PWM provides lower switching losses and lower switching energy harmonics at high frequencies. For each configuration, the switching frequency can be offset slightly for FM band frequency planning flexibility.

4.1.2. EMI Mitigation

By nature, the switching characteristic of Class D amplifiers that provides high power efficiency also creates harmonic spurs at multiples of the PWM switching rate that can radiate as EMI. Common mode PWM switching from ground to the supply translates into a radiated pattern with large energy components at the fundamental and odd harmonics of the switching frequency. Fast pulse edge transitions and differential mode ripple currents flowing through inductor windings further contribute to radiated interference. To simplify design for EMI compliance and radio receiver co-existence, the Si270x features EMI mitigation modes for managing the PWM switching noise, including pulse edge slew rate control, common mode switching noise spectral shifting, and common mode switching noise spectral spreading/shaping.

4.1.2.1. Slew Rate Control

Output pulse edge slew rate can be programmed via 2-Wire control for 10 ns or 20 ns (property PWM_OUTPUT_SLEW_RATE). While faster transition times are favorable for higher efficiency, slower transition times are favorable for EMI attenuation.

4.1.2.2. Spectral Shifting

The frequency locations for the PWM common mode switching energy can be shifted to facilitate frequency planning. This spectral shifting is useful for example in radios to avoid radiating interference at frequencies where the radio is being tuned.

When spectral shifting is programmed for Integer Mode PWM, the common mode switching energy and harmonics are located at F_C x (2n–1) for all positive integers n, where Fc is the PWM switching frequency. Alternatively, when programmed for Fractional Mode PWM, the common mode switching energy and harmonics are shifted down in frequency by 50%, and are located at F_C x (2n–1)/2.

The spectral shifting mode can be programmed dynamically by setting property PWM_CONFIG during normal operation without adversely affecting the internal audio processing or the amplified audio signal integrity.

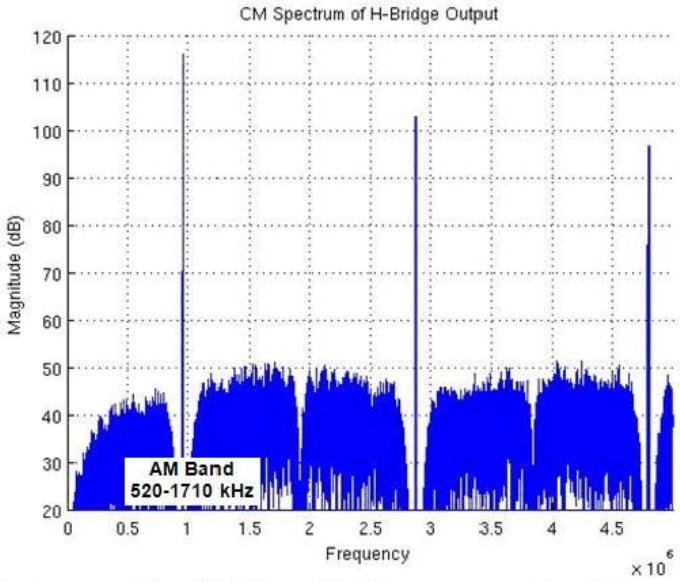


Figure 11. PWM CM Spectrum for Integer Mode PWM

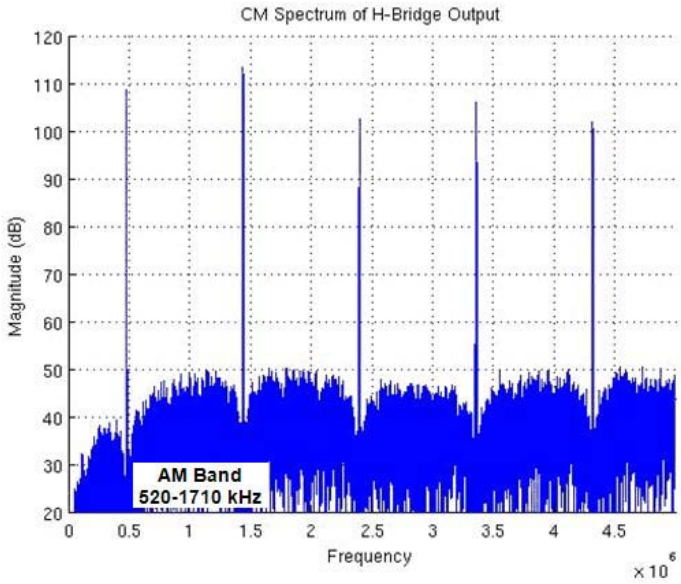


Figure 12. PWM CM Spectrum for Fractional Mode PWM

4.1.2.3. Spectral Spreading

Spread mode PWM can be used to spread PWM common mode switching energy resulting in a peak energy suppression greater than 20 dB at all frequencies. This Spectral Shaping feature is useful for mitigating EMI radiation and eliminating inductors for filter-less applications. Spread Mode PWM can be programmed dynamically by setting property PWM_CONFIG during normal operation without adversely affecting the internal audio processing or the differential output signal integrity.

4.1.2.4. Spectral Shaping Noise-Free Notch for AM Radio (Si2705/07 only)

When using Spread Mode PWM with full rate PWM switching (960 kHz), a tunable noise-free notch can be programmed via 2-Wire control to shape the switching noise and create a narrow frequency band in the AM radio spectrum in which the PWM common mode switching energy is not allowed to spread. This noise-free notch is

nominally 20 kHz wide and tunable in 5 kHz increments from 520 to 1710 kHz, virtually equalizing the noise level across the band. The noise-free notch can be dynamically tuned during normal operation without adversely affecting the internal audio processing or the differential output signal integrity.

Spread Mode PWM with the tunable noise-free notch is useful for systems in which the Si2705/07 needs to co-exist with an AM radio receiver. In normal AM radio operation, the system MCU programs the noise-free notch frequency in the Si2705/07 to the same frequency as the AM radio to inhibit PWM switching noise from interfering with radio reception. Because Spread Mode PWM is also engaged, switching noise outside of the noise-free notch band is also suppressed for mitigating broadband EMI radiation

The noise-free notch can be placed at different frequencies by programming property PWM_AM_TUNE_FREQ. More information on the complete range of programming parameters and settings available for optimized operation can be found in the “AN469: Si270x Programming Guide”.

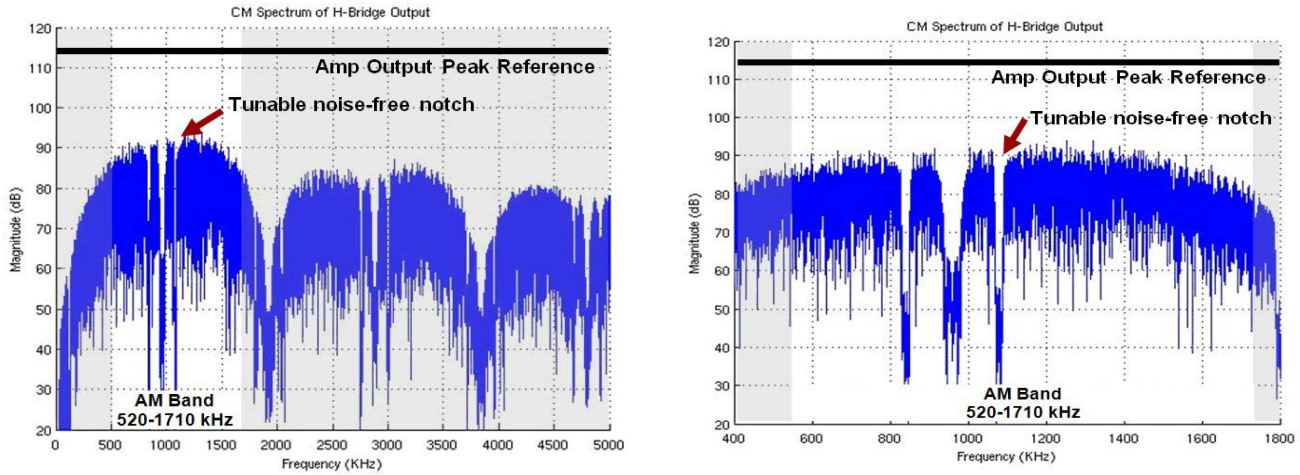


Figure 13. PWM CM Spectrum for Spread Mode PWM with Noise-Free Notch

4.2. Operating Modes

The Si2704/05/06/07 features four operating modes: one active mode (Active) and three low power modes (Standby, Sleep and Power Down). The low power modes differ on power consumption and wake up times, providing the flexibility to meet system design requirements. See Table 3, “DC Characteristics—Supplies and Interfaces,” on page 6 for additional information on startup times and power consumption.

Figure 14 illustrates the device state diagram highlighting the key operating modes and the allowed transitions.

For more information concerning operating modes and their programming requirements, refer to “AN469: Si270x Programming Guide”.

4.2.1. Active Mode

Active mode is the normal operational mode in which the chip accepts digital I^2S data at the input, drives an audio output and is programmable via a 2-Wire interface bus.

Active Mode is initiated by setting the ACTIVE argument of the ACTIVATE command via the 2-Wire interface. To avoid clicks and pops in the audio output, mute is de-asserted after entering Active Mode.

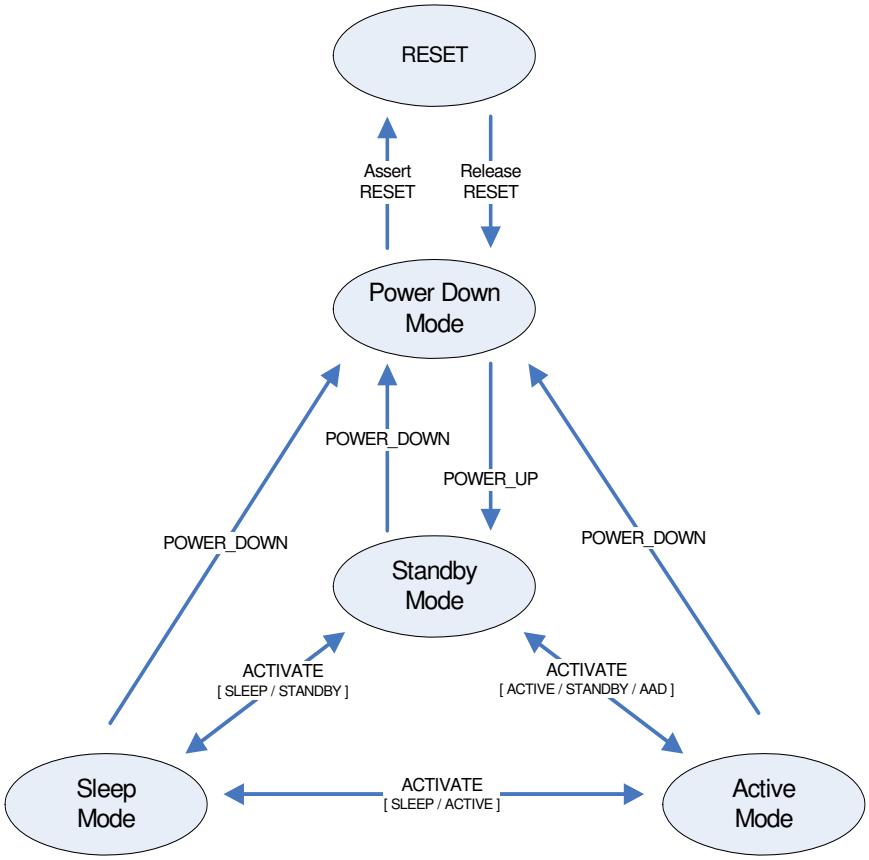


Figure 14. Operating Modes

4.2.2. Standby Mode

Standby Mode is a reduced power state where the register states are preserved and the 2-Wire interface is fully operational, allowing for new parameters and configuration settings to be programmed even though the amplifier output is powered down. This state has the shortest wake-up time relative to the other low power modes. If the buffered reference clock output (CLKO) is enabled, the timing generation circuitry remains active.

Standby Mode is initiated by setting the STANDBY argument of the ACTIVATE command via the 2-Wire interface. Standby Mode can also be initiated by setting the AAD argument of the ACTIVATE command, which additionally enables the Audio Activity Detector. See "4.5.2. Audio Activity Detector" on page 24 for additional information about this setting.

To avoid clicks and pops in the audio output, mute is first asserted before entering Standby Mode.

4.2.3. Sleep Mode

Sleep Mode is the lowest power consumption state in which the chip parameters and configurations are retained. However, chip parameter and configuration settings cannot be programmed and the buffered reference clock output (CLKO) is disabled in this mode. The time to activate the chip is shorter from the Sleep Mode than when activating from the Power Down Mode.

Sleep mode is initiated by setting the SLEEP argument of the ACTIVATE command.

4.2.4. Power Down Mode and Reset

Asserting the $\overline{\text{RST}}$ pin low disables the analog and digital circuitry, resets the registers to their default settings, and disables the 2-Wire bus. The $\overline{\text{RST}}$ pin should always be asserted low when power to the device is ramped up, and released once the power supply voltages have stabilized.

After $\overline{\text{RST}}$ is released high, the chip comes up in Power Down Mode with the registers set to their default values. The 2-Wire interface remains active but only responds to the POWER_UP command that puts the device into

Standby Mode so that the high power outputs are prevented from being enabled prior to the registers being configured. Any other command sent to the device is acknowledged on the bus but ignored by the device. This mode has the highest wake-up time and lowest power consumption of the three low power modes.

A POWER_DOWN command causes a transition to Power Down Mode, disabling the outputs and resetting all parameter registers to default values.

4.3. Chip Configuration

The Si270x can be programmed via the 2-Wire interface for several operating configurations.

4.3.1. Multi-Function Pins (MFPs)

Three multi-function pins (MFPs) support a wide range of system configurations while minimizing pin count. These MFPs are programmed via the 2-Wire interface. Table 13 outlines all available signals, and Table 14 shows the signal configuration options available on each MFP with the default in bold.

Table 13. Multi-Function Signal Definitions

Signal Name	Functional Description
OUTSEL	Tri-level output mode select
$\overline{\text{INT}}$	Interrupt flag
DIN2	I^2S data input 2
DIN3	I^2S data input 3
DOUT	I^2S data output
GPO1–3	General purpose output

The MFPs default to High-Z state. MFP1 can be programmed to be signal $\overline{\text{INT}}$ or GPO1. MFP2 can be programmed to be signal OUTSEL, DIN2, DOUT2 or GPO2. MFP3 can be programmed to be signal DIN3, DOUT or GPO3. Table 14 summarizes the MFP configuration options with the default functionality shown in bold.

Table 14. MFP Configuration Options

Pin Name	Pin Number	Signal Options
MFP1	#10 (QFN) #13 (eTQFP)	**High-Z,** $\overline{\text{INT}}$, GPO1
MFP2	#11 (QFN) #14 (eTQFP)	**High-Z,** OUTSEL, DIN2, DOUT, GPO2
MFP3	#7 (QFN) #10 (eTQFP)	**High-Z,** DIN3, DOUT, GPO3

The Si270x can receive digital I^2S audio signal from up to three different sources with the default configuration being only one input. For cases where more than one signal input is desired or alternatively a signal output is desired, the MFPs should be programmed to an appropriate configuration with additional DINx/DOUT signals.

Three general purpose output (GPO) pins are also available. The GPOs can be programmed to output logic 1, logic 0, or a Hi-Z state. These pins can be used for example to control multiplexer switches in the application via the 2-Wire bus.

MFP pin function is established using the MFP_PIN_CFG command. Refer to the “AN469: Si270x Programming Guide” for more information on the options and settings requested for operation of the multi function pins.

4.3.2. Output Mode Configuration (Si2705/07 only)

The Si2705/07 can be programmed via 2-Wire or configured using the OUTSEL MFP to operate in three different output modes: 2.1 mode, 2.0 mode and aux out mode, with the 2.0 mode being the default. If OUTSEL is not configured as OUTSEL, these output modes can instead be programmed by setting the argument OUTSEL_MODE of the ACTIVATE command. Refer to the "AN469: Si270x Programming Guide" for more information on the options and settings requested for the different operation modes.

OUTSEL is a three-level input with decoding to configure the analog audio signal output at AUXOL/R pins as shown in Table 15.

Table 15. OUTSEL MFP Decoding

		Description		
OUTSEL	**Output Configuration**	**H-Bridge Amplifier**	**Aux Channel Analog Output (mono aux out)**	**Main Channel Analog Output (stereo aux out)**
GND	Aux Out Mode	disable	disable	enable
$V_{IO}/2$	2.0 Mode	enable	disable	disable
V_{IO}	2.1 Mode	enable	enable	disable

For stereo implementations, the 2.0 mode is selected enabling the main channel stereo power stage outputs. This is the default mode when OUTSEL is not externally driven, or when OUTSEL is driven to mid-level between V_{IO} and GND.

In 2.1 mode, with OUTSEL driven high to V_{IO}, the main channel stereo power stage is enabled to drive stereo bridge-tied loads while a PWM DAC produces mono analog audio from the auxiliary channel to drive a subwoofer or central channel analog input amplifier.

To drive an external stereo analog amplifier (e.g., for headphones) the PWM DAC can be configured to output the main stereo channel. In this case, OUTSEL is driven low to GND.

To avoid unwanted audible pop noises on the output, the Si270x implements circuitry to minimize the output transients that occur while charging and discharging the PWM DAC ac coupling capacitor (see C10 and C11 in the typical application schematic on page 13). The click and pop noise reduction circuit controls the charging and discharging currents on the capacitors to prevent sudden changes in the output bias level and the consequent glitches in the output voltage.

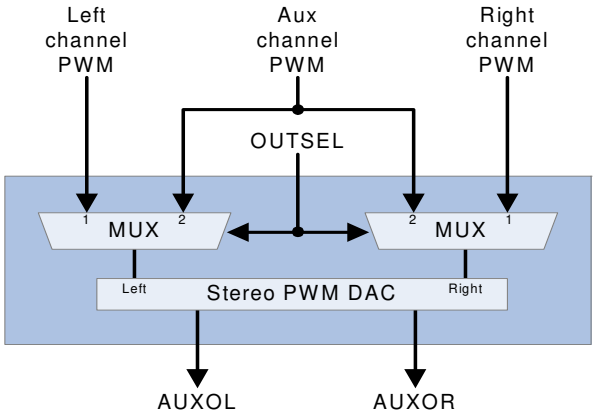


Figure 15. MUX OUTSEL Configuration

OUTSEL can be driven by a headphone plug detection circuit as shown in Figure 16. The ratio between the two resistors in the diagram configures the outputs for a 2.0 (with R1=R2) or a 2.1 application (with R2>>R1). In this application example, OUTSEL may be used for enabling and disabling the external amplifiers.

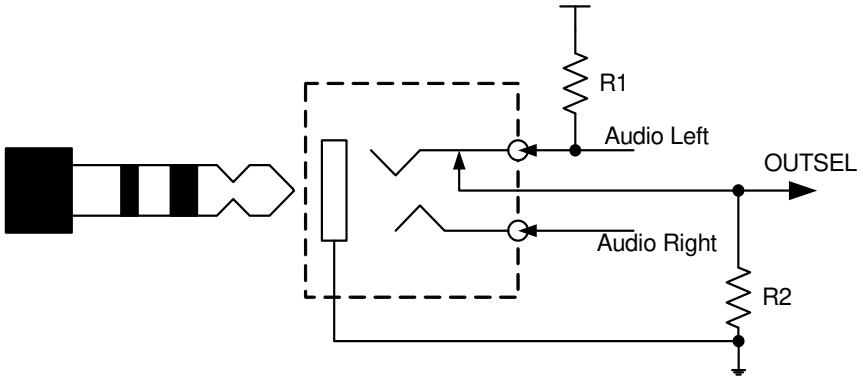


Figure 16. Headphone Plug Detection Application Schematic

4.4. Clocking

A low jitter on-chip PLL synchronizes to an external clock reference and generates all necessary internal clocks. Three options are available for the external reference: a crystal, a reference clock or the digital I^2S audio bit clock.

In addition, a buffered user-programmable output clock can be generated on the CLKO pin for use as a clock reference for external circuits.

4.4.1. Reference Clock Input

Using an external crystal, the on-chip crystal oscillator generates a precise, low jitter internal clock reference for the best audio performance.

For system design flexibility, the device also supports the options to use either an external reference clock or the I^2S bit clock as the PLL reference. Noise performance of the amplifier is a direct function of the jitter characteristics of the external source.

The source of the external reference is programmed using the CLOCK_SOURCE property through the 2-Wire interface.

4.4.1.1. Crystal Oscillator Operation

When a crystal is connected between XTLI and XTLO pins and the chip is configured properly all the timing for the chip is derived from the on-chip crystal oscillator.

A range of crystals are supported and the device needs to be programmed to the selected frequency using the CLOCK_REF_FREQ property. The crystal oscillator provides the best audio performance.

4.4.1.2. External Reference Clock Operation

In this mode, the device operates in slave clock mode and the reference clock is provided by an external clock source on pin XTLI. A wide range of input clock frequencies are supported in this mode ranging from 2.048 to 49 MHz. Refer to Table 11 on page 12 or to the “AN469: Si270x Programming Guide” for more information on the complete range of frequencies and settings required for operation on this mode.

4.4.1.3. I^2S Reference Clock Operation

The device can operate in slave clock mode using the DCLK signal from the I^2S bus as a timing reference. In this mode the device needs to be programmed for one of the supported I^2S clock rates and pin XTLI should be connected to ground.

4.4.2. Reference Clock Output

The Si2704/05/06/07 may provide a buffered output clock to be used as reference for external circuits when the chip is programmed for either Active or Standby mode. The clock output frequency and synchronization source is programmable.

The Si270x supports a number of reference clock frequencies that are related to the PWM switching rate. These CLKO output frequencies can be especially useful for synchronizing the amplifier to switching power supplies.

Refer to the “AN469: Si270x Programming Guide” for more information on the settings requested for operation.

4.5. Digital Audio I²S Interface

The Si270x receives digital audio data using its I²S interface. I²S inputs DIN2 and DIN3 can be configured as either an input or output while DIN is restricted to input only, and all three can be configured to operate in either master or slave mode. Only one output is supported at a time. All data ports operate synchronously from a single bit-clock and frame-clock signal. During normal operation, the crossbar mixer outputs are independently programmed to be a linear combination of any of the channels from the configured inputs with a scaling range from –1 to +1 for each channel with 8-bit precision.

4.5.1. Auto-Rate Detection

The Si270x features an auto-rate detector. It actively monitors the I²S bit and frame clock inputs during operation, detects rate changes, and makes the necessary adjustments to various clock system parameters to ensure correct operation of the amplifier.

4.5.2. Audio Activity Detector

The device has an audio activity detector (AAD) that monitors the presence of audio at the input. In normal operation, if the input audio level falls below a programmable threshold for a programmable period of time, it causes the device to enter the low power Standby Mode. When the input audio level subsequently increases above the threshold, the device returns to normal Active Mode.

4.5.3. Digital Audio Output

The Si270x provides a bypass mode that routes I²S audio input directly to the I²S output port. The output port in turn can be connected to an off-chip device such as a DAC, DSP or digital media controller.

4.5.4. Audio data formats

The digital audio interface supports 3 different audio data formats: I²S, Left-Justified and DSP Mode.

In I²S mode, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high. Figure 17 shows a diagram for the I²S digital audio format.

In Left-Justified mode, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low. Figure 18 shows a diagram for the Left-Justified digital audio format.

In DSP mode, the DFS becomes a pulse, one DCLK period wide. The left channel is transferred first, followed immediately by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge. Figure 19 shows a diagram for the DSP digital audio format.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In this event, for power saving, in I²S slave mode DCLK sent to the Si270x can be programmed to remain low until the next DFS transition appears.

The device supports both rising edge and falling edge DCLK. The number of audio bits in each audio sample defaults to 24 bits and can be configured to 16, 20, 24 or 32 bits. The leading edge and the data format are selected using the DIGITAL_AUDIO_CONFIG property.

4.5.5. I²S Master Mode

In master mode, the Si270x is configured for 32-bit word per audio sample, rising edge DCLK, and I²S mode data format.

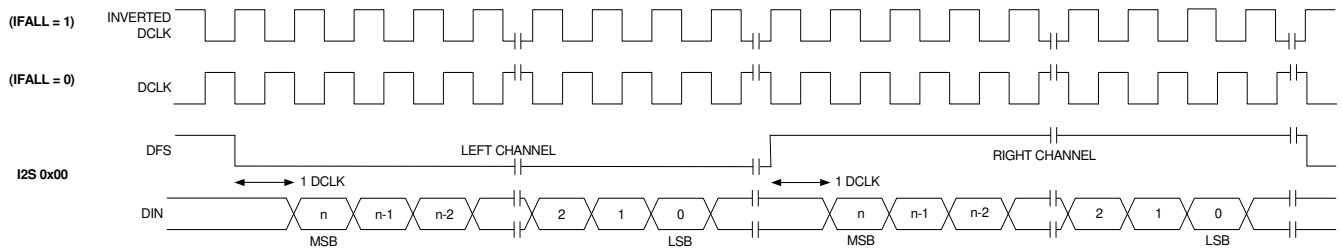


Figure 17. I²S Digital Audio Format

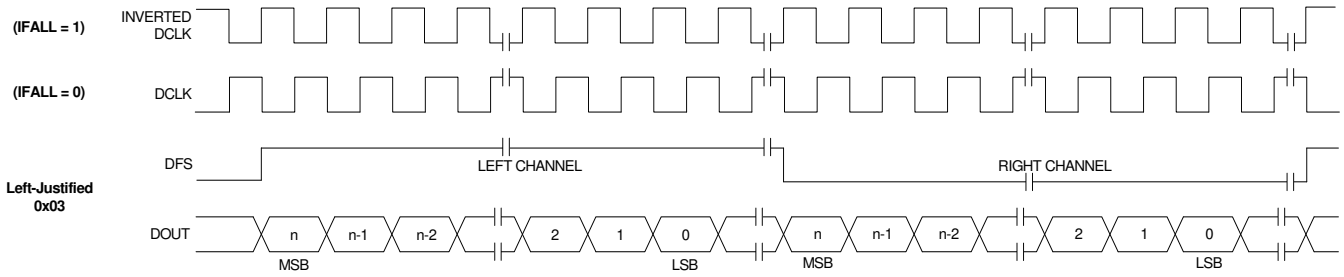


Figure 18. Left-Justified Digital Audio Format

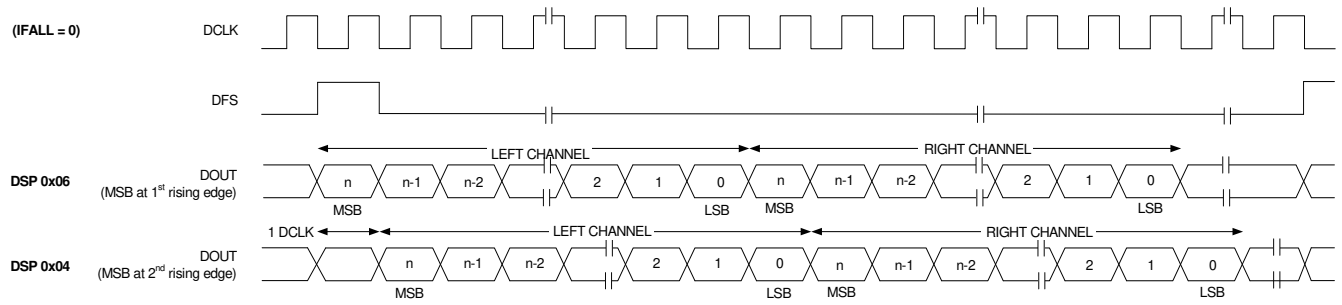


Figure 19. DSP Digital Audio Format